DISCRETE SEMICONDUCTORS

Small-signal Field-effect Transistors

1998

Data Handbook SC07

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In striving for state-of-the-art perfection, we continuously improve components and processes with respect to environmental demands. Our components offer no hazard to the environment in normal use when operated or stored within the limits specified in the data sheet.

Some components unavoidably contain substances that, if exposed by accident or misuse, are potentially hazardous to health. Users of these components are informed of the danger by warning notices in the data sheets supporting the components. Where necessary the warning notices also indicate safety precautions to be taken and disposal instructions to be followed. Obviously users of these components, in general the set-making industry, assume responsibility towards the consumer with respect to safety matters and environmental demands.

All used or obsolete components should be disposed of according to the regulations applying at the disposal location. Depending on the location, electronic components are considered to be 'chemical', 'special' or sometimes 'industrial' waste. Disposal as domestic waste is usually not permitted.

Small-signal Field-effect Transistors

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DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

Small-signal Field effect Transistors — Preface

Dear Customer,

Welcome to the latest edition of the SC07 data handbook “Small-signal Field-effect Transistors”.

It contains data on our extensive range of JFETs and Dual Gate MOSFETs, while information on our vertical D-MOSFETs can now be found in data handbook SC13B.

Several new devices have been introduced since the last edition of SC07, including BF1105, R, WR and BF1109, R, WR. These Dual Gate MOSFETs are specifically developed for TV/VCR tuner applications and provide fully integrated DC biasing.

For spice parameters or the latest information on all Philips Semiconductors’ products, visit our WWW site at http://www.semiconductors.philips.com/. Or call your local Philips Semiconductors sales office or franchised distributor from the address list on the back page of this book.

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N-CHANNEL JUNCTION FIELD-EFFECT TRANSISTORS

TYPE NUMBER	PACKAGE	$\pm V_{DS}$ (V)	CHARACTERISTICS					PAGE
			I_G (mA)	I_{DSS} min - max (mA)	$-V_{(P)GS}$ (V)	$\lvert y_{fs} \rvert$ (mS)	C_{rs} (pF)	
General purpose analog applications								
J210	TO-92	25	10	2 to 15	1 to 3	4	0.8	291
J211	TO-92	25	10	7 to 20	2.5 to 4.5	6	0.8	291
J212	TO-92	25	10	15 to 40	4 to 6	7	0.8	291
PMBFJ210	SOT23	25	10	2 to 15	1 to 3	4	0.8	325
PMBFJ211	SOT23	25	10	7 to 20	2.5 to 4.5	6	0.8	325
PMBFJ212	SOT23	25	10	15 to 40	4 to 6	7	0.8	325
DC, LF and HF amplifiers								
BF245A	TO-92 variant	30	10	2 to 6.5	<8	3 to 6.5	1.1	87
BF245B	TO-92 variant	30	10	6 to 15	<8	3 to 6.5	1.1	87
BF245C	TO-92 variant	30	10	12 to 25	<8	3 to 6.5	1.1	87
BF545A	SOT23	30	10	2 to 6.5	0.4 to 7.5	3 to 6.5	0.8	102
BF545B	SOT23	30	10	6 to 15	0.4 to 7.5	3 to 6.5	0.8	102
BF545C	SOT23	30	10	12 to 25	0.4 to 7.5	3 to 6.5	0.8	102
BF556A	SOT23	30	10	3 to 7	0.5 to 7.5	4.5	0.8	111
BF556B	SOT23	30	10	6 to 13	0.5 to 7.5	4.5	0.8	111
BF556C	SOT23	30	10	11 to 18	0.5 to 7.5	4.5	0.8	111
Preamplifiers for AM tuners in car radios								
BF851A	TO-92	25	10	2 to 6.5	0.2 to 1.0	12	2.4	119
BF851B	TO-92	25	10	6 to 15	0.5 to 1.5	16	2.4	119
BF851C	TO-92	25	10	12 to 25	0.8 to 2.0	20	2.4	119
BF861A	SOT23	25	10	2 to 6.5	0.2 to 1.0	12	2.1	127
BF861B	SOT23	25	10	6 to 15	0.5 to 1.5	16	2.1	127
BF861C	SOT23	25	10	12 to 25	0.8 to 2.0	20	2.1	127
RF stages FM portables, car radios, mains radios and mixer stages								
BF410A(1)	TO-92 variant	20	10	0.7 to 3	typ. 0.8	2.5	0.5	95
BF410B(1)	TO-92 variant	20	10	2.5 to 7	typ. 1.5	4	0.5	95
BF410C(1)	TO-92 variant	20	10	6 to 12	typ. 2.2	6	0.5	95
BF410D(1)	TO-92 variant	20	10	10 to 18	typ. 3	7	0.5	95
BF510(1)	SOT23	20	10	0.7 to 3	typ. 0.8	2.5	0.4	98
BF511(1)	SOT23	20	10	2.5 to 7	typ. 1.5	4	0.4	98
BF512(1)	SOT23	20	10	6 to 12	typ. 2.2	6	0.4	98
BF513(1)	SOT23	20	10	10 to 18	typ. 3	7	0.4	98

N-CHANNEL JUNCTION FIELD-EFFECT TRANSISTORS (continued)

TYPE NUMBER	PACKAGE	±V_{DS} (V)	CHARACTERISTICS					PAGE
			I_G (mA)	I_{DSS} min - max (mA)	$-V_{(P)GS}$ (V)	$\lvert y_{fs} \rvert$ (mS)	C_{rs} (pF)	
Low level general purpose amplifiers								
BFR30	SOT23	25	5	4 to 10	<5	1 to 4	1.5	256
BFR31	SOT23	25	5	1 to 5	<2.5	1.5 to 4.5	1.5	256
General purpose amplifiers								
BFT46	SOT23	25	5	0.2 to 1.5	<1.2	>1	1.5	264
AM input stages UHF/VHF amplifiers								
PMBF4416	SOT23	30	10	5 to 15	<6	4.5 to 7.5	<0.8	303
PMBF4416A	SOT23	35	10	5 to 15	2.5 to 6	4.5 to 7.5	<0.8	303
PMBF5484	SOT23	25	10	1 to 5	0.3 to 3	3 to 6	<1	309
PMBF5485	SOT23	25	10	4 to 10	0.5 to 4	3.5 to 7	<1	309
PMBF5486	SOT23	25	10	8 to 20	2 to 6	4 to 8	<1	309
PMBFJ308	SOT23	25	50	12 to 60	1 to 6.5	>10	1.3	333
PMBFJ309	SOT23	25	50	12 to 30	1 to 4	>10	1.3	333
PMBFJ310	SOT23	25	50	24 to 60	2 to 6.5	>10	1.3	333
PN4416	TO-92	30	10	5 to 15	<6	4.5 to 7.5	0.8	345
PN4416A	TO-92	35	10	5 to 15	2.5 to 6	4.5 to 7.5	0.8	345
2N5484	TO-92	25	10	1 to 5	0.3 to 3	3 to 6	<1	80
2N5485	TO-92	25	10	4 to 10	0.5 to 4	3.5 to 7	<1	80
2N5486	TO-92	25	10	8 to 20	2 to 6	4 to 8	<1	80

Note

1. Asymmetrical.

N-CHANNEL JUNCTION FIELD-EFFECT TRANSISTORS FOR SWITCHING

TYPE NUMBER	PACKAGE	RATINGS		CHARACTERISTICS								PAGE
		V_{DS} (V)	I_G (mA)	I_{DSS} (mA)		$-V_{(P)GS}$ (V)		R_{DSon} max. (Ω)	C_{rs} max. (pF)	t_{on} max. (ns)	t_{off} max. (ns)	
				min.	max.	min.	max.					
BSR56	SOT23	40	50	50	–	4	10	25	5	–	25	273
BSR57	SOT23	40	50	20	100	2	6	40	5	–	50	273
BSR58	SOT23	40	50	8	80	0.8	4	60	5	–	100	273
J108	TO-92	25	50	80	–	3	10	8	15	typ. 4	typ. 6	281
J109	TO-92	25	50	40	–	2	6	12	15	typ. 4	typ. 6	281
J110	TO-92	25	50	10	–	0.5	4	18	15	typ. 4	typ. 6	281
J111	TO-92	40	50	20	–	3	10	30	typ. 3	typ. 13	typ. 35	285

N-CHANNEL JUNCTION FIELD-EFFECT TRANSISTORS FOR SWITCHING (continued)

TYPE NUMBER	PACKAGE	RATINGS		CHARACTERISTICS								PAGE
		V_{DS} (V)	I_G (mA)	I_{DSS} (mA)		$-V_{(P)GS}$ (V)		R_{DSon} max. (Ω)	C_{rs} max. (pF)	t_{on} max. (ns)	t_{off} max. (ns)	
				min.	max.	min.	max.					
J112	TO-92	40	50	5	–	1	5	50	typ. 3	typ. 13	typ. 35	285
J113	TO-92	40	50	2	–	0.5	3	100	typ. 3	typ. 13	typ. 35	285
PMBF4391	SOT23	40	50	50	150	4	10	30	3.5	15	20	299
PMBF4392	SOT23	40	50	25	75	2	5	60	3.5	15	35	299
PMBF4393	SOT23	40	50	5	30	0.5	3	100	3.5	15	50	299
PMBFJ108	SOT23	25	50	80	–	3	10	8	15	typ. 4	typ. 6	316
PMBFJ109	SOT23	25	50	40	–	2	6	12	15	typ. 4	typ. 6	316
PMBFJ110	SOT23	25	50	10	–	0.5	4	18	15	typ. 4	typ. 6	316
PMBFJ111	SOT23	40	50	20	–	3	10	30	typ. 3	typ. 13	typ. 35	319
PMBFJ112	SOT23	40	50	5	–	1	5	50	typ. 3	typ. 13	typ. 35	319
PMBFJ113	SOT23	40	50	2	–	0.5	3	100	typ. 3	typ. 13	typ. 35	319
PN4391	TO-92	40	50	50	–	4	10	30	5	15	20	342
PN4392	TO-92	40	50	25	–	2	5	60	5	15	35	342
PN4393	TO-92	40	50	5	–	0.5	3	100	5	15	50	342

P-CHANNEL JUNCTION FIELD-EFFECT TRANSISTORS FOR SWITCHING

TYPE NUMBER	PACKAGE	RATINGS		CHARACTERISTICS								PAGE
		V_{DS} (V)	I_G (mA)	I_{DSS} (mA)		$-V_{(P)GS}$ (V)		R_{DSon} max. (Ω)	C_{rs} typ. (pF)	t_{on} typ. (ns)	t_{off} typ. (ns)	
				min.	max.	min.	max.					
J174	TO-92	30	50	20	135	5	10	85	4	7	15	288
J175	TO-92	30	50	7	70	3	6	125	4	15	30	288
J176	TO-92	30	50	2	35	1	4	250	4	35	35	288
J177	TO-92	30	50	1.5	20	0.8	2.25	300	4	45	45	288
PMBFJ174	SOT23	30	50	20	135	5	10	85	4	7	15	322
PMBFJ175	SOT23	30	50	7	70	3	6	125	4	15	30	322
PMBFJ176	SOT23	30	50	2	35	1	4	250	4	35	35	322
PMBFJ177	SOT23	30	50	1.5	20	0.8	2.25	300	4	45	45	322

N-CHANNEL, SINGLE GATE MOS-FETS FOR SWITCHING

TYPE NUMBER	PACKAGE	RATINGS		CHARACTERISTICS								PAGE
		V_{DS} (V)	I_D (mA)	I_{DSS} (mA)		$-V_{(P)GS}$ (V)		MODE	R_{DSon} max. (Ω)	C_{rss} typ. (pF)	t_{on}/t_{off} max. (ns)	
				min.	max.	min.	max.					
BSD22	SOT143	20	50	–	–	–	2	depl.	30	0.6	1/5	270
BSS83	SOT143	10	50	–	–	0.1[1]	2[1]	enh.	45	0.6	1/5	276

Notes

1. $V_{GS(th)}$.

N-CHANNEL, DUAL GATE MOS-FETS

All types protected against excessive input voltage surges.

TYPE NUMBER	PACKAGE	RATINGS		CHARACTERISTICS						REMARKS	PAGE
		V_{DS} (V)	I_D (mA)	I_{DSS} min. max. (mA)	$-V_{(P)GS}$ max. (V)	$\|y_{fs}\|$ min. (mS)	C_{is} typ. (pF)	C_{os} typ. (pF)	F typ. (dB) at 800 MHz		
BF901	SOT143	12	30	–	0.7[1]	25	2.35	1.4	1.7	VHF & UHF	135
BF901R	SOT143R	12	30	–	0.7[1]	25	2.35	1.4	1.7	VHF & UHF	135
BF904	SOT143	7	30	–	1[1]	22	2.2	1.3	2	VHF & UHF	138
BF904R	SOT143R	7	30	–	1[1]	22	2.2	1.3	2	VHF & UHF	138
BF904WR	SOT343R	7	30	–	1[1]	22	2.2	1.3	2	VHF & UHF	147
BF908	SOT143	12	40	3 to 27	2	36	3.1	1.7	1.5	VHF & UHF	156
BF908R	SOT143R	12	40	3 to 27	2	36	3.1	1.7	1.5	VHF & UHF	156
BF908WR	SOT343R	12	40	3 to 27	2	36	3.1	1.7	1.5	VHF & UHF	161
BF909	SOT143	7	40	–	1[1]	36	3.6	2.3	2	VHF & UHF	165
BF909R	SOT143R	7	40	–	1[1]	36	3.6	2.3	2	VHF & UHF	165
BF909WR	SOT343R	7	40	–	1[1]	36	3.6	2.3	2	VHF & UHF	173
BF989	SOT143	20	20	2 to 20	2.7	9.5	1.8	0.9	2.8	UHF	181
BF990A	SOT143	18	30	–	1.3	18	2.6	1.2	2	UHF	184
BF991	SOT143	20	20	4 to 25	2.5	10	2.1	1.1	0.7[2]	VHF	187
BF992	SOT143	20	40	–	1.3	20	4	2	1.2[2]	VHF	190
BF992R	SOT143R	20	40	–	1.3	20	4	2	1.2[2]	VHF	190
BF994S	SOT143	20	30	4 to 20	2.5	15	2.5	1	1[2]	VHF	195
BF996S	SOT143	20	30	4 to 20	2.5	15	2.3	0.8	1.8	UHF	198
BF998	SOT143	12	30	2 to 18	2.5	21	2.1	1.05	1	VHF & UHF	201
BF998R	SOT143R	12	30	2 to 18	2.5	21	2.1	1.05	1	VHF & UHF	201
BF998WR	SOT343R	12	30	2 to 18	2.5	22	2.1	1.05	1	VHF & UHF	210

N-CHANNEL, DUAL GATE MOS-FETS (continued)

All types protected against excessive input voltage surges.

TYPE NUMBER	PACKAGE	RATINGS		CHARACTERISTICS						REMARKS	PAGE
		V_{DS} (V)	I_D (mA)	I_{DSS} min.. max. (mA)	$-V_{(P)GS}$ max. (V)	$\|y_{fs}\|$ min. (mS)	C_{is} typ. (pF)	C_{os} typ. (pF)	F typ. (dB) at 800 MHz		
BF1100	SOT143	14	30	–	1(1)	24	2.2	1.4	2	VHF & UHF	218
BF1100R	SOT143R	14	30	–	1(1)	24	2.2	1.4	2	VHF & UHF	218
BF1100WR	SOT343R	14	30	–	1(1)	24	2.2	1.4	2	VHF & UHF	229
BF1105	SOT143	7	30	–	–	25	2.2	–	1.7	VHF & UHF	240
BF1105R	SOT143R	7	30	–	–	25	2.2	–	1.7	VHF & UHF	240
BF1105WR	SOT343R	7	30	–	–	25	2.2	–	1.7	VHF & UHF	240
BF1109	SOT143	11	30	–	1.2(1)	30	2.2	–	1.5	VHF & UHF	248
BF1109R	SOT143R	11	30	–	1.2(1)	30	2.2	–	1.5	VHF & UHF	248
BF1109WR	SOT343R	11	30	–	1.2(1)	30	2.2	–	1.5	VHF & UHF	248

Notes

1. $V_{GS(th)}$.
2. At 200 MHz.

REPLACED/WITHDRAWN TYPES

The following type numbers were included in the previous issue of this data handbook, but are not in the current edition.

TYPE NUMBER	REASON FOR DELETION
2N4091	Discontinued
2N4092	Discontinued
2N4093	Discontinued
2N4391	Discontinued
2N4392	Discontinued
2N4393	Discontinued
2N4416	Discontinued
2N4416a	Discontinued
2N4856	Discontinued
2N4857	Discontinued
2N4858	Discontinued
2N4859	Discontinued
2N4860	Discontinued
2N4861	Discontinued
BC264A; BC264B; BC264C; BC264D	Discontinued. Replaced by BF245A-C
BF246A; BF246B; BF246C; BF247A; BF247B; BF247C	Discontinued
BF256A; BF256B; BF256C	Discontinued. Replaced by BF245A-C
BF990AR	Discontinued. Replaced by BF990A
BFR29	Discontinued
BFU308; BFU309; BFU310	Discontinued
BFW10; BFW11	Discontinued. Replaced by BF245A-C
BFW12; BFW13	Discontinued. Replaced by BF245A-C
BSD12	Discontinued
BSD211	Discontinued
BSD212	Discontinued
BSD213	Discontinued
BSD214	Discontinued
BSD215	Discontinued
BSV78	Discontinued
BSV79	Discontinued2N40
BSV80	Discontinued
BSV81	Discontinued
J308; J309; J310	Discontinued. Replaced by J108-110
PZFJ108; PZFJ109; PZFJ110	Discontinued. Replaced by J108-110

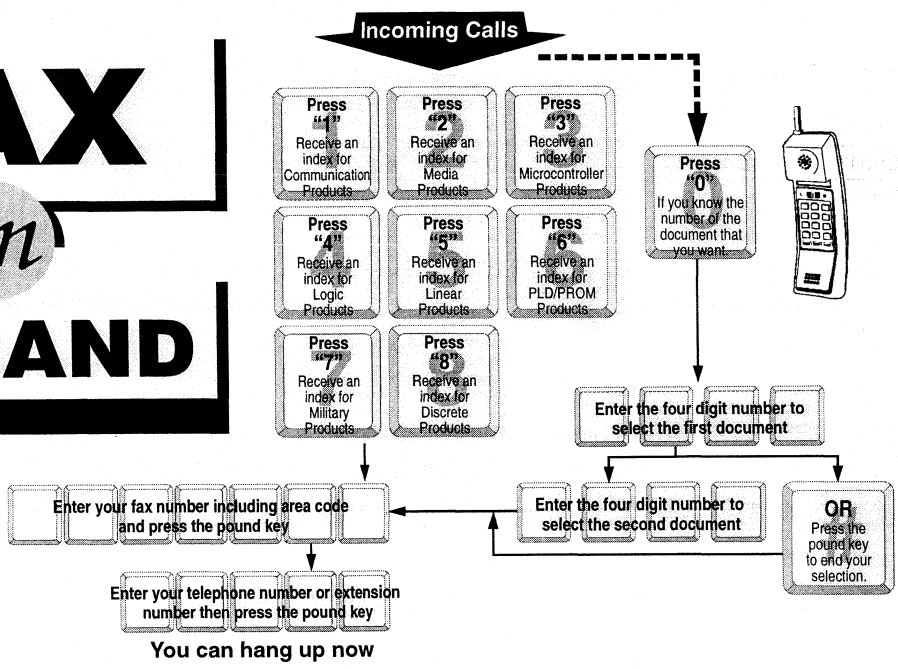
Types in SOT23, SOT89, SOT143 and SOT343 packages are marked with a code as listed in the following table.

TYPE NUMBER	MARKING CODE
BF510	S6p
BF511	S7p
BF512	S8p
BF513	S9p
BF545A	M65
BF545B	M66
BF545C	M67
BF556A	M84
BF556B	M85
BF556C	M86
BF861A	M33
BF861B	M34
BF861C	M35
BF901	M01
BF901R	M02
BF904	M04
BF904R	M06
BF904WR	MC
BF908	M26
BF908R	M27
BF908WR	MD
BF909	M28
BF909R	M29
BF989	MAp
BF990A	M87

TYPE NUMBER	MARKING CODE
BF991	M91
BF992	M92
BF992R	M52
BF994S	MGp
BF996S	MHp
BF998	MOp
BF998R	MO$\overline{p}$
BF998WR	MB
BF1100	M56
BF1100R	M57
BF1100WR	MF
BF1105	NEp
BF1105R	NAp
BF1105WR	NA
BF1109	NFp
BF1109R	NBp
BF1109WR	NB
BFR30	M1p
BFR31	M2p
BFT46	M3p
BSD22	M32
BSR56	M4p
BSR57	M5p
BSR58	M6p
BSS83	M74

TYPE NUMBER	MARKING CODE
PMBF4391	p6J
PMBF4392	p6K
PMBF4393	p6G
PMBF4416	p6A
PMBF4416A	M16
PMBF5484	p6B
PMBF5485	p6M
PMBF5486	p6H
PMBFJ108	p08
PMBFJ109	p09
PMBFJ110	p10
PMBFJ111	p11
PMBFJ112	p12
PMBFJ113	p13
PMBFJ174	p6X
PMBFJ175	p6W
PMBFJ176	p6S
PMBFJ177	p6Y
PMBFJ210	M68
PMBFJ211	M69
PMBFJ212	M70
PMBFJ308	M08
PMBFJ309	M09
PMBFJ310	M10

FAX-on-DEMAND System



What is it?

The FAX-on-DEMAND system is a computer facsimile system that allows customers to receive selected documents by fax automatically.

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GENERAL

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QUALITY

Total Quality Management

Philips Semiconductors is a Quality Company, renowned for the high quality of our products and service. We keep alive this tradition by constantly aiming towards one ultimate standard, that of zero defects. This aim is guided by our Total Quality Management (TQM) system, the basis of which is described in the following paragraphs.

QUALITY ASSURANCE

Based on ISO 9000 standards, customer standards such as Ford TQE and IBM MDQ. Our factories are certified to ISO 9000 by external inspectorates.

PARTNERSHIPS WITH CUSTOMERS

PPM co-operations, design-in agreements, ship-to-stock, just-in-time and self-qualification programmes, and application support.

PARTNERSHIPS WITH SUPPLIERS

Ship-to-stock, statistical process control and ISO 9000 audits.

QUALITY IMPROVEMENT PROGRAMME

Continuous process and system improvement, design improvement, complete use of statistical process control, realization of our final objective of zero defects, and logistics improvement by ship-to-stock and just-in-time agreements.

Advanced quality planning

During the design and development of new products and processes, quality is built-in by advanced quality planning. Through failure-mode-and-effect analysis the critical parameters are detected and measures taken to ensure good performance on these parameters. The capability of process steps is also planned in this phase.

Product conformance

The assurance of product conformance is an integral part of our quality assurance (QA) practice. This is achieved by:

- Incoming material management through partnerships with suppliers.
- In-line quality assurance to monitor process reproducibility during manufacture and initiate any necessary corrective action. Critical process steps are 100% under statistical process control.
- Acceptance tests on finished products to verify conformance with the device specification. The test results are used for quality feedback and corrective actions. The inspection and test requirements are detailed in the general quality specifications.
- Periodic inspections to monitor and measure the conformance of products.

Product reliability

With the increasing complexity of Original Equipment Manufacturer (OEM) equipment, component reliability must be extremely high. Our research laboratories and development departments study the failure mechanisms of semiconductors. Their studies result in design rules and process optimization for the highest built-in product reliability. Highly accelerated tests are applied to the products reliability evaluation. Rejects from reliability tests and from customer complaints are submitted to failure analysis, to result in corrective action.

Customer responses

Our quality improvement depends on joint action with our customer. We need our customer's inputs and we invite constructive comments on all aspects of our performance. Please contact our local sales representative.

Recognition

The high quality of our products and services is demonstrated by many Quality Awards granted by major customers and international organizations.

PRO ELECTRON TYPE NUMBERING SYSTEM

Basic type number

This type designation code applies to discrete semiconductor devices (not integrated circuits), multiples of such devices, semiconductor chips and Darlington transistors.

FIRST LETTER

The first letter gives information about the material for the active part of the device.

A germanium or other material with a band gap of 0.6 to 1 eV

B silicon or other material with a band gap of 1 to 1.3 eV

C gallium arsenide (GaAs) or other material with a band gap of 1.3 eV or more

R compound materials, e.g. cadmium sulphide

SECOND LETTER

The second letter indicates the function for which the device is primarily designed. The same letter can be used for multi-chip devices with similar elements.

In the following list low power types are defined by $R_{th\ j\text{-}mb}$ > 15 K/W and power types by $R_{th\ j\text{-}mb} \leq$ 15 K/W.

- A diode; signal, low power
- B diode; variable capacitance
- C transistor; low power, audio frequency
- D transistor; power, audio frequency
- E diode; tunnel
- F transistor; low power, high frequency
- G multiple of dissimilar devices/miscellaneous devices; e.g. oscillators. Also with special third letter; see under Section "Serial number".
- H diode; magnetic sensitive
- L transistor; power, high frequency
- N photocoupler
- P radiation detector; e.g. high sensitivity photo-transistor; with special third letter
- Q radiation generator; e.g. LED, laser; with special third letter
- R control or switching device; e.g. thyristor, low power; with special third letter
- S transistor; low power, switching
- T control or switching device; e.g. thyristor, low power; with special third letter
- U transistor; power, switching
- W surface acoustic wave device
- X diode; multiplier, e.g. varactor, step recovery
- Y diode; rectifying, booster
- Z diode; voltage reference or regulator, transient suppressor diode; with special third letter.

SERIAL NUMBER

The number comprises three figures running from 100 to 999 for devices primarily intended for consumer equipment, or one letter (Z, Y, X, etc.) and two figures running from 10 to 99 for devices primarily intended for industrial or professional equipment.[1]

(1) When the supply of these serial numbers is exhausted, the serial number may be expanded to three figures for industrial types and four figures for consumer types.

Version letter

A letter may be added to the basic type number to indicate minor electrical or mechanical variants of the basic type.

RATING SYSTEMS

The rating systems described are those recommended by the IEC in its publication number 134.

Definitions of terms used

ELECTRONIC DEVICE

An electronic tube or valve, transistor or other semiconductor device. This definition excludes inductors, capacitors, resistors and similar components.

CHARACTERISTIC

A characteristic is an inherent and measurable property of a device. Such a property may be electrical, mechanical, thermal, hydraulic, electro-magnetic or nuclear, and can be expressed as a value for stated or recognized conditions. A characteristic may also be a set of related values, usually shown in graphical form.

BOGEY ELECTRONIC DEVICE

An electronic device whose characteristics have the published nominal values for the type. A bogey electronic device for any particular application can be obtained by considering only those characteristics that are directly related to the application.

RATING

A value that establishes either a limiting capability or a limiting condition for an electronic device. It is determined for specified values of environment and operation, and may be stated in any suitable terms. Limiting conditions may be either maxima or minima.

RATING SYSTEM

The set of principles upon which ratings are established and which determine their interpretation. The rating system indicates the division of responsibility between the device manufacturer and the circuit designer, with the object of ensuring that the working conditions do not exceed the ratings.

Absolute maximum rating system

Absolute maximum ratings are limiting values of operating and environmental conditions applicable to any electronic

device of a specified type, as defined by its published data, which should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking no responsibility for equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in the characteristics of the device under consideration and of all other electronic devices in the equipment.

The equipment manufacturer should design so that, initially and throughout the life of the device, no absolute maximum value for the intended service is exceeded with any device, under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, equipment control adjustment, load variations, signal variation, environmental conditions, and variations in characteristics of the device under consideration and of all other electronic devices in the equipment.

Design maximum rating system

Design maximum ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking responsibility for the effects of changes in operating conditions due to variations in the characteristics of the electronic device under consideration.

The equipment manufacturer should design so that, initially and throughout the life of the device, no design maximum value for the intended service is exceeded with a bogey electronic device, under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, variation in characteristics of all other devices in the equipment, equipment control adjustment, load variation, signal variation and environmental conditions.

Design centre rating system

Design centre ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under normal conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device in average applications, taking responsibility for normal changes in operating conditions due to rated supply voltage variation, equipment component variation, equipment control adjustment, load variation, signal variation, environmental conditions, and variations in the characteristics of all electronic devices.

The equipment manufacturer should design so that, initially, no design centre value for the intended service is exceeded with a bogey electronic device in equipment operating at the stated normal supply voltage.

LETTER SYMBOLS

The letter symbols for transistors detailed in this section are based on IEC publication number 148.

Basic letters

In the representation of currents, voltages and powers, lower-case letter symbols are used to indicate all instantaneous values that vary with time. All other values are represented by upper-case letters.

Electrical parameters[(1)] of external circuits and of circuits in which the device forms only a part are represented by upper-case letters. Lower-case letters are used for the representation of electrical parameters inherent in the device. Inductances and capacitances are always represented by upper-case letters.

The following is a list of basic letter symbols used with semiconductor devices:

B, b susceptance (imaginary part of an admittance)
C capacitance
G, g conductance (real part of an admittance)
H, h hybrid parameter
I, i current
L inductance
P, p power
R, r resistance (real part of an impedance)
V, v voltage
X, x reactance (imaginary part of an impedance)
Y, y admittance
Z, z impedance

(1) For the purpose of this publication, the term 'electrical parameters' applies to four-pole matrix parameters, elements of electrical equivalent circuits, electrical impedances and admittances, inductances and capacitances.

Subscripts

Upper-case subscripts are used for the indication of:

- continuous (DC) values (without signal), e.g. I_D
- instantaneous total values, e.g. i_D
- average total values, e.g. $I_{D(AV)}$
- peak total values, e.g. I_{DM}
- root-mean-square total values, e.g. $I_{D(RMS)}$.

Lower-case subscripts are used for the indication of values applying to the varying component alone:

- instantaneous values, e.g. i_b
- root-mean-square values, e.g. $I_{d(rms)}$
- peak values, e.g. I_{dm}
- average values, e.g. $I_{d(av)}$.

The following is a list of subscripts used with basic letter symbols for semiconductor devices:

A, a	anode
amb	ambient
(AV), (av)	average value
B, b	base
(BO)	breakover
(BR)	breakdown
case	case
C, c	collector
C	controllable
D, d	drain
E, e	emitter
F, f	fall, forward (or forward transfer)
G, g	gate
H	holding
h	heatsink
I, i	input
j-a	junction to ambient
j-mb	junction to mounting base
K, k	cathode
L	load
M, m	peak value
(min)	minimum
(max)	maximum
mb	mounting base
O, o	as third subscript: the terminal not mentioned is open-circuit
(OV)	overload
P, p	pulse
Q, q	turn-off
R, r	as first subscript: reverse (or reverse transfer), rise. As second subscript: repetitive, recovery. As third subscript: with a specified resistance between the terminal not mentioned and the reference terminal
(RMS), (rms)	root-mean-square value
S, s	as first subscript: series, source, storage, stray, switching. As second subscript: surge (non-repetitive). As third subscript: short circuit between the terminal not mentioned and the reference terminal
stg	storage
th	thermal
TO	threshold
tot	total
W	working
X, x	specified circuit
Z, z	reference or regulator (zener)
1	input (four-pole matrix)
2	output (four-pole matrix).

Applications and examples

Transistor currents

The first subscript indicates the terminal carrying the current (conventional current flow from the external circuit into the terminal is positive).

Examples: I_D, i_D, i_d, I_{dm}.

Transistor voltages

A voltage is indicated by the first two subscripts: the first identifies the terminal at which the voltage is measured and the second the reference terminal or the circuit node. The second subscript may be omitted when there is no possibility of confusion.

Examples: V_{GS}, v_{GS}, v_{gs}, V_{gsm}.

Supply voltages or currents

Supply voltages or supply currents are indicated by repeating the appropriate terminal subscript.

Examples: V_{DD}, I_{SS}.

A reference terminal is indicated by a third subscript.

Example: V_{DDS}.

DEVICES WITH MORE THAN ONE TERMINAL OF THE SAME KIND

If a device has more than one terminal of the same kind, the subscript is formed by the appropriate letter for the terminal, followed by a number. Hyphens may be used to avoid confusion in multiple subscripts.

Examples:

I_{G2}	continuous (DC) current flowing into the second gate terminal
$V_{G2\text{-}S}$	continuous (DC) voltage between the terminals of second gate and source.

MULTIPLE DEVICES

For multiple unit devices, the subscripts are modified by a number preceding the letter subscript. Hyphens may be used to avoid confusion in multiple subscripts.

Examples:

I_{2D}	continuous (DC) current flowing into the drain terminal of the second unit
$V_{1D\text{-}2D}$	continuous (DC) voltage between the drain terminals of the first and second units.

ELECTRICAL PARAMETERS

The upper-case variant of a subscript is used for the designation of static (DC) values.

Examples:

g_{FS}	static value of forward transconductance in common-source configuration (DC current gain)
R_{DS}	DC value of the drain-source resistance.

The static value is the slope of the line from the origin to the operating point on the appropriate characteristic curve, i.e. the quotient of the appropriate electrical quantities at the operating point.

The lower-case variant of a subscript is used for the designation of small-signal values.

Examples:

g_{fs}	small-signal value of the short-circuit forward transconductance in common-source configuration
$Z_i = R_i + jX_i$	small-signal value of the input impedance.

If more than one subscript is used, subscripts for which a choice of style is allowed, the subscripts chosen are all upper-case or all lower-case.

Examples: h_{FE}, y_{RE}, h_{fe}, g_{FS}.

FOUR-POLE MATRIX PARAMETERS

The first letter subscript (or double numeric subscript) indicates input, output, forward transfer or reverse transfer.

Examples: h_i (or h_{11}), h_o (or h_{22}), h_f (or h_{21}), h_r (or h_{12}).

A further subscript is used for the identification of the circuit configuration. When no confusion is possible, this further subscript may be omitted.

Examples: h_{fe} (or h_{21e}), h_{FE} (or h_{21E}).

DISTINCTION BETWEEN REAL AND IMAGINARY PARTS

If it is necessary to distinguish between real and imaginary parts of electrical parameters, no additional subscripts are used. If basic symbols for the real and imaginary parts exist, these may be used.

Examples: $Z_i = R_i + jX_i$, $y_{fe} = g_{fe} + jb_{fe}$.

If such symbols do not exist or are not suitable, the notation shown in the following examples is used.

Examples:

Re (h_{ib}) etc. for the real part of h_{ib}.

Im (h_{ib}) etc. for the imaginary part of h_{ib}.

S-PARAMETER DEFINITIONS

The S-parameter symbols in this section are based on IEC publication 747-7.

S-parameters (return losses or reflection coefficients) of a module can be defined as the S_{11} and the S_{22} of a two-port network (see Fig.1).

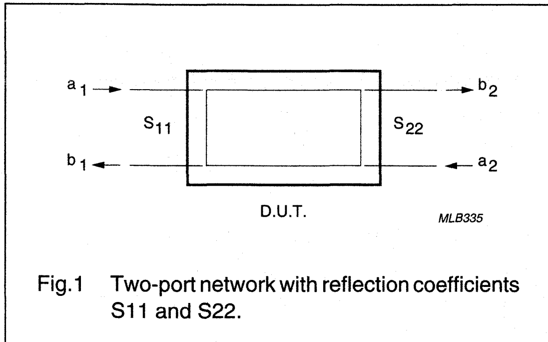


Fig.1 Two-port network with reflection coefficients S11 and S22.

$$b_1 = S_{11} \cdot a_1 + S_{12} \cdot a_2 \quad (1)$$

$$b_2 = S_{21} \cdot a_1 + S_{22} \cdot a_2 \quad (2)$$

where:

$$a_1 = \frac{1}{2 \cdot \sqrt{Z_o}} \cdot (V_1 + Z_o \cdot i_1) = \text{signal into port 1} \quad (3)$$

$$a_2 = \frac{1}{2 \cdot \sqrt{Z_o}} \cdot (V_2 + Z_o \cdot i_2) = \text{signal into port 2}$$

$$b_1 = \frac{1}{2 \cdot \sqrt{Z_o}} \cdot (V_1 + Z_o \cdot i_1) = \text{signal out port 1} \quad (4)$$

$$b_2 = \frac{1}{2 \cdot \sqrt{Z_o}} \cdot (V_1 + Z_o \cdot i_2) = \text{signal out port 2}$$

From (1) and (2) formulae for the return losses can be derived:

$$S_{11} = \frac{b_1}{a_1}\bigg|_{a_2 = 0} \quad (5)$$

$$S_{22} = \frac{b_2}{a_2}\bigg|_{a_1 = 0} \quad (6)$$

In (5), $a_2 = 0$ means output port terminated with Z_o (derived from formula (4)).

In (6), $a_1 = 0$ means input port terminated with Z_o (derived from formula (3)).

Measurement

The return losses are measured with a network analyzer after calibration, where the influence of the test jig is eliminated. The necessary termination of the other port with Z_o is done automatically by the network analyzer.

The network analyser must have a directivity of at least 40 dB to obtain an accuracy of 0.5 dB when measuring return loss figures of 20 dB. A full two-port correction method can be used to improve the accuracy.

TAPE AND REEL PACKING

Tape and reel packing meets the feed requirements of automatic pick and place equipment (packing conforms to IEC publication 286-2 and 286-3). Additionally, the tape is an ideal shipping container.

Packing (TO-92 leaded types)

The transistors are supplied on tape in boxes (ammopack) or on reels. The number per reel and per ammopack is 2000. The ammopack has 80 layers of 25 transistors each. Each layer contains 25 transistors, plus one empty position in order to fold the layer correctly. The ammopack is accessible from both sides, enabling the user to choose between 'normal' (see Fig.3) and 'reverse' tape. 'Normal' is indicated by a plus sign (+) on the ammopack and 'reverse' by a minus sign (–). In the European version, the leading pin is the source.

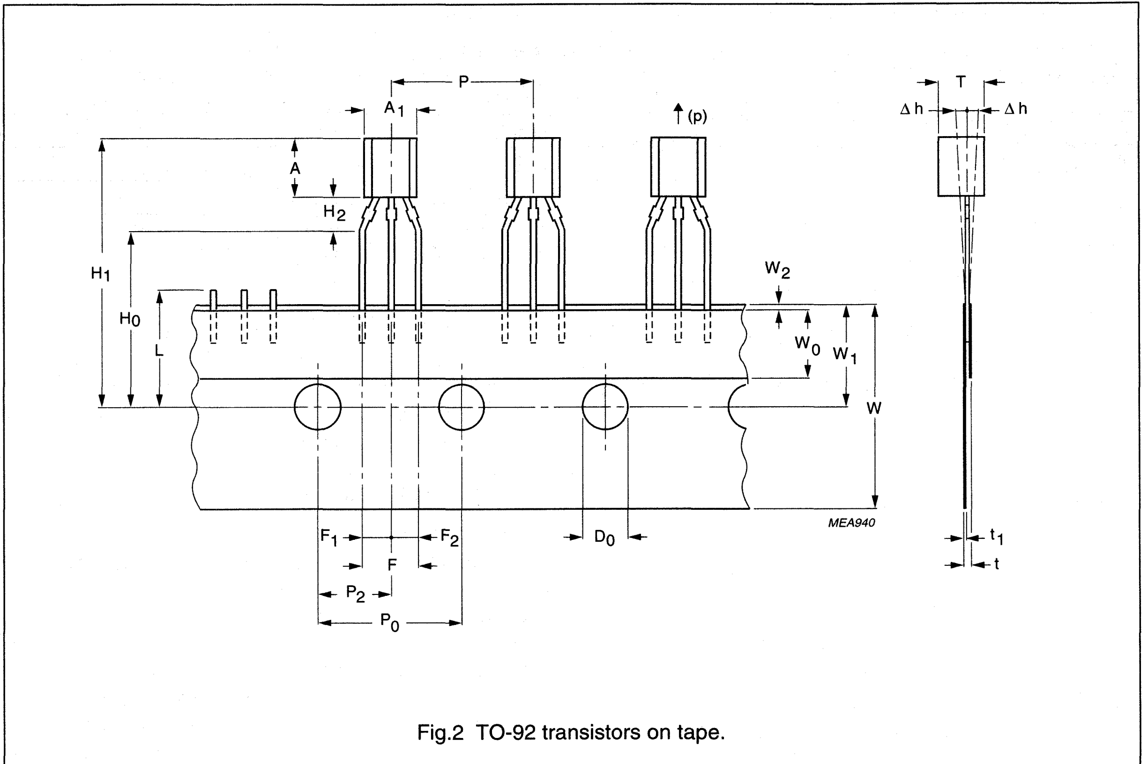


Fig.2 TO-92 transistors on tape.

Table 1 Tape specification (TO-92 leaded types)

SYMBOL	DIMENSION	SPECIFICATIONS					REMARKS
		MIN.	NOM.	MAX.	TOL.	UNIT	
A_1	body width	4	–	4.8	–	mm	
A	body height	4.8	–	5.2	–	mm	
T	body thickness	3.5	–	3.9	–	mm	
P	pitch of component	–	12.7	–	±1	mm	
P_0	feed hole pitch	–	12.7	–	±0.3	mm	
	cumulative pitch error	–	–	–	±0.1		note 1
P_2	feed hole centre to component centre	–	6.35	–	±0.4	mm	to be measured at bottom of clinch
F	distance between outer leads	–	5.08	–	+0.6/–0.2	mm	
Δh	component alignment	–	0	1	–	mm	at top of body
W	tape width	–	18	–	±0.5	mm	
W_0	hold-down tape width	–	6	–	±0.2	mm	
W_1	hole position	–	9	–	+0.7/–0.5	mm	
W_2	hold-down tape position	–	0.5	–	±0.2	mm	
H_0	lead wire clinch height	–	16.5	–	±0.5	mm	
H_1	component height	–	–	23.25	–	mm	
L	length of snipped leads	–	–	11	–	mm	
D_0	feed hole diameter	–	4	–	±0.2	mm	
t	total tape thickness	–	–	1.2	–	mm	t_1 = 0.3 to 0.6
F_1, F_2	lead-to-lead distance	–	–	–	+0.4/–0.2	mm	
H_2	clinch height	–	–	–	–	mm	
(p)	pull-out force	6	–	–	–	N	

Note

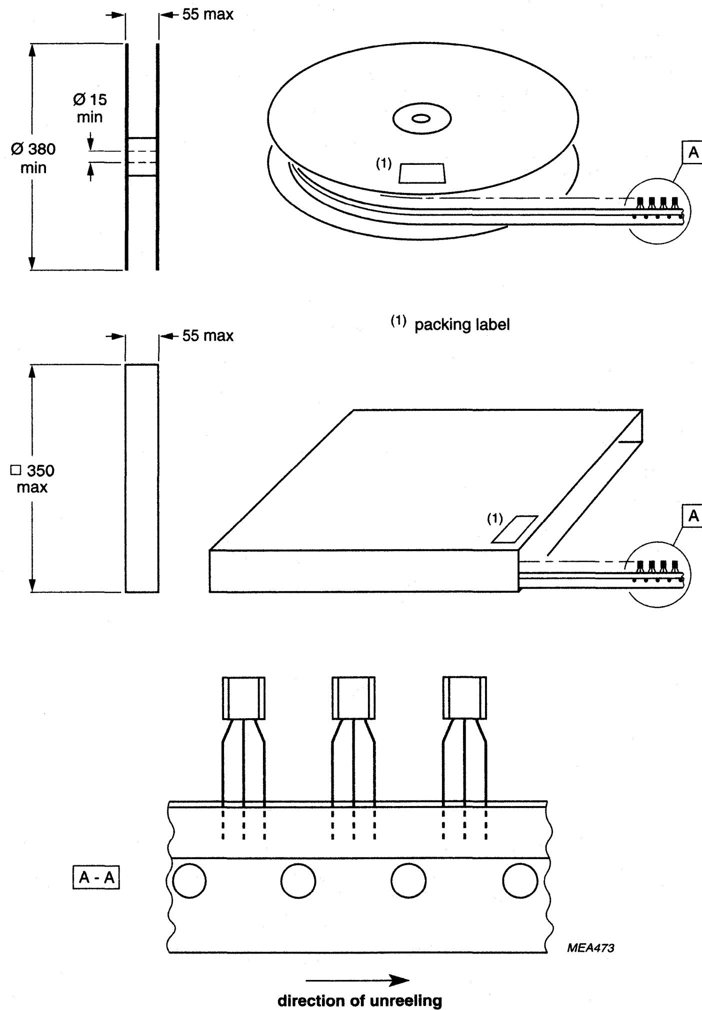
1. Measured over 20 devices.

Dropouts

A maximum of 0.5% of the specified number of transistors in each packing may be missing. Up to 3 consecutive components may be missing provided the gap is followed by 6 consecutive components.

Tape splicing

Splice the carrier tape on the back and/or front so that the feed hole pitch (P_0) is maintained (see Figs 2 and 4).



Dimensions in mm.

Fig.3 Dimensions of reel and box.

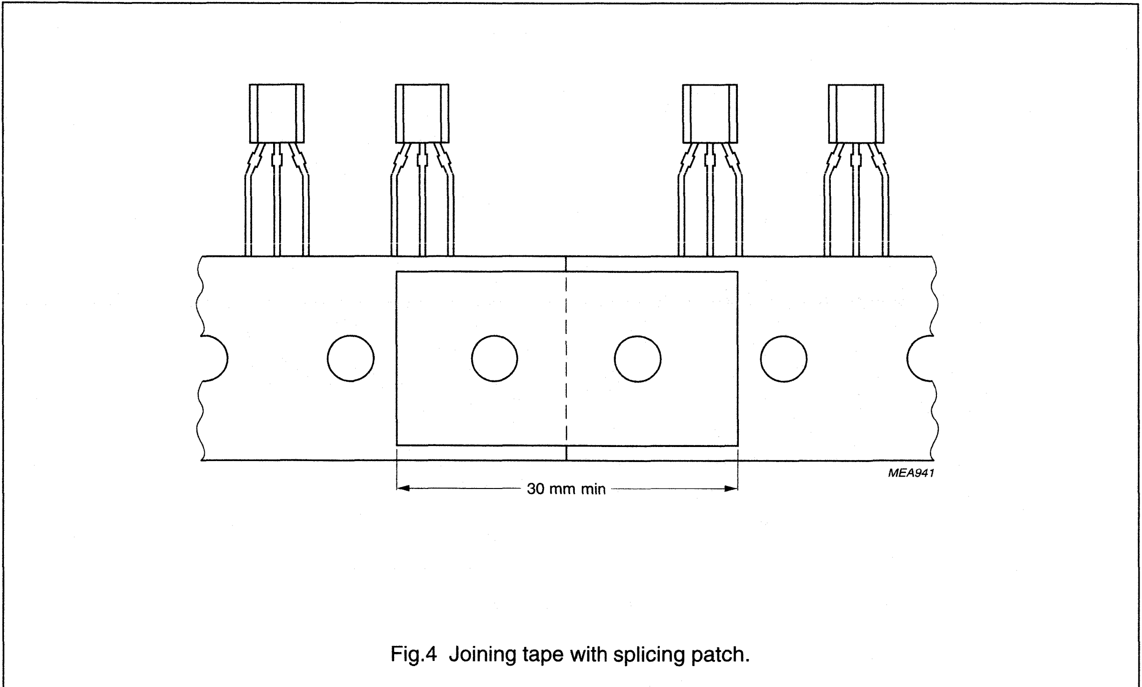
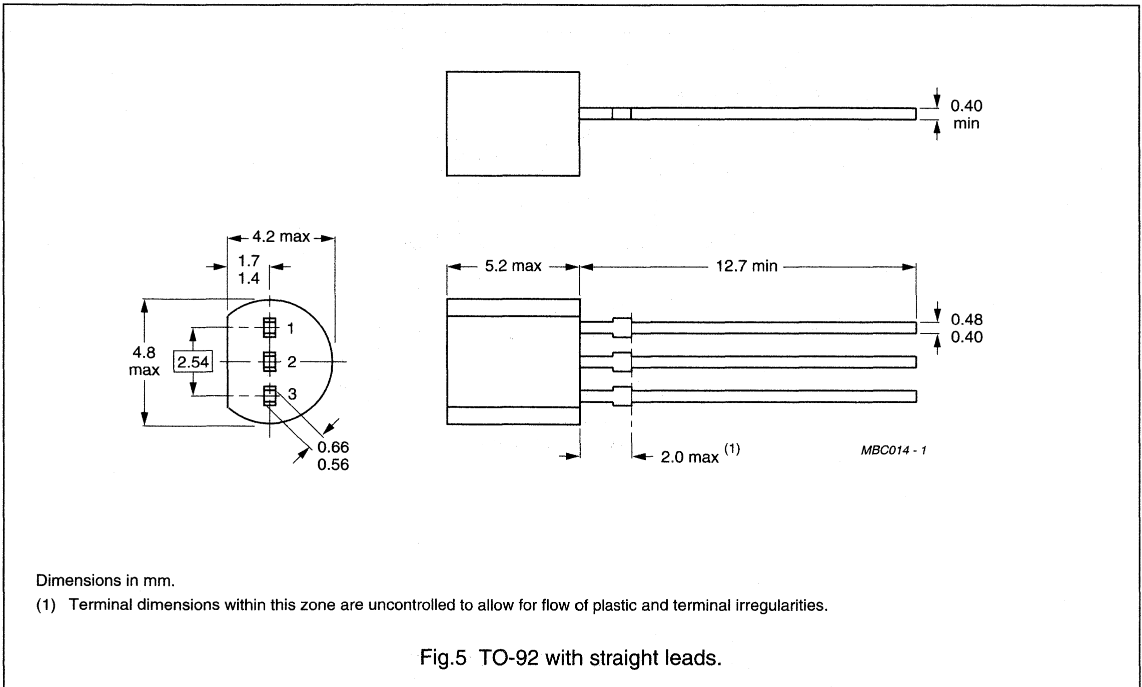


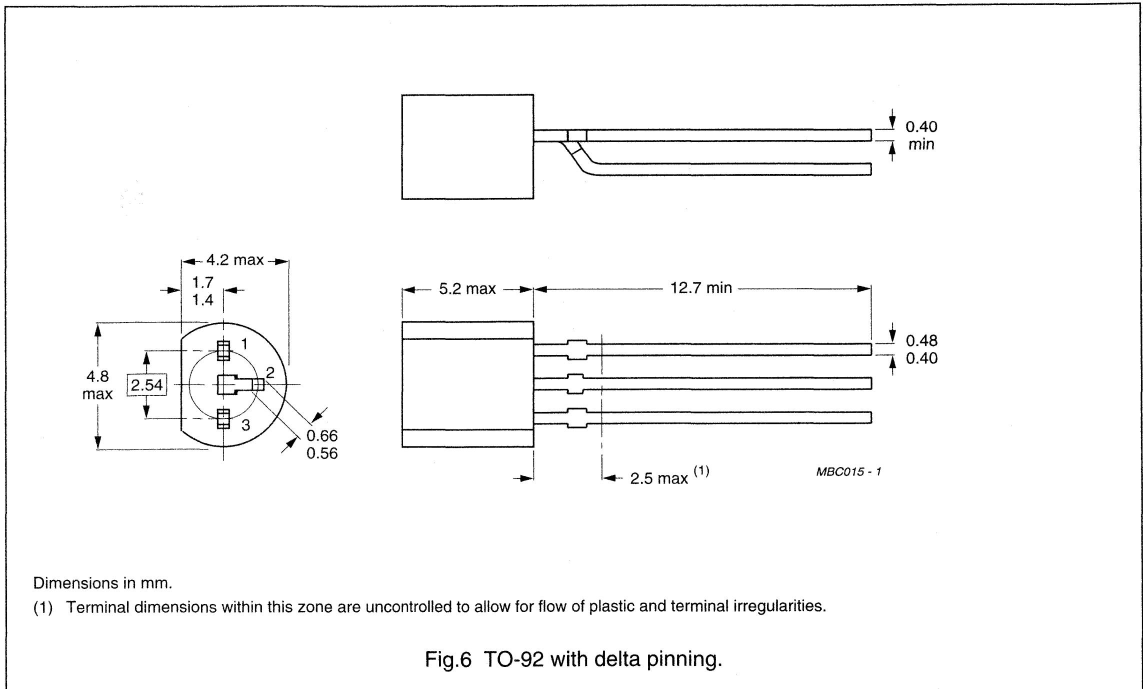
Fig.4 Joining tape with splicing patch.



Dimensions in mm.

(1) Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

Fig.5 TO-92 with straight leads.



Dimensions in mm.

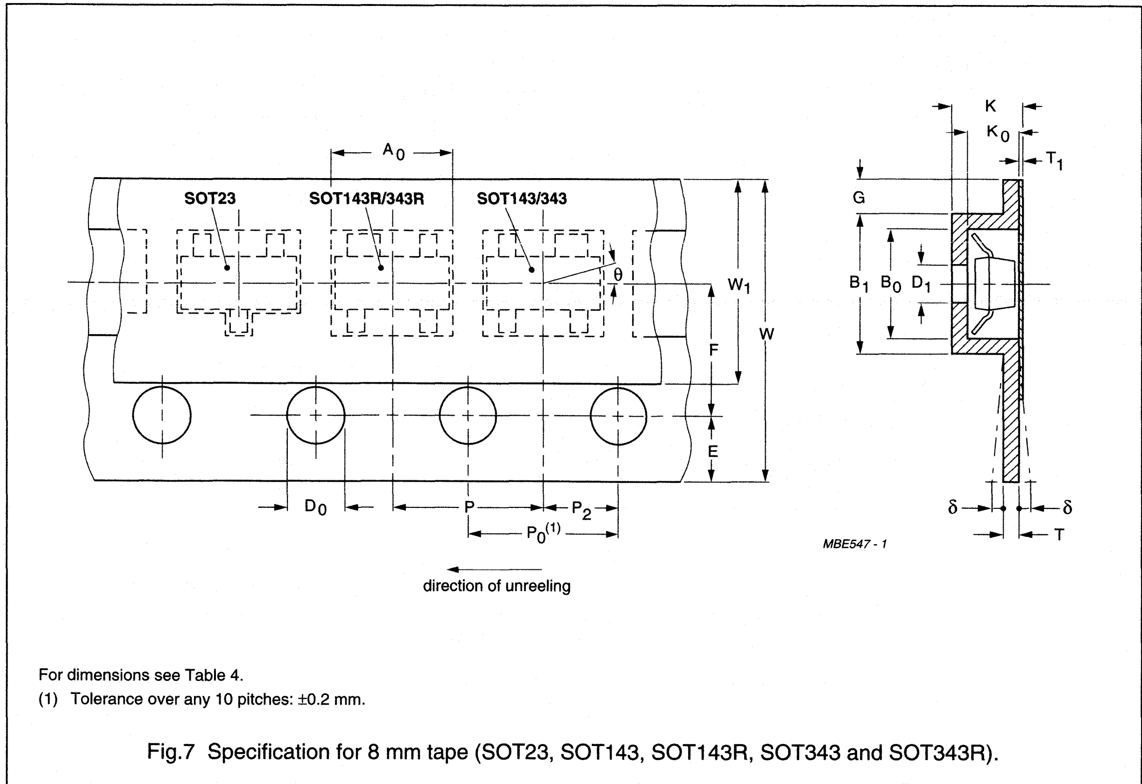
(1) Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

Fig.6 TO-92 with delta pinning.

Packing SMD types

Table 2 Packing quantities per reel (SMD types)

PACKAGE	180 mm REEL	330 mm REEL
SOT23	3000	10000
SOT143	3000	10000
SOT143R	3000	10000
SOT343	3000	10000
SOT343R	3000	10000



For dimensions see Table 4.

(1) Tolerance over any 10 pitches: ±0.2 mm.

Fig.7 Specification for 8 mm tape (SOT23, SOT143, SOT143R, SOT343 and SOT343R).

Table 3 Carrier tape widths for packages

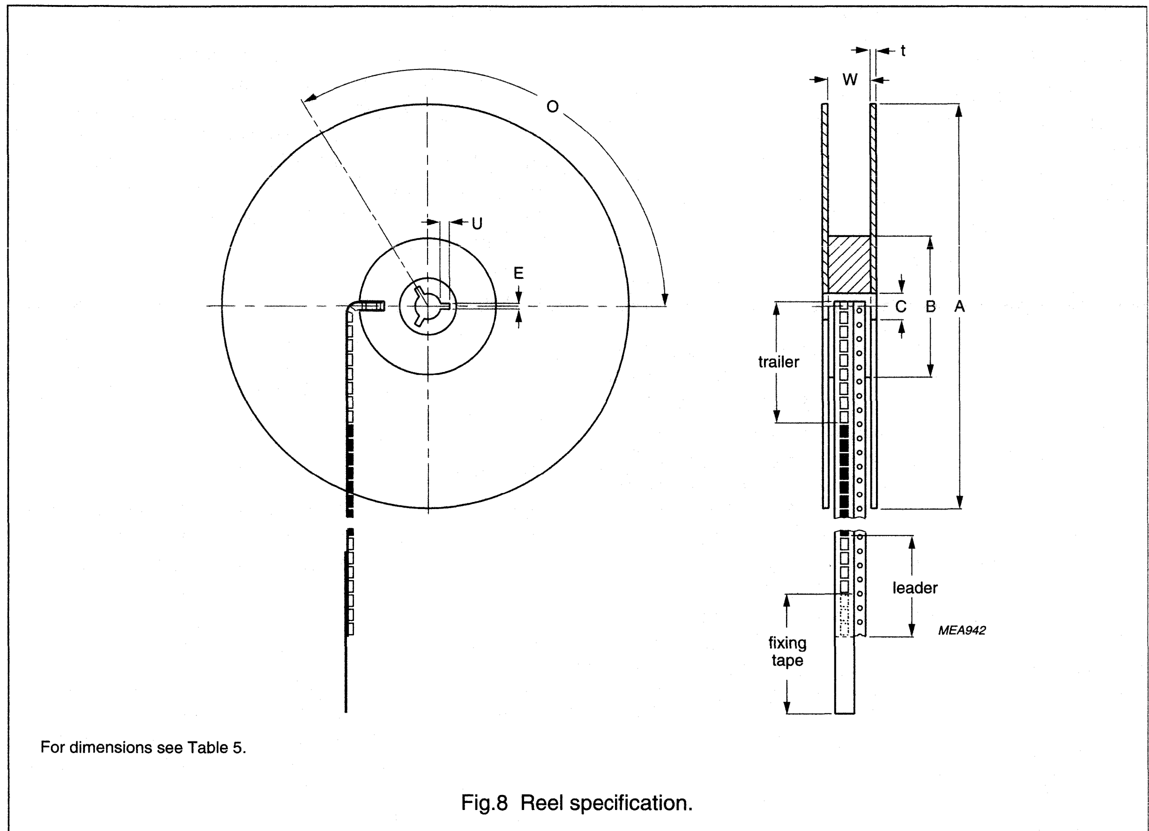
CARRIER TAPE
8 mm
SOT23
SOT143(R)
SOT343(R)

Table 4 SMD packages: tape dimensions (in mm)

DIMENSION (Figs 7 to 10)	CARRIER TAPE		TOLERANCE
	8 mm	12 mm	
Overall dimensions			
W	8.0	12.0	±0.2
K	<1.5	<2.4	–
G	>0.75	>0.75	–
Sprocket holes; note 1			
D_0	1.5	1.5	+0.1/–0
E	1.75	1.75	±0.1
P_0	4.0	4.0	±0.1
Relative placement compartment			
P_2	2.0	2.0	±0.1
F	3.5	5.5	±0.05
Compartment			
A_0	Compartment dimensions depend on package size. Maximum clearance between device and compartment is 0.3 mm; the minimum clearance ensures that the device is not totally restrained within the compartment.		
B_0			
B_1			
K_0			
D_1	>1.0	>1.5	–
P	4.0	8.0	±0.1
θ	<15°	<15°	–
Cover tape; note 2			
W_1	<5.4	<9.5	–
T_1	<0.1	<0.1	–
Carrier tape			
W	8.0	12.0	±0.2
T	<0.2	<0.2	–
δ	<0.3	<0.3	–

Notes

1. Tolerance over any 10 pitches ±0.2 mm.
2. The cover tape shall not overlap the tape or sprocket holes.



For dimensions see Table 5.

Fig.8 Reel specification.

Table 5 Reel dimensions (in mm)

DIMENSION (see Fig.8)	**8 mm TAPE**	**12 mm TAPE**	**TOLERANCE**
Flange			
A	180 [(1)] – 286 or 330	180 or 330	±0.5
t	1.5	1.5	+0.5/–0.1
W	8.4	12.4	18.0+0.2
Hub			
B	62	62	±1.5
C	12.75	12.75	+0.15/–0.2
Key slot			
E	2	2	±0.2
U	4	4	±0.5
O	120°	120°	–

Note

1. Large reel diameter depends on individual package (286 or 350).

MOUNTING AND SOLDERING

Mounting methods

There are two basic forms of electronic component construction, those with leads for through-hole mounting and microminiature types for surface mounting (SMD). Through-hole mounting gives a very rugged construction and uses well established soldering methods. Surface mounting has the advantages of high packing density plus high-speed automated assembly. Surface mounting techniques are complex and this chapter gives only a simplified overview of the subject.

Although many electronic components are available as surface mounting types, some are not and this often leads to the use of through-hole as well as surface mounting components on one substrate (a mixed print). The mix of components affects the soldering methods that can be applied. A substrate having SMDs mounted on one or both sides but no through-hole components is likely to be suitable for reflow or wave soldering. A double sided mixed print that has through-hole components and some SMDs on one side and densely packed SMDs on the other normally undergoes a sequential combination of reflow and wave soldering. When the mixed print has only through-hole components on one side and all SMDs on the other, wave soldering is usually applied.

Reflow soldering

SOLDER PASTE

Most reflow soldering techniques utilize a paste that is a mixture of flux and solder. The solder paste is applied to the substrate before the components are placed. It is of sufficient viscosity to hold the components in place and, therefore, an application of adhesive is not required. Drying of the solder paste by preheating increases the viscosity and prevents any tendency for the components to become displaced during the soldering process. Preheating also minimizes thermal shock and drives off flux solvents.

Screen printing

This is the best high-volume production method of solder paste application. An emulsion-coated, fine mesh screen with apertures etched in the emulsion to coincide with the surfaces to be soldered is placed over the substrate. A squeegee is passed across the screen to force solder paste through the apertures and on to the substrate. The layer thickness of screened solder paste is usually between 150 and 200 μm.

Stencilling

In this method a stencil with etched holes to pass the paste is used. The thickness of the stencil determines the amount of amount of solder paste that is deposited on the substrate. This method is also suited to high-volume work.

Dispensing

A computer-controlled pressure syringe dispenses small doses of paste to where it is required. This method is mainly suitable for small production runs and laboratory use.

Pin transfer

A pin picks up a droplet of solder paste from a reservoir and transfers it to the surface of the substrate or component. A multi-pin arrangement with pins positioned to match the substrate is possible and this speeds up the process time.

REFLOW TECHNIQUES

Thermal conduction

The prepared substrates are carried on a conveyor belt, first through a preheating stage and then through a soldering stage. Heat is transferred to the substrate by conduction through the belt. Figure 9 shows a theoretical time/temperature relationship for thermal conduction reflow soldering. This method is particularly suited to thick film substrates and is often combined with infrared heating.

Infrared

An infrared oven has several heating elements giving a broad spectrum of infrared radiation, normally above and below a closed loop belt system. There are separate zones for preheating, soldering and cooling. Dwell time in the soldering zone is kept as short as possible to prevent damage to components and substrate. A typical heating profile is shown in Fig.10. This reflow method is often applied in double-sided prints.

Vapour phase

A substrate is immersed in the vapours of a suitable boiling liquid. The vapours transfer latent heat of condensation to the substrate and solder reflow takes place. Temperature is controlled precisely by the boiling point of the liquid at a given pressure. Some systems employ two vapour zones, one above the other. An elevator tray, suspended from a hoist mechanism passes the substrate vertically through the first vapour zone into the secondary soldering zone and then hoists it out of the vapour to be cooled. A theoretical time/temperature relationship for this method is shown in Fig.11.

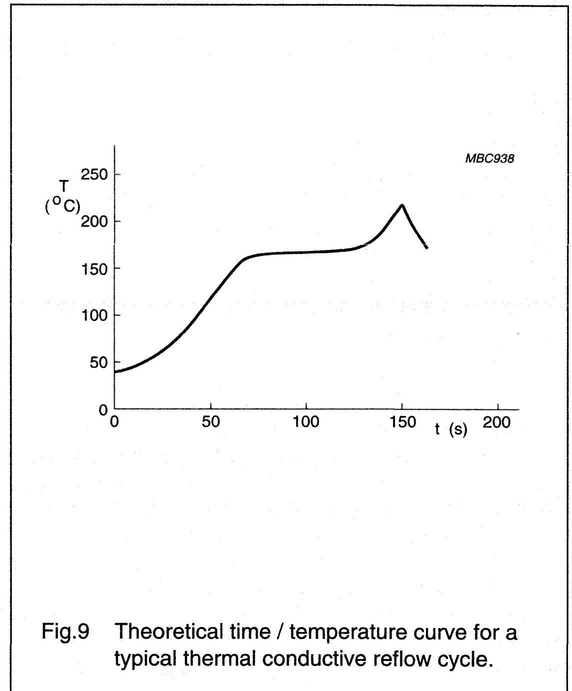


Fig.9 Theoretical time / temperature curve for a typical thermal conductive reflow cycle.

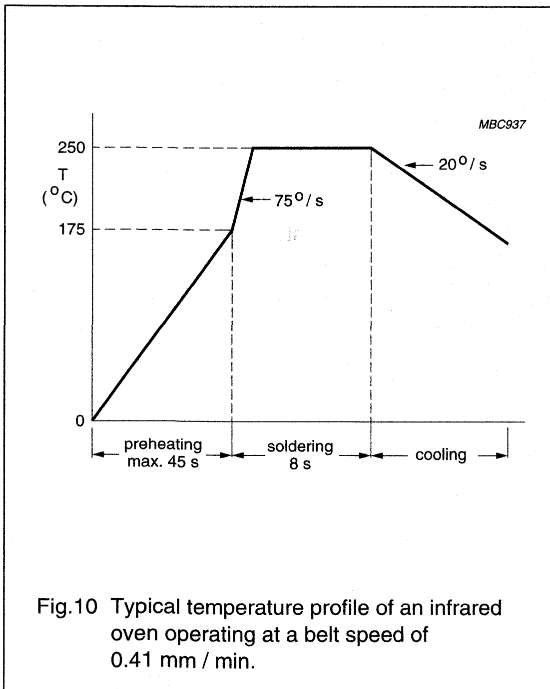


Fig.10 Typical temperature profile of an infrared oven operating at a belt speed of 0.41 mm / min.

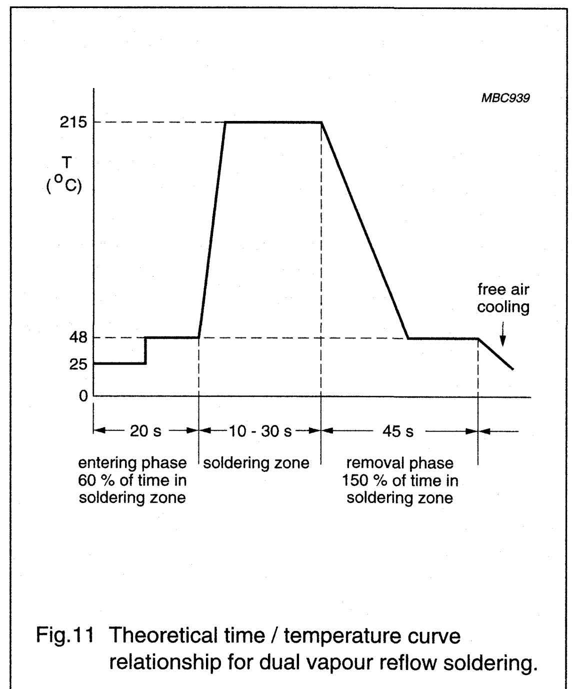


Fig.11 Theoretical time / temperature curve relationship for dual vapour reflow soldering.

Wave soldering

This soldering technique is not recommended for SOT89.

ADHESIVE APPLICATION

Since there are no connecting wires to retain them, leadless and short-leaded components are held in place with adhesive for wave soldering. A spot of adhesive is carefully placed between each SMD and the substrate. The adhesive is then heat-cured to withstand the forces of the soldering process, during which the components are fully immersed in solder. There are several methods of adhesive application.

Pin transfer method

A pin is used to transfer a droplet of adhesive from a reservoir to a precise position on the surface where it is required. The size of the droplet depends on pin diameter, depth to which the pin is dipped in the reservoir, rheology of the adhesive, and the temperature of adhesive and surrounds. The pin can be part of a pin array (bed of nails) that corresponds exactly with the required adhesive positions on the substrate. With this method, adhesive can be applied to the whole of one side of a substrate in one operation and is therefore suitable for high-volume production and can be used with pre-loaded mixed prints.

Alternatively, pins can be used to transfer adhesive to the components before they are placed on the substrate. This adds flexibility to production runs where variations in layout must be accommodated.

Screen printing method

A fine mesh screen is coated with emulsion except in the positions where the adhesive is required to pass. The screen is placed on the substrate and a squeegee passing across it forces adhesive through the uncoated parts of the screen. The amount of adhesive printed-through depends on the size of the uncoated screen areas, the thickness of the screen coating, the rheology of the adhesive and various machine parameters. With this method, the substrate must be flat and pre-loaded mixed prints cannot be accommodated.

Pressure syringe method

A computer-controlled syringe dispenses adhesive from an enclosed reservoir by means of pulses of compressed air. The adhesive dot size depends on the size of the syringe nozzle, the duration and pressure of the pulsed air and the viscosity of the adhesive. This method is most suited to low volume production. An advantage is the flexibility provided by computer programmability.

FLUXING

The quality of the soldered connections between components and substrate is critical for circuit performance and reliability. Flux promotes solderability of the connecting surfaces and is chosen for the following attributes:

- removal of surface oxides
- prevention of reoxidation
- transference of heat from source to joint area
- residue that is non-corrosive or, if residue is corrosive, should be easy to clean away after soldering
- ability to improve wettability (readiness of a metal surface to form an alloy at its interface with the solder) to ensure strong joints with low electrical resistance
- suitability for the desired method of flux application.

In wave soldering, liquified flux is usually applied as a foam, a spray or in a wave.

Foam

Flux foam is made by forcing low-pressure, water-free clean air through an aerator immersed in liquid flux. Fine bubbles of flux are directed onto the substrate/component surfaces where they burst and form a thin, even layer. The flux also penetrates any plated-through holes. The flux has to be chosen for its foaming capabilities.

Spray

Several methods of spray fluxing exist, the most common involves a mesh drum rotating in liquid flux. Air is blown into the drum which, when passing through the fine mesh, directs a spray of flux onto the underside of the substrate. The amount of flux deposited is controllable by the speed of the substrate passing through the spray, the speed of rotation of the drum and the density of the flux.

Wave

A wave fluxer creates a double flowing wave of liquid flux which adheres to the surface as the substrate passes through. Wave height control is essential and a soft wipe-off brush is usually incorporated to remove excess flux from the substrate.

PRE-HEATING

Pre-heating of the substrate and components is performed immediately before soldering. This reduces thermal shock as the substrate enters the soldering process, causes the flux to become more viscous and accelerates the chemical action of the flux and so speeds up the soldering action.

SOLDERING

Wave soldering is usually the best method to use when high throughput rates are required. The single-wave soldering principle (see Fig.12) is the most straight forward method and can be used on simple substrates with two-terminal SMD components. More complex substrates with increased circuit density and closer spacing of conductors can pose the problems of nonwetting (dry joints) and solder bridging. Bridging can occur across the closely spaced leads of multi-leaded devices as well as across adjacent leads on neighbouring components. Nonwetting is usually caused by components with plastic bodies. The plastic is not wetted by solder and creates a depression in the solder wave, which is augmented by surface tension. This can cause a shadow behind the component and prevent solder from reaching the joint surfaces. A smooth laminar solder wave is required to avoid bridging and a high pressure wave is needed to completely cover the areas that are difficult to wet. These conflicting demands are difficult to attain in a single wave but dual wave techniques go a long way in overcoming the problem.

In a dual wave machine (see Fig.13), the substrate first comes into contact with a turbulent wave which has a high vertical velocity. This ensures good solder contact with both edges of the components and prevents joints from being missed. The second smooth laminar wave completes the formation of the solder fillet, removes excess solder and prevents bridging. Figure 14 indicates the time/temperature relationship measured at the soldering site in dual wave soldering.

New methods of wave soldering are developing continually. For example, the Omega System is a single wave agitated by pulses, which combines the functions of smoothness and turbulence. In another, a lambda wave injects air bubbles in the final part of the wave. A further innovation is the hollow jet wave in which the solder wave flows in the opposite direction to the substrate.

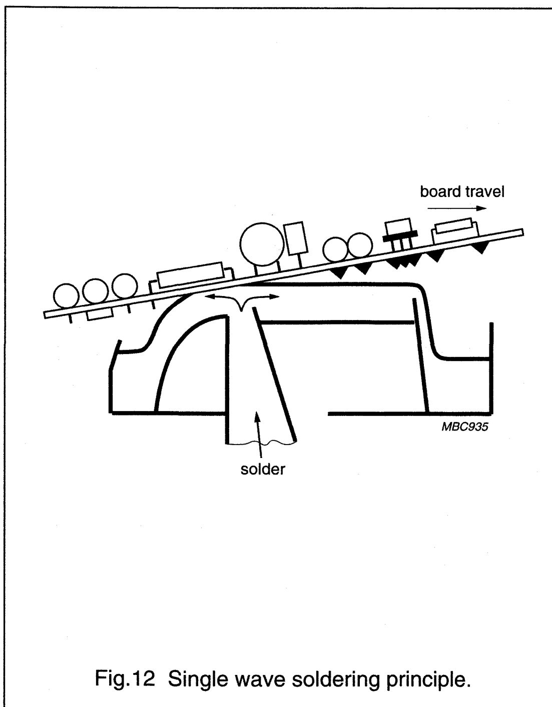


Fig.12 Single wave soldering principle.

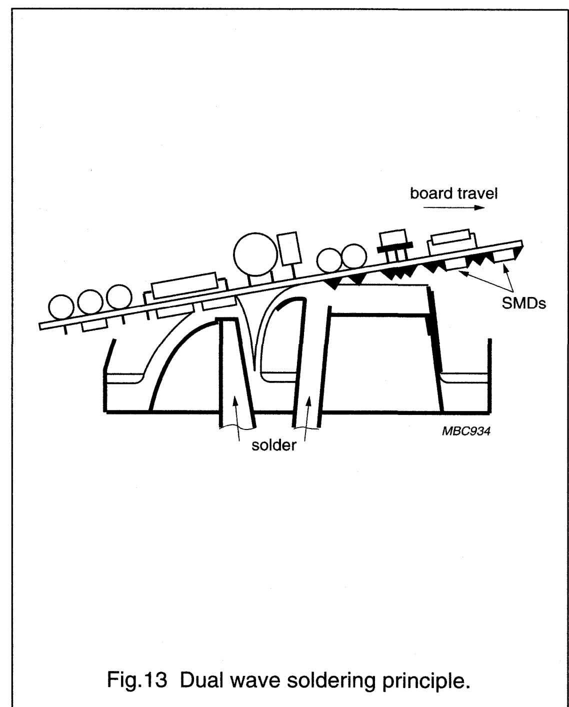


Fig.13 Dual wave soldering principle.

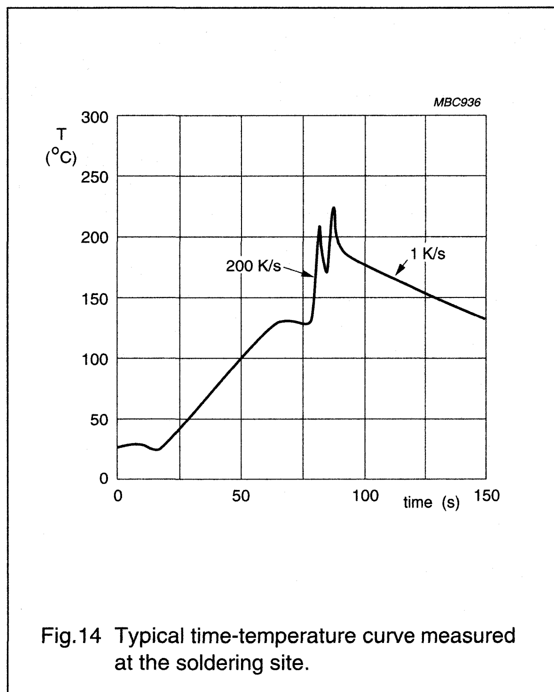


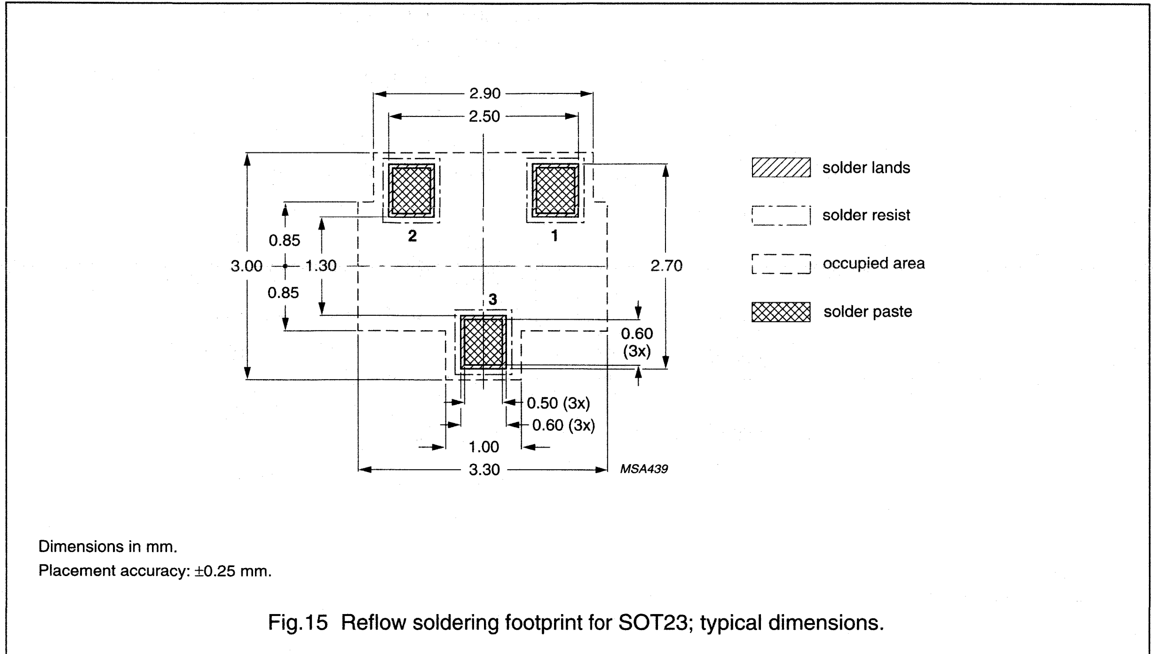
Fig.14 Typical time-temperature curve measured at the soldering site.

Footprint design

The footprint design of a component for surface mounting is influenced by many factors:

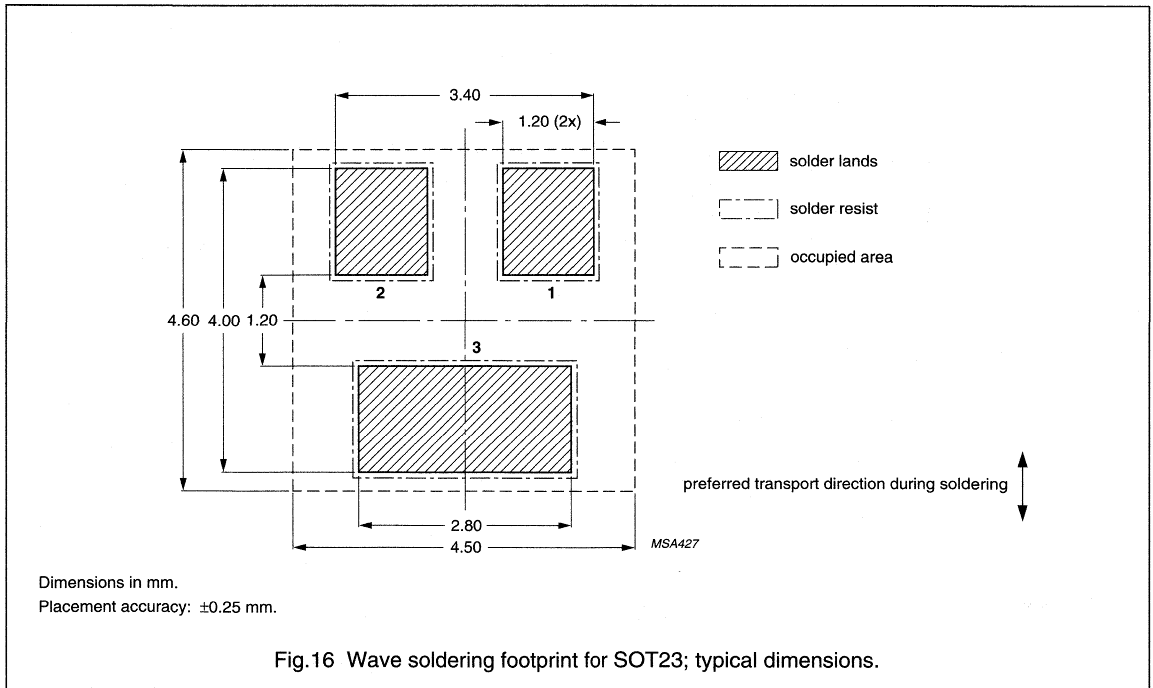
- features of the component, its dimensions and tolerances
- circuit board manufacturing processes
- desired component density
- minimum spacing between components
- circuit tracks under the component
- component orientation (if wave soldering)
- positional accuracy of solder resist to solder lands
- positional accuracy of solder paste to solder lands (if reflow soldering)
- component placement accuracy
- soldering process parameters
- solder joint reliability parameters.

SOT23 FOOTPRINTS



Dimensions in mm.
Placement accuracy: ±0.25 mm.

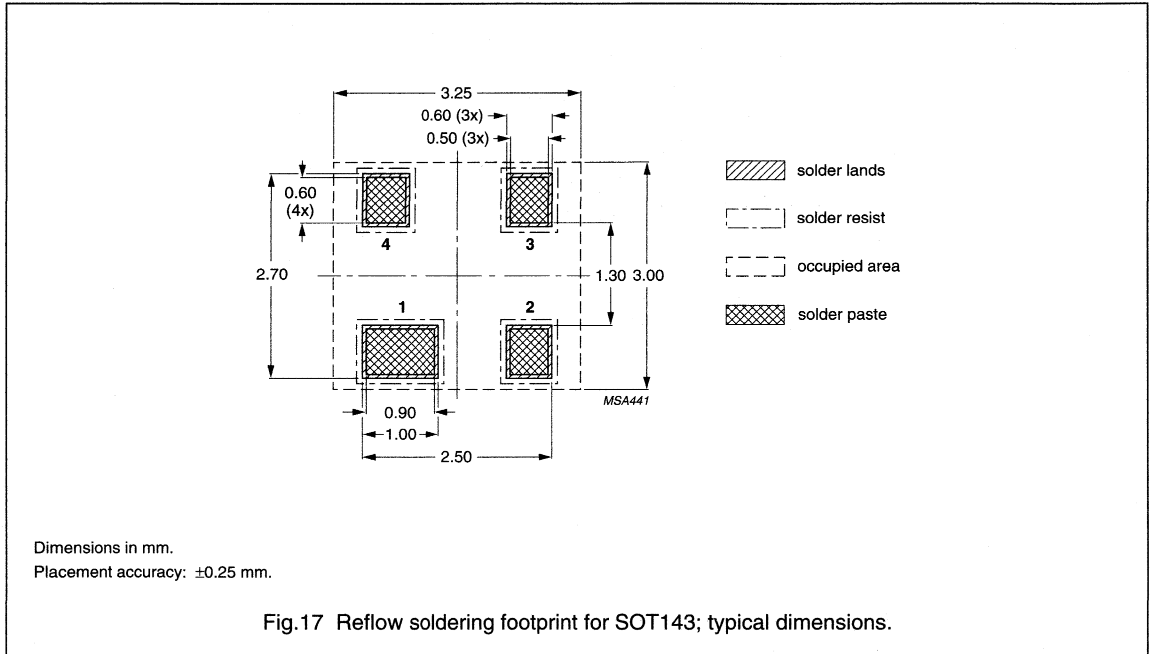
Fig.15 Reflow soldering footprint for SOT23; typical dimensions.



Dimensions in mm.
Placement accuracy: ±0.25 mm.

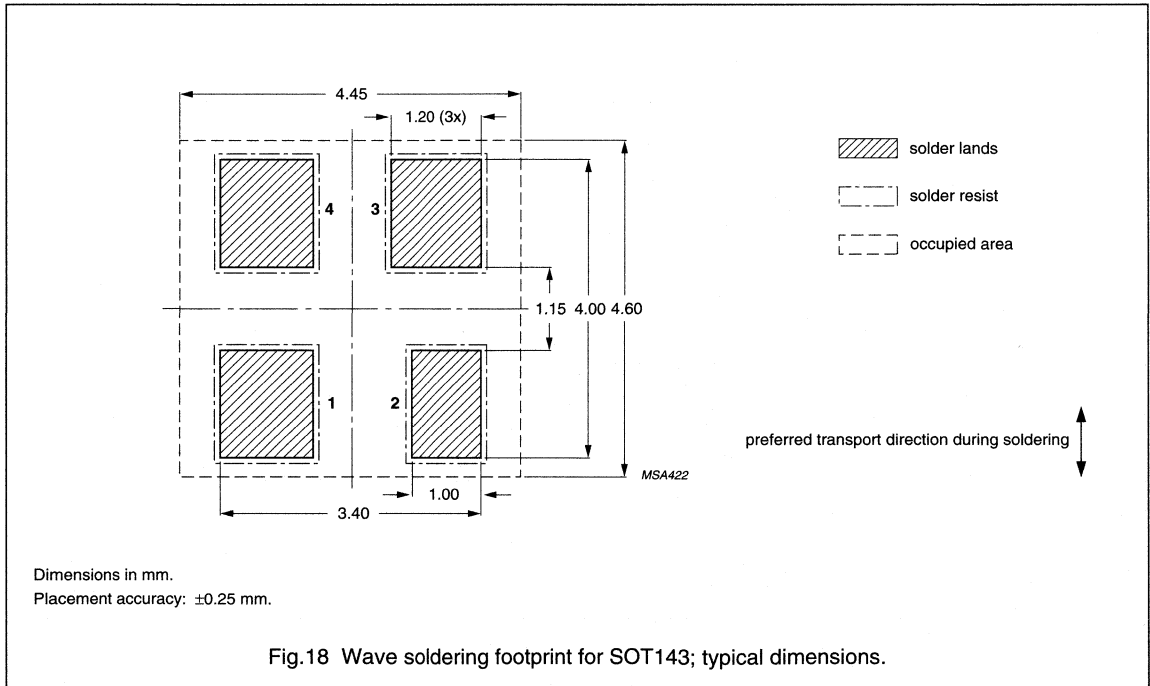
Fig.16 Wave soldering footprint for SOT23; typical dimensions.

SOT143/SOT143R FOOTPRINTS



Dimensions in mm.
Placement accuracy: ±0.25 mm.

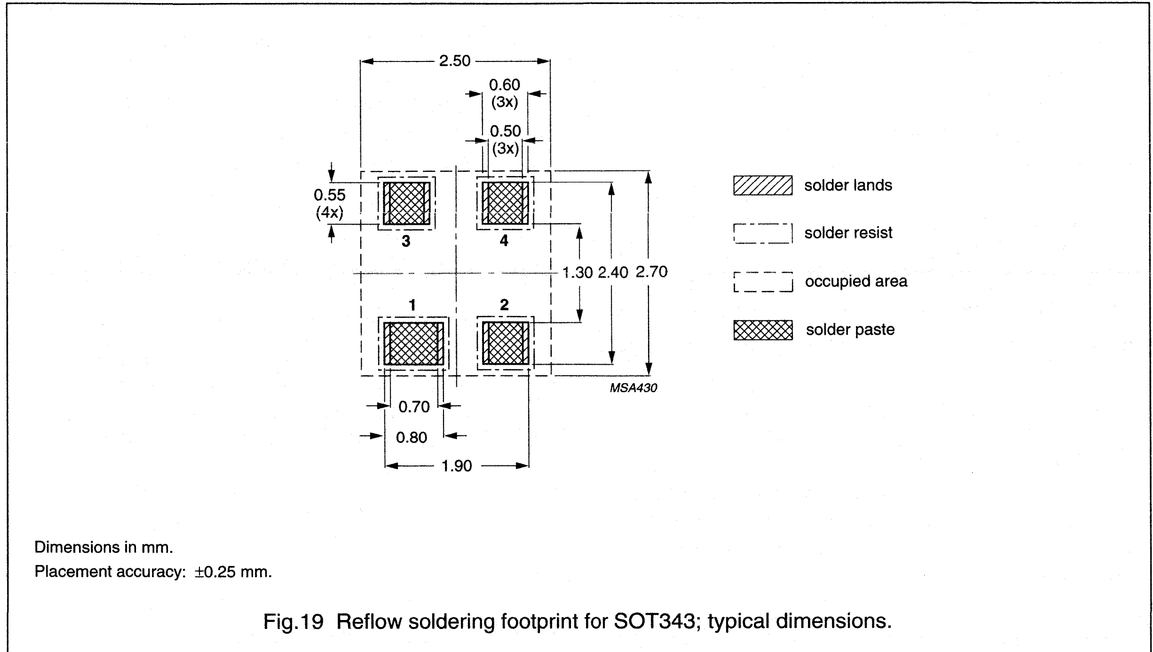
Fig.17 Reflow soldering footprint for SOT143; typical dimensions.



Dimensions in mm.
Placement accuracy: ±0.25 mm.

Fig.18 Wave soldering footprint for SOT143; typical dimensions.

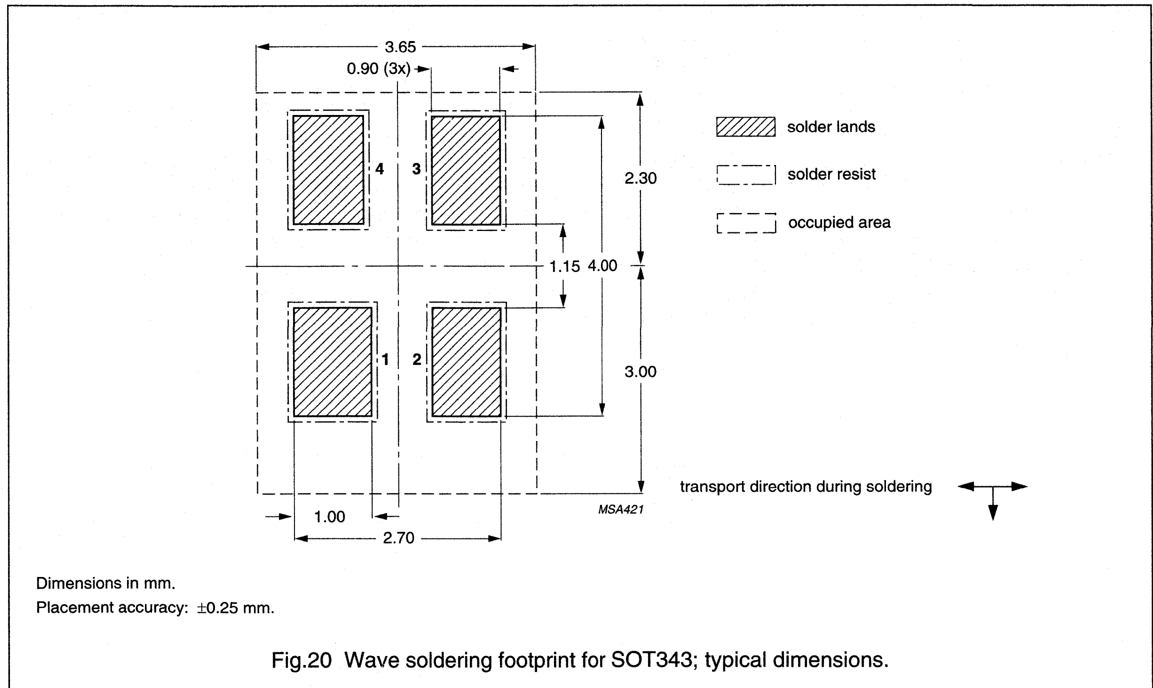
SOT343 FOOTPRINTS



Dimensions in mm.

Placement accuracy: ±0.25 mm.

Fig.19 Reflow soldering footprint for SOT343; typical dimensions.



Dimensions in mm.

Placement accuracy: ±0.25 mm.

Fig.20 Wave soldering footprint for SOT343; typical dimensions.

Hand soldering microminiature components

It is possible to solder microminiature components with a light-weight hand-held soldering iron, but this method has obvious drawbacks and should be restricted to laboratory use and/or incidental repairs on production circuits:

- hand-soldering is time-consuming and therefore expensive.
- the component cannot be positioned accurately and the connecting tags may come into contact with the substrate and damage it.
- there is a risk of breaking the substrate and internal connections in the component could be damaged.
- the component package could be damaged by the iron.

THERMAL CONSIDERATIONS

Thermal resistance

Circuit performance and long-term reliability are affected by the temperature of the transistor die. Normally, both are improved by keeping the die temperature (junction temperature) low.

Electrical power dissipated in any semiconductor device is a source of heat. This increases the temperature of the die about some reference point, normally an ambient temperature of 25 °C in still air. The size of the increase in temperature depends on the amount of power dissipated in the circuit and the net thermal resistance between the heat source and the reference point.

Devices lose most of their heat by conduction when mounted on a a printed board, a substrate or heatsink. Referring to Fig.21 (for surface mounted devices mounted on a substrate), heat conducts from its source (the junction) via the package leads and soldered connections to the substrate. Some heat radiates from the package into the surrounding air where it is dispersed by convection or by forced cooling air. Heat that radiates from the substrate is dispersed in the same way.

The elements of thermal resistance shown in Fig.22 are defined as follows:

$R_{th\ j\text{-}mb}$ thermal resistance from junction to mounting base

$R_{th\ j\text{-}c}$ thermal resistance from junction to case

$R_{th\ j\text{-}s}$ thermal resistance from junction to soldering point

$R_{th\ s\text{-}a}$ thermal resistance from soldering point to ambient

$R_{th\ c\text{-}a}$ thermal resistance from case to ambient ($R_{th\ s\text{-}a}$ and $R_{th\ c\text{-}a}$ are the same for most packages)

$R_{th\ j\text{-}a}$ thermal resistance from junction to ambient.

The temperature at the junction depends on the ability of the package and its mounting to transfer heat from the junction region to the ambient environment. The basic relationship between junction temperature and power dissipation is:

$$T_{j\ max} = T_{amb} + P_{tot\ max}(R_{th\ j\text{-}s} + R_{th\ s\text{-}a}) = T_{amb} + P_{tot\ max}(R_{th\ j\text{-}a})$$

where:

$T_{j\ max}$ is the maximum junction temperature

T_{amb} is the ambient temperature

$P_{tot\ max}$ is the maximum power handling capability of the device, including the effects of external loads when applicable.

In the expression for $T_{j\ max}$, only T_{amb} and $R_{th\ s\text{-}a}$ can be varied by the user. The package mounting technique and the flow of cooling air are factors that affect $R_{th\ s\text{-}a}$. The device power dissipation can be controlled to a limited extent but under recommended usage, the supply voltage and circuit loading dictate a fixed power maximum. The $R_{th\ j\text{-}s}$ value is essentially independent of external mounting method and cooling air; but is sensitive to the materials used in the package construction, the die bonding method and the die area, all of which are fixed.

Values of $T_{j\,max}$ and $R_{th\,j\text{-}s}$, or $R_{th\,j\text{-}c}$ or $R_{th\,j\text{-}a}$ are given in the device data sheets. For applications where the temperature of the case is stabilized by a large or temperature-controlled heatsink, the junction temperature can be calculated from

$T_j = T_{case} + P_{tot} \times R_{th\,j\text{-}c}$ or, using the soldering point definition, from $T_j = T_{solder} + P_{tot} \times R_{th\,j\text{-}s}$.

Thermal resistance ($R_{th\,s\text{-}a}$ and $R_{th\,c\text{-}a}$)

The thermal resistance from soldering point to ambient (SMDs), and that from case to ambient depends on the mounting technique, the shape and material of the tracks and substrate. Standard mounting conditions to set the maximum power ratings of the various packages are shown in Figs 23 to 37?. Each figure shows single-sided 35 µm copper-clad epoxy fibre-glass print, 1.5 mm thick, the tracks are fully solder-tinned and the shaded areas shown are copper or ceramic (Al_2O_3) 0.7 mm thick.

$R_{th\,s\text{-}a}$ for SMDs mounted on ceramic substrate

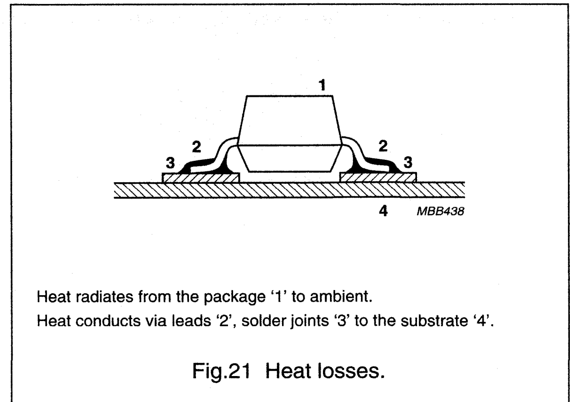
The thermal resistance $R_{th\,s\text{-}a}$ for devices in SOT23, 89, 143 and 223 packages mounted on ceramic substrate is a function of the substrate area as shown in Fig.28.

The thermal resistance $R_{th\,j\text{-}a}$ can then be calculated by:

$R_{th\,j\text{-}a}$ (substrate) = $R_{th\,j\text{-}a}$ (PCB) − $R_{th\,s\text{-}a}$ (PCB) + $R_{th\,s\text{-}a}$ (substrate)

The $R_{th\,s\text{-}a}$ (PCB) is:

SOT23 and SOT143	150 K/W
SOT89	140 K/W
SOT223	a function of pad area as shown in Fig.27.



Heat radiates from the package '1' to ambient.
Heat conducts via leads '2', solder joints '3' to the substrate '4'.

Fig.21 Heat losses.

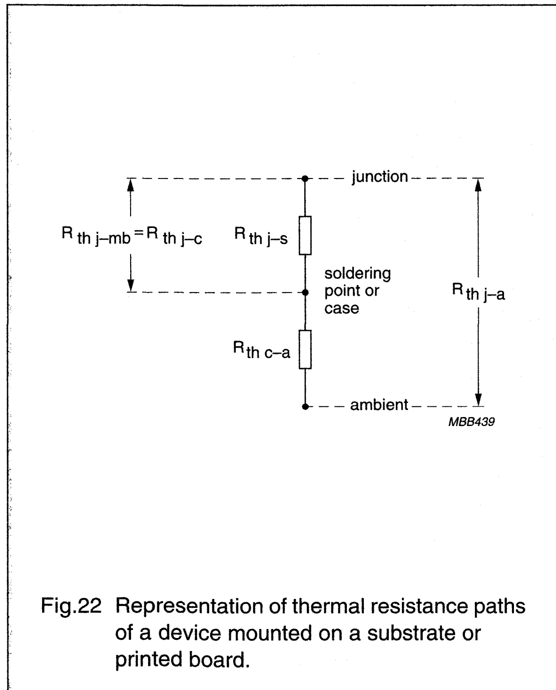
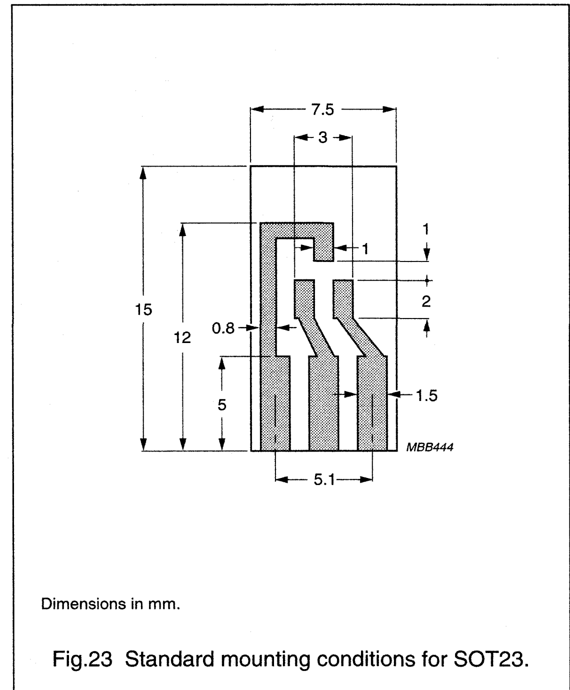
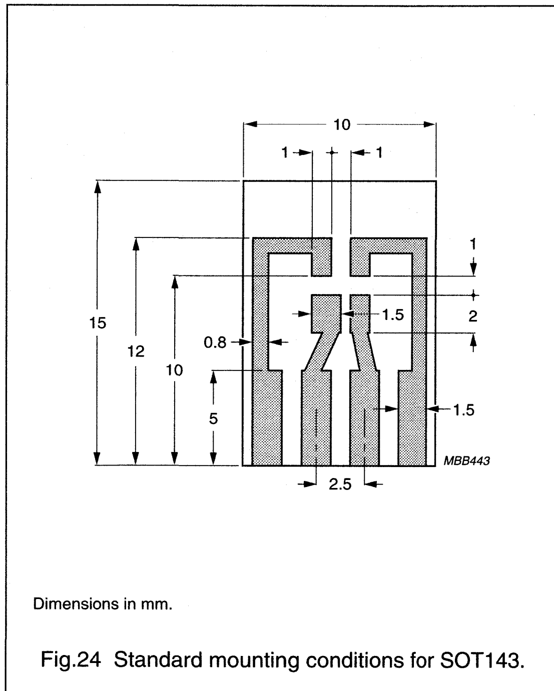


Fig.22 Representation of thermal resistance paths of a device mounted on a substrate or printed board.



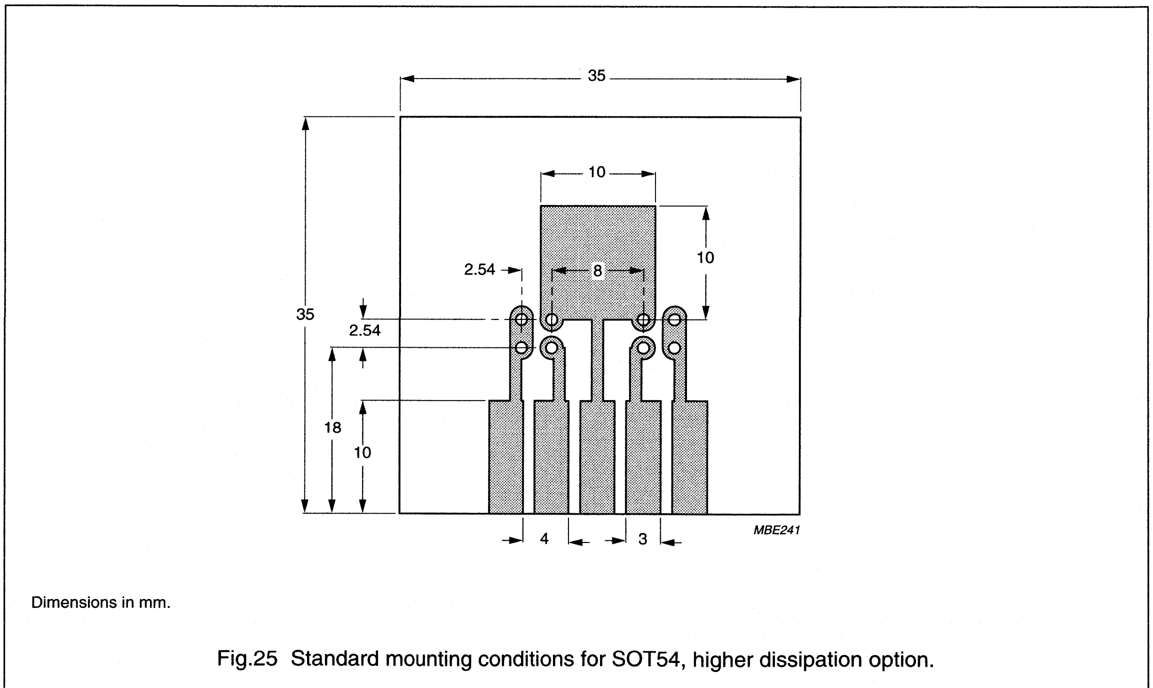
Dimensions in mm.

Fig.23 Standard mounting conditions for SOT23.



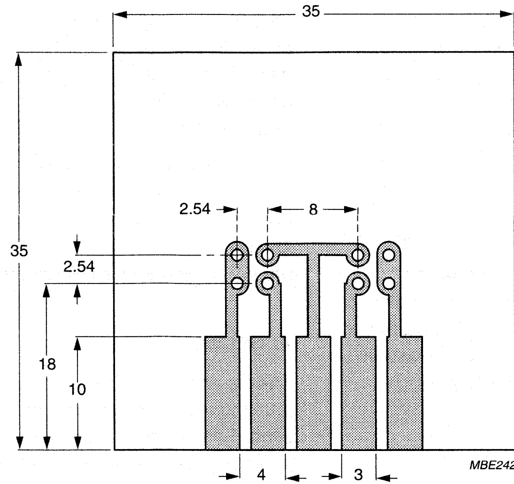
Dimensions in mm.

Fig.24 Standard mounting conditions for SOT143.



Dimensions in mm.

Fig.25 Standard mounting conditions for SOT54, higher dissipation option.



Dimensions in mm.

Fig.26 Standard mounting conditions for SOT54.

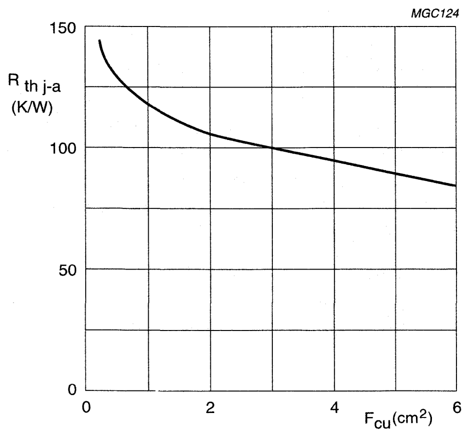


Fig.27 Thermal resistance ($R_{th\ j\text{-}a}$) as a function of FR4 epoxy fibre-glass circuit board.

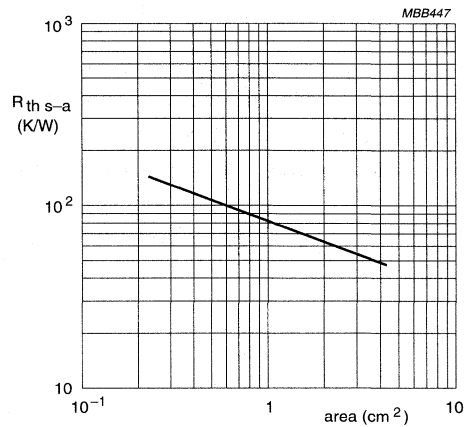


Fig.28 Thermal resistance ($R_{th\ s\text{-}a}$) as a function of area of ceramic substrate.

ELECTROSTATIC CHARGES

Electrostatic charges can exist in many things; for example, man-made-fibre clothing, moving machinery, objects with air blowing across them, plastic storage bins, sheets of paper stored in plastic envelopes, paper from electrostatic copying machines, and people. The charges are caused by friction between two surfaces, at least one of which is non-conductive. The magnitude and polarity of the charges depend on the different affinities for electrons of the two materials rubbing together, the friction force and the humidity of the surrounding air.

Electrostatic discharge is the transfer of an electrostatic charge between bodies at different potentials and occurs with direct contact or when induced by an electrostatic field. Our devices **can** be damaged if the following precautions are not taken.

WORK STATION

Figure 29 shows a working area suitable for safely handling electrostatic sensitive devices. It has a work bench, the surface of which is conductive or covered by an antistatic sheet. Typical resistivity for the bench surface is between 1 and 500 kΩ per cm^2. The floor should also be covered with antistatic material.

The following precautions should be observed:

- Persons at a work bench should be earthed via a wrist strap and a resistor.
- All mains-powered electrical equipment should be connected via an earth leakage switch.
- Equipment cases should be earthed.
- Relative humidity should be maintained between 50 and 65%.
- An ionizer should be used to neutralize objects with immobile static charges.

RECEIPT AND STORAGE

Our devices are packed for dispatch in antistatic/conductive containers, usually boxes, tubes or blister tape. The fact that the contents are sensitive to electrostatic discharge is shown by warning labels on both primary and secondary packing.

The devices should be kept in their original packing whilst in storage. If a bulk container is partially unpacked, the unpacking should be performed at a protected work station. Any devices that are stored temporarily should be packed in conductive or antistatic packing or carriers.

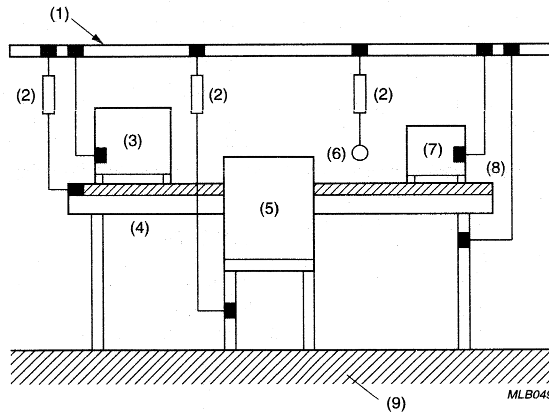
ASSEMBLY

The devices must be removed from their protective packing with earthed component pincers or short-circuit clips. Short-circuit clips must remain in place during mounting, soldering and cleansing/drying processes. Do not remove more devices from the storage packing than are needed at any one time. Production/assembly documents should state that the product contains electrostatic sensitive devices and that special precautions need to be taken.

All tools used during assembly, including soldering tools and solder baths, must be earthed. All hand tools should be of conductive or antistatic material and, where possible, should not be insulated.

Measuring and testing of completed circuit boards must be done at a protected work station. Place the soldered side of the circuit board on conductive or antistatic foam and remove the short-circuit clips. Remove the circuit board from the foam, holding the board only at the edges. Make sure the circuit board does not touch the conductive surface of the work bench. After testing, replace the circuit board on the conductive foam to await packing.

Assembled circuit boards should be handled in the same way as unmounted devices. They should also carry warning labels and be packed in conductive or antistatic packing.



(1) Earthing rail.
(2) Resistor (500 kΩ ± 10%, 0.5 W).
(3) Ionizer.
(4) Work bench.
(5) Chair.
(6) Wrist strap.
(7) Electrical equipment.
(8) Conductive surface/antistatic sheet.
(9) Antistatic floor.

Fig.29 Protected work station.

IDEAS FOR DESIGN

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MOS-FET analog switches	53

JFET CONSTANT-CURRENT SOURCES

The simplest JFET current source is shown in Fig.1. The JFET has been selected rather than a MOS-FET because it does not require gate bias (depletion mode). The current will be reasonably constant for a V_{DS} larger than several volts. However, because of I_{DSS} spread, the current is unpredictable. This can be seen, for example, with the 2N5484 which has a specified I_{DSS} of 1 to 5 mA. The circuit is attractive because of its simplicity. (Current regulator diodes are JFETs with the gate tied to the source, sorted according to current).

With a small variation this circuit gives an adjustable current source (see Fig.2). Resistor R back-biases the gate by $V = I_D \times R$, thus reducing I_D. The value of R can be calculated from the I_D/V_G characteristic for that particular JFET. This circuit makes it possible to set the current (must be less than I_{DSS}) as well as to make this current more predictable.

A JFET current source always shows some variation of output current with output voltage because of its finite output impedance, even if built with source resistor.

An improvement can be made by using a second JFET to hold the drain-source voltage of the current source constant (see Fig.3). The JFET Q2 has a larger I_{DSS} and is connected in series with the current source. It passes the (constant) drain current from Q1 through to the load, whilst holding the drain at Q1 at a fixed voltage; namely the gate-source voltage that makes Q2 operate at the same current as Q1. Q2 therefore shields Q1 from voltage swings at its output, and since Q1 is not subject to drain voltage variations, it provides constant current.

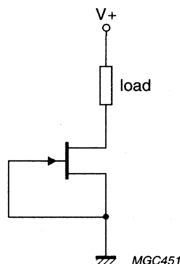

Fig.1 Simple JFET current source.

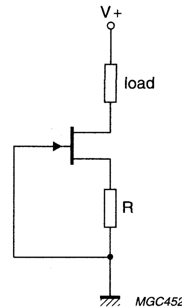

Fig.2 Adjustable JFET current source.

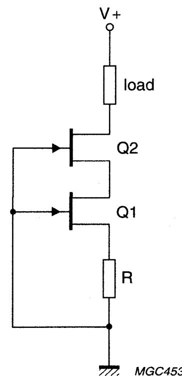

Fig.3 Adjustable JFET current source with high output impedance.

JFET SOURCE FOLLOWERS AND AMPLIFIERS

There are normally three major considerations to be taken into account when designing amplifiers: voltage gain, distortion and noise, and the importance of each of these depends on the application. This is also true for the type of circuit configuration used. There are three basic circuit configurations for JFETs:

- Common source configuration (CSC)
- Common gate configuration (CGC)
- Common drain configuration (CDC).

The choice of circuit configuration depends on the design requirements with respect to:

- Input impedance (high in CSC and CDC)
- Impedance matching to signal source and load
- Distortion (lowest in CGC).

Common-drain amplifiers, or source followers, and common-source amplifiers are analogous to emitter followers and common-emitter amplifiers in bipolar transistors. However, the absence of DC gate current makes it possible to realize very high input impedances. Such amplifiers are essential when dealing with the high-impedance signal sources encountered in measurement and instrumentation.

It is convenient to use a self-biasing scheme with a single gate-biasing resistor to ground.

Figure 4 shows a source follower, Fig.5 a common- source amplifier. The gate-biasing resistor can be quite large (at least 1 MΩ), because the gate leakage current is in the order of nA.

Matched FETs can be used to construct high input impedance front-end stages for bipolar differential amplifiers, op-amps and comparators.

There are many applications in which the signal source impedance is intrinsically high, e.g. capacitor microphones, pH probes, charged particle detectors, or microelectrode signals in biology and medicine. In these cases a FET input stage is ideal.

Within some circuits there are situations where the following stage must draw little or no current. Common examples are analog 'sample and hold' and 'peak detector' circuits, in which the level is stored in a capacitor and will 'droop' if the next amplifier draws significant input current. In all these applications the negligible input current of a FET is an important feature.

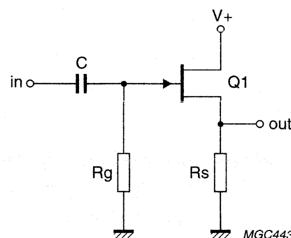

Fig.4 JFET source follower circuit.

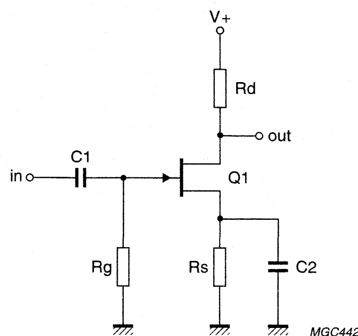

Fig.5 Common-source amplifier circuit.

JFET VOLTAGE CONTROLLED RESISTORS

Under certain biasing conditions, the on-resistance of the JFET is a function of the gate source voltage alone, so that the JFET will behave as an almost pure ohmic resistor.

Figure 6 shows the output characteristics of a PMBF4416 for relatively small positive and negative values of V_{DS} in the linear or triode region, where $V_{DS} < V_{GS} - V_{GSth}$. It can be seen that all characteristics pass through the origin (no offset) and are symmetrical and relatively linear. This means that the JFET can be used as a variable resistance in voltage controlled attenuators, analog multipliers, amplitude modulators, bandwidth controlled filters, automatic gain control circuits, and so on.

The channel resistance in the linear region is the inverse of the transconductance in the saturated region:
$R_{DS} = 1/g_m$ at a given V_{GS}.

In the first quadrant, the boundaries are set by $V_{GS} = 0$ and $V_{GD} = -V_{GSth}$, in the third quadrant by $V_{GS} = -V_{GSth}$ and $V_{GD} = 0$.

In the first quadrant, as V_{DS} increases towards $V_{DSsat} = V_{GS} - V_{GSth}$, the value of R_{DSon} changes, causing distortion in voltage-controlled-resistor circuits. The same thing happens in the third quadrant, as the negative drain voltage exceeds the negative gate voltage and causes the gate-channel diode to start conducting.

This signal distortion must be as low as possible, while at the same time a large signal handling capability is desirable. The linearity can be improved by means of feedback from the drain to the gate (see Fig.7).

Now, part of the drain signal is applied to the gate. In the case of a positive V_{DS} signal, this reduces the gate voltage, increasing the drain current and pushing the bias line into the more linear part of the operating region.

When V_{DS} is negative, V_{GS} will go more negative, causing a reduction in drain current. This reduces the conduction of the gate channel diode, resulting in a more linear bias line.

The value of R1 and R2 should be equal, to maintain symmetry between the first and third quadrants.

Feedback is essential for a reasonably linear characteristic, and high values of I_{DSS} and V_{GSth} are preferred.

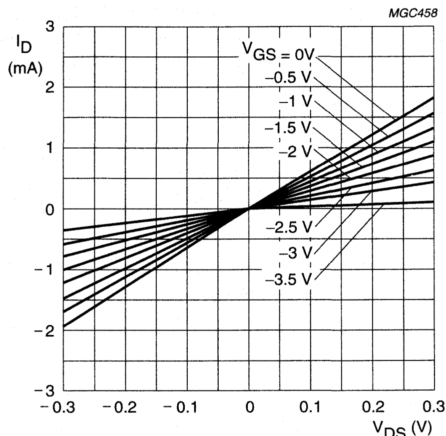

Fig.6 Output characteristics; PMBF4416.

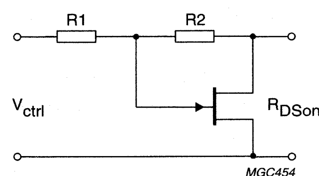

Fig.7 JFET voltage controlled resistor.

MOS-FET ANALOG SWITCHES

The combination of low on-resistance, extremely high off-resistance, low leakage current and low capacitance, makes FETs, particularly lateral MOS-FETs, ideal as voltage-controlled switching elements for analog signals.

Like mechanical switches, the FET switch is a bi-directional device; signals can go either way through it.

The circuit as shown in Fig.8 will switch signals in the −10 to +10 V range if the gate has been driven from −15 V (off) to +15 V (on); the body (back-gate) should then be tied to −15 V.

With any FET switch it is important to provide a load resistance in the 1 to 100 kΩ range in order to reduce capacitive feed-through of the input signal, that would otherwise occur during the off-state. If it is necessary to switch signals that may nearly reach the supply voltages, the simple N-channel switch shown in Fig.8 will not work, since the gate is not forward biased at the peak of the signal swing.

The solution is to use paralleled complementary MOS-FET switches (Fig.9). In this case the gate-drive is somewhat more complicated, since the N-channel FET needs to be positive biased with respect to the back-gate and the P-channel negative biased. This switch is also bidirectional; either terminal can be the input.

A useful application of FET analog switches is the ‘multiplexer’, a circuit that allows you to select any of several inputs, as specified by a control signal. The analog signal present on the selected input will be passed through to the output.

Because analog switches are bidirectional, an analog multiplexer is also a ‘demultiplexer’; a signal can be fed into the output and will appear on the selected input.

Voltage-controlled analog switches form essential building blocks for op-amps, integrators, sample-and-hold circuits and peak detectors.

Another application is in switchable RC low-pass filters. A multiplexer is used to select one out of a series of resistors, or independent switches are used to select one or more resistors in parallel.

As stated before, a load resistor is necessary to reduce capacitive feed-through (cross-talk).

If a switch that has really low cross-talk performance is needed, the circuit shown in Fig.10 could be used. When switches Q1 and Q2 are off, Q3 is on and will prevent any capacitive feed-through.

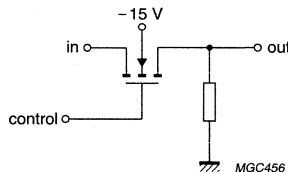

Fig.8 MOS-FET analog switch.

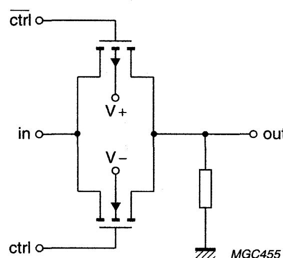

Fig.9 Paralleled complementary MOS-FET switches.

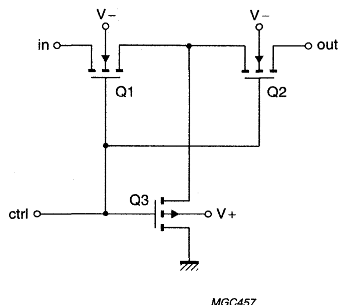

Fig.10 MOS-FET analog switch with low cross talk performance.

APPLICATION INFORMATION

Application of Philips Dual-gate MOSFETs

Philips Semiconductors B.V.

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Date : 7 - Oct. - 1997
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APPLICATION OF PHILIPS DUAL-GATE MOSFETS

1. INTRODUCTION

In Philips we have different types of Dual Gate Mosfets.
Our preferred types for use in T.V. tuners are:

the 12V types: BF998, BF908,BF1100, (SOT143)
BF998R, BF908R,BF1100R, (SOT143R)
BF998WR, BF908WR,BF1100WR, (SOT343R)

the 9V types: BF1100, BF1109, (SOT143)
BF1100R, BF1109R, (SOT143R)
BF1100WR, BF1109WR, (SOT343R)

and also for 9V the: BF998, BF998R, BF998WR,
BF908, BF908R and BF908WR
with somewhat worse performance compared to the 12V application.

and the 5V types: BF904, BF909, BF1105 (SOT143)
BF904R, BF909R, BF1105R (SOT143R)
BF904WR, BF909WR, BF1105WR (SOT343R).

The types BF998((W)R) and BF908((W)R) have no integrated bias.
The types BF904((W)R), BF909((W)R) and BF1100((W)R), have partly integrated bias and
the types BF1105((W)R), and BF1109((W)R), have fully integrated bias.
As a consequence the external bias circuits of the different Mosfets are different.
The BF998((W)R) and the BF904((W)R) are Mosfets with relatively low transferconductance ($Y_{fs\ typ}$: 24 - 25 mS) and capacitances ($C_{is\ typ}$: 2.1 - 2.2 pF).
The BF908((W)R) and the BF909((W)R) are Mosfets with relatively high transferconductance ($Y_{fs\ typ}$: 43 mS) and capacitances ($C_{is\ typ}$: 3.1 - 3.6 pF).
The BF1100((W)R), BF1105((W)R) and the BF1109((W)R) are Mosfets with a transferconductance between the above mentioned values ($Y_{fs\ typ}$: 28 - 31 mS) and still with low capacitances ($C_{is\ typ}$: 2.2 pF).
The Mosfets were developed with different transferconductances to optimize them for different frequency ranges.

2. GENERAL

In the introduction all the typenumbers and the different packages are mentioned.
The package has no influence on the d.c. biasing.
The influence of the package on the RF parameters (in the frequency area of T.V. tuners) is very small. Therefore in this report the application differences and examples will be given for the devices in the SOT143 package. This application information is also valid for the Mosfets in SOT143R and SOT343R

3. DC BIAS CIRCUITS

DC bias circuits for Mosfets without integrated bias.

We have two types of Mosfets without integrated bias, BF908 and BF998.
These Mosfets are depletion types. Depletion type Mosfets have negative pinch-off voltages.
In TV tuners AGC is necessary. For TV tuners no negative AGC voltages are available. Due to this it is necessary to lift up the Source voltage. Otherwise it is not possible to obtain maximum possible gain reduction. This lift up must be done with two resistors in the Source. For a.c. these resistors must be decoupled with a capacitor.
The nominal current of the BF998 is 10mA and that of the BF908 is 15mA.
This biasing is done with a voltage divider at Gate1.
Because there is no Gate1 current in the Mosfets the values of the resistors of the Gate1 voltage divider need to only relatively high ohmic.
The parallel connection of the 2 resistors must be higher than 10kΩ
The d.c circuit for biasing the Mosfets without integrated bias is than as given in Fig. 1 below.

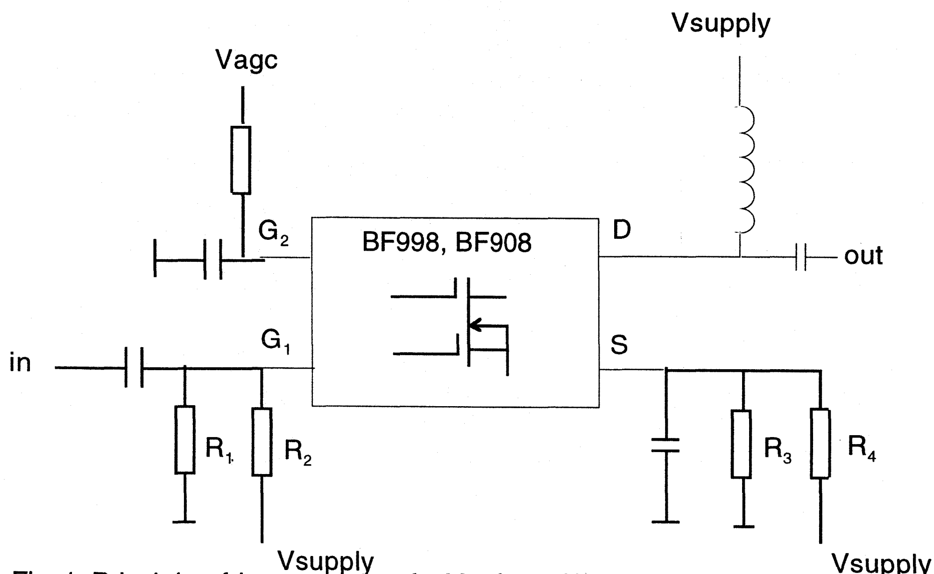


Fig. 1: Principle of the [illegible]t for Mosfets without integrated bias.

As stated in the introduction the BF998 and BF908 are for 12V tuners. However, they can be applied at 9V with some loss of performance.For the 12V and 9V application the values of the resistors R_1, R_2, R_3 and R_4 can be calculated.
At 12V application we assume that the nominal AGC voltage is 9V. In the 9V application the nominal AGC voltage is 7.5V.
The nominal V_{G2-S} in the 12V - as well as in the 9V application is 4V.

In table 1, below, the values of the resistors for the 12V- and 9V applications of the BF998 and BF908 are given.

Table 1: Resistors in the bias circuit for Mosfets without integrated bias.

	V_{supply}	$V_{agc\ nom}$	$V_{G2\text{-}S\ nom}$	$I_{D\ nom}$	R_1 / R_2	R_3 (Ω)	R_4 (Ω)
BF998	12 V	9 V	4 V	10 mA	5 / 7	360	1800
BF998	9 V	7.5 V	4.V	10 mA	7 / 11	240	1200
BF908	12 V	9V	4 V	15 mA	5 / 7	240	1200
BF908	9 V	7.5 V	4 V	15 mA	7 / 11	160	750

DC bias circuit of Mosfets with partly integrated bias.
We have three types of Mosfets with partly integrated bias. The 5V types BF904 and BF909 and the 9V to 12V type BF1100.
These Mosfets are enhancement types. This means that the pinch-off voltages are positive. So, no negative voltages are needed for fully switching-off the Mosfets.
Due to this it is not necessary to lift up the Source voltage.
For application of these types the nominal Gate2 voltage is to be set to 4V.
In 12V applications the nominal AGV voltage is 9V. In a 9V application 7.5V.
For these applications a voltage divider at Gate2 is needed. Because there is no Gate2 current, no special requirements for this divider are necessary.
We propose to set the nominal current of the BF904 and BF1100 to 10mA and that of the BF909 to 15mA.
This biasing is done with a resistor (R_{GG}) at Gate1.
The d.c circuit for biasing the Mosfets with partly integrated bias is than as given in Fig. 2 (next page).
The necessary resistors for the different applications are given in table 2 (next page).

Application of Philips Dual-gate MOSFETs

Note:

Although the BF904 and BF909 are especially developed for 5V application, these Mosfets can also be applied at lower supply voltages, down to appr. 3V. The nominal AGC voltage must be always at least 0.5V lower than the supply voltage.
The bias current can than be set by changing the resistor R_{GG} to the wanted value. The d.c. stabilization is than somewhat worse compared to the 5V application. Therefore we propose not to go lower than a Drain current of 5mA.
The BF1100 cannot be applied at supply voltages lower than 9V. Also for this Mosfet the bias current can be set to other than the recommended bias current.
In the graphs 1,2 and 3 the bias current as a function of the supply voltage and the Gate1 resistor R_{GG} are given for the BF904, BF909 and BF1100 respectively.

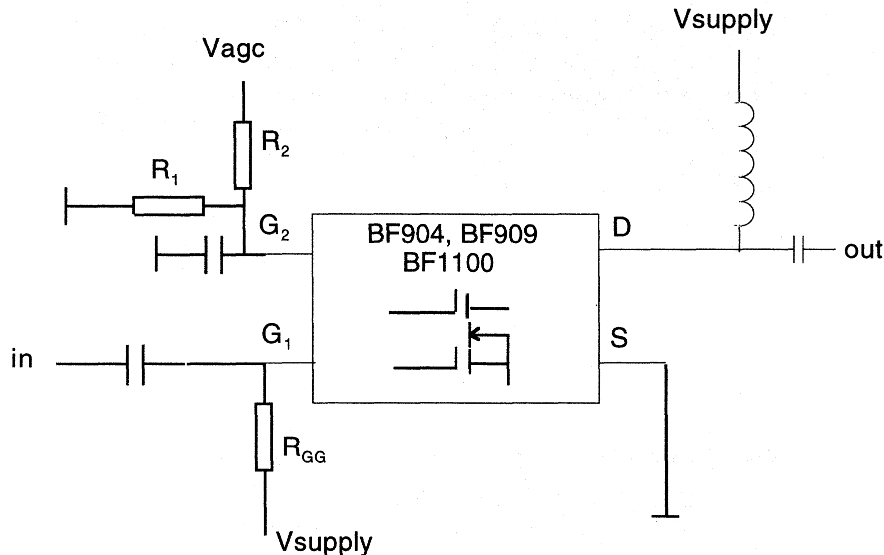
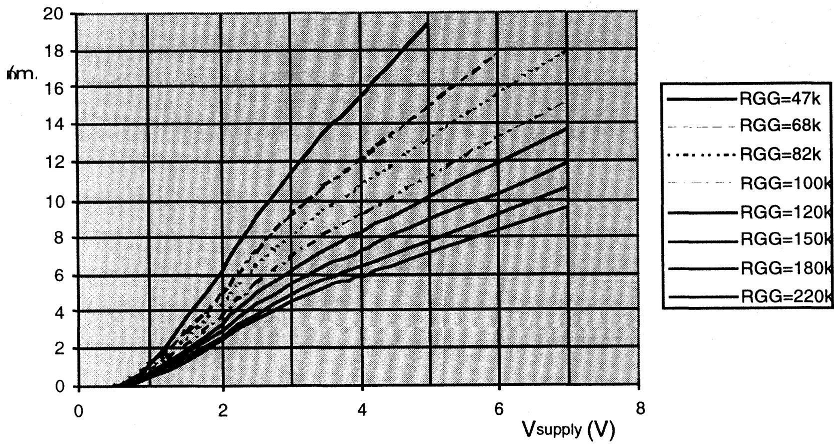


Fig. 2: Principle of the bias circuit for Mosfets with partly integrated bias.

Table 2: Resistors in the bias circuit for Mosfets with partly integrated bias.

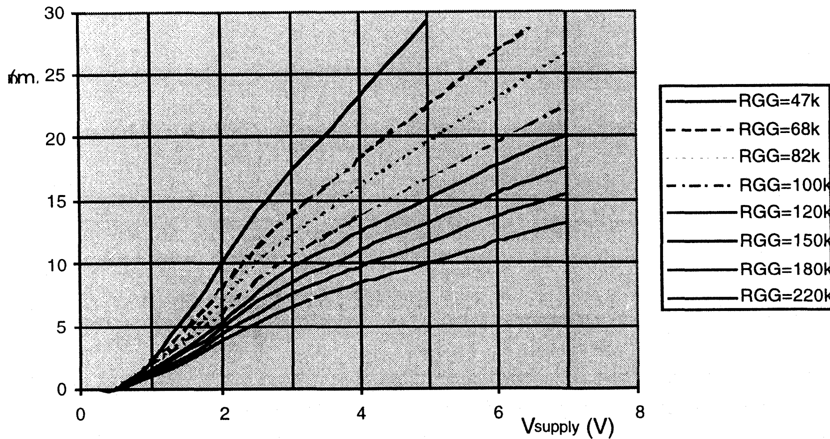
	Application	R_{GG}	R_1 / R_2
BF904	5V	120kΩ	no R_1
BF909	5V	120kΩ	no R_1
BF1100	9V 12V	180kΩ 250kΩ	8 / 7 4 / 5

BF904: Bias current as a function of suppl voltage and Gate1 resistor



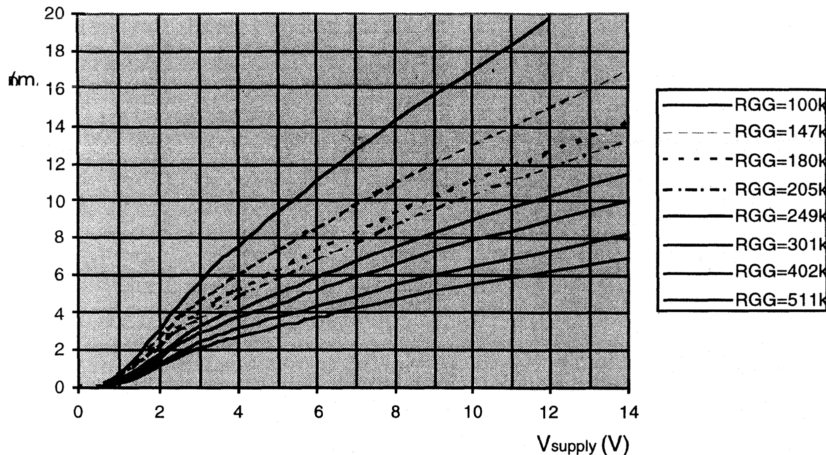
Graph. 1

BF909: Drain current as a function of suppl voltage and Gate1 resistor



Graph 2.

Application of Philips Dual-gate MOSFETs



Graph 3.

<u>DC bias circuit of Mosfets with fully integrated bias.</u>

We have two types of Mosfets with fully integrated bias. The 5V type BF1105 and the 9V type BF1109.
These Mosfets are also enhancement types and therefore no negative voltages are needed for fully switching-off the Mosfets.
Due to this it is not necessary to lift up the Source voltage.
Because of the fully integrated bias no external resistor at Gate1 is needed for biasing the Mosfets.
Both types, BF1105 and BF1109, have been developed for a typical "Self Biasing Current" of 12mA.
For application of these types the nominal Gate2 voltage is to be set to 4V.
In 5V applications the nominal AGV voltage is 4V. In a 9V application 7.5V.
For the 9V application a voltage divider at Gate2 is needed. Because there is no Gate2 current, no special requirements for this divider are necessary.
The d.c circuit for biasing the Mosfets with fully integrated bias is than as given in Fig. 3 (next page).
The necessary resistors for the different applications are given in table 3 (next page).

The Self Biasing Currents of the BF1105 and BF1109 are, over a large range of the supply voltage, marginally dependent on the supply voltage.
The relation between the Self Biasing Currents, of the BF1105 and BF1109, and the supply voltage is given in graph 4 (next page).

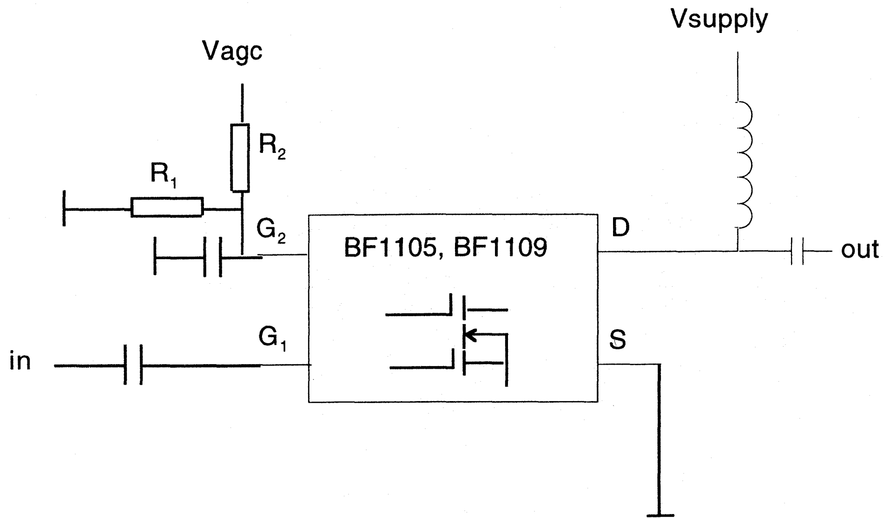
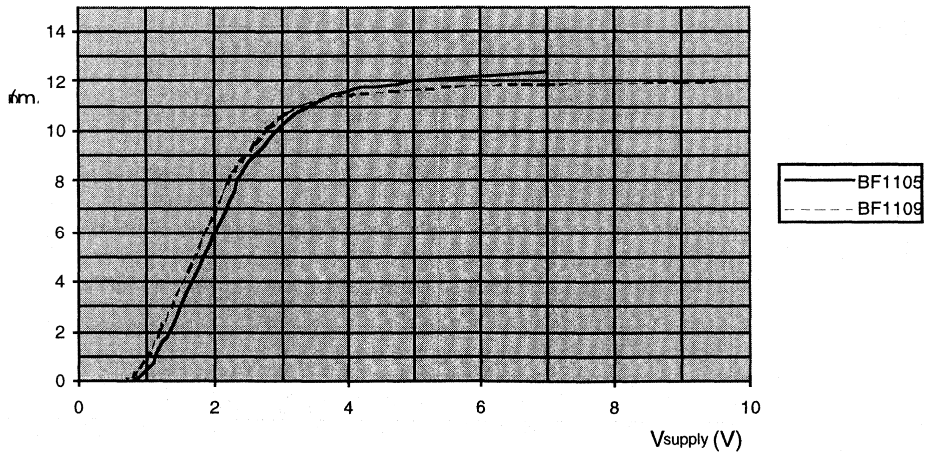


Fig. 3: Principle of the bias circuit for Mosfets with fully integrated bias.

Table 3: Resistors in the bias circuit for Mosfets with fully integrated bias.

	Application	R_1 / R_2
BF1105	5V	no R_1
BF1109	9V	8 / 7



Graph 4.

4. SWITCHING-OFF THE MOSFETS

General

All the Mosfets can be switched-off at the Drain, Gate1, Gate2 and the Source. Switching-off at Gate2 is usually not done, because Gate2 is used for AGC purposes.
If switching-off at Gate2 can be combined with AGC it will also be a possible solution. This method of switching-off will not be described in this report.
Switching-off at the Source is also not recommendable. Especially not for the Mosfets with partly - and fully integrated bias, because at these Mosfets the Sources are directly connected to ground.
Therefore we concentrate only on switching-off in the Drain and at Gate1.

Switching-off in the Drain

Switching-off in the Drain is usually done with a switching transistor in series with the Drain of the Mosfet.
This switching transistor is an open collector pnp transistor, which is situated in the PLL- or MOPLL IC.
With this method of switching the supply voltage to the Drain is switched-off or - on.
There is no principle difference in switching the different types of Mosfets.
The principle circuits of the Mosfets with the switches are than as given in the Figs. 4, 5 and 6.

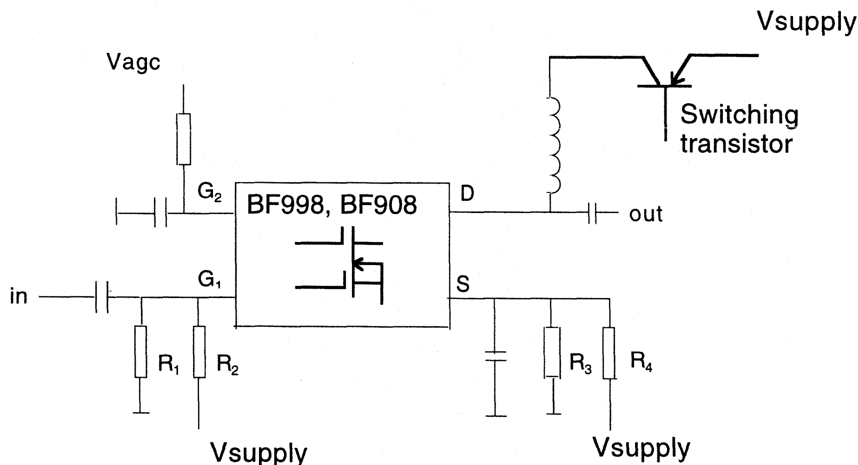


Fig.4: Switching in the Drain of the Mosfets BF998 and BF908

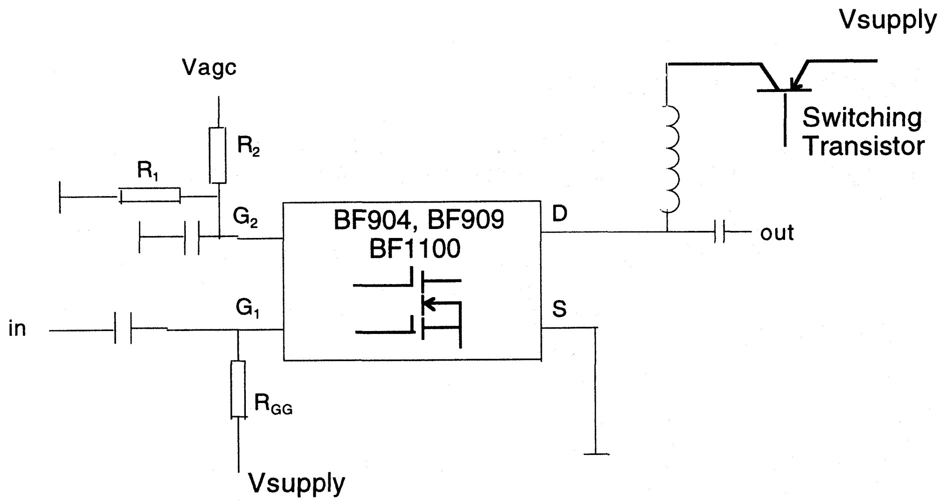


Fig.5: Switching in the Drain of the Mosfets BF904, BF909 and BF1100

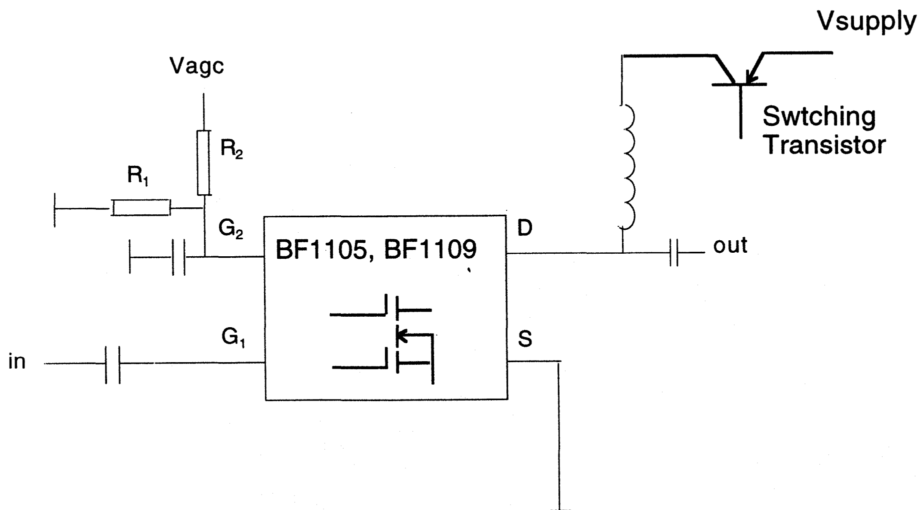


Fig.6: Switching in the Drain of the Mosfets BF1105 and BF1109

Note:
If switching is done in the Drain special attention must be paid to the influence of the voltage drop over the switch.
In some applications (2 band concepts with switched v.h.f. bands with band-switching diodes) also a bandswitching diode is d.c. connected in series with the switching transistor. This causes extra voltage drop.
In 12V applications (BF998, BF908 and BF1100) and the 9V applications (BF998 and BF908) this has marginal influence on the a.c. performance.
In the 9V application of the BF1100 this voltage drop can cause worse cross-modulation at nominal gain. Especially at relatively high load impedances.
This is also the case in the 5V application of the BF904, BF909 and the BF1105.
This influence is decribed in chapter 8.
This worse cross-modulation performance can be compensated by decreasing the nominal Gate2 voltage by appr. 0.5 V - 1 V. This has little influence on the gain as can be seen from the AGC characteristics (chapter 6).

Switching-off at Gate1 with open collector p.n.p. switch
This method of switching is only possible in the circuits with BF998 / BF908 and BF904 / BF909 / BF1100. This methode of switching is not possible if the BF1105 or the BF1109 are applied. This because of the lay out of the internal biasing circuit in these Mosfets.
The principle circuits for switching-off these Mosfets at Gate1 are given in the Figs. 7 and 8.

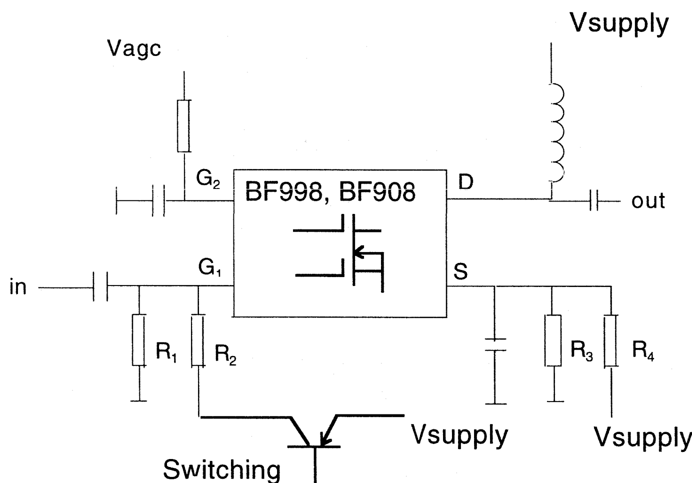


Fig.7: Sv ı open collector p.n.p. transistor at Gate1 of the Mosfets BF998 and BF908

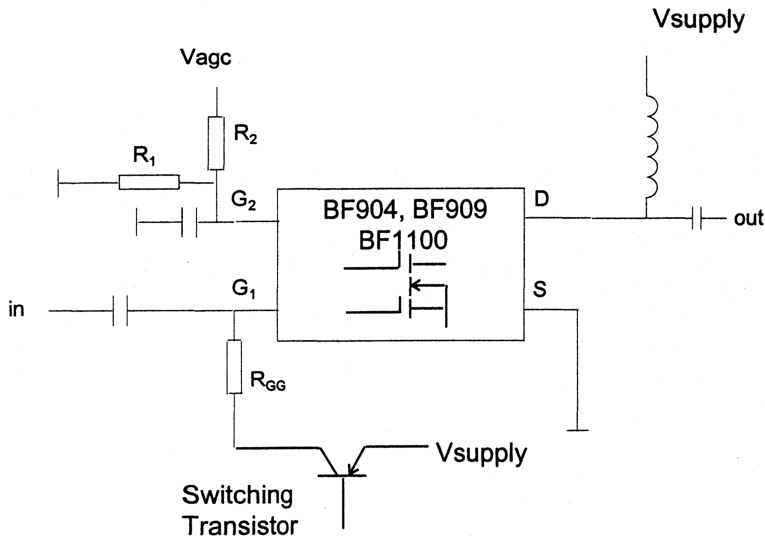


Fig.8: Switching with open collector p.n.p. transistor at Gate1 of the Mosfets BF904,BF909 and BF1100

Switching-off at Gate1 with open collector n.p.n. switch

This method of switching can be used for all types of Mosfets. However, for some types an extra resistor is needed.

The principle circuits for switching-off the different types of Mosfets are given in the Figs. 9, 10 and 11.

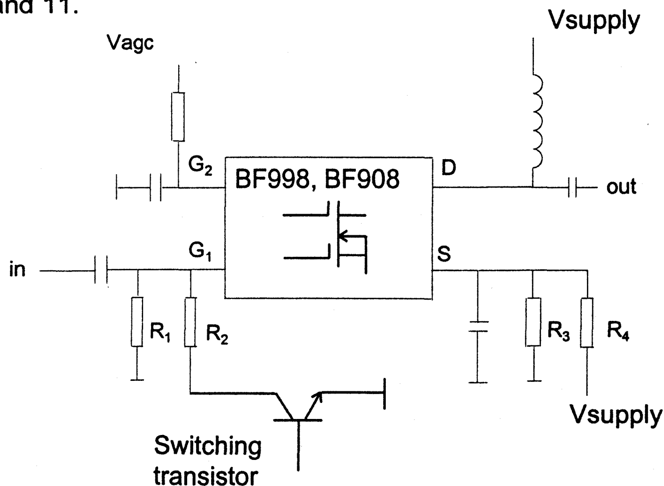


Fig.9: Switching with open collector n.p.n. transistor at Gate1 of the Mosfets BF998 and BF908

Application of Philips Dual-gate MOSFETs

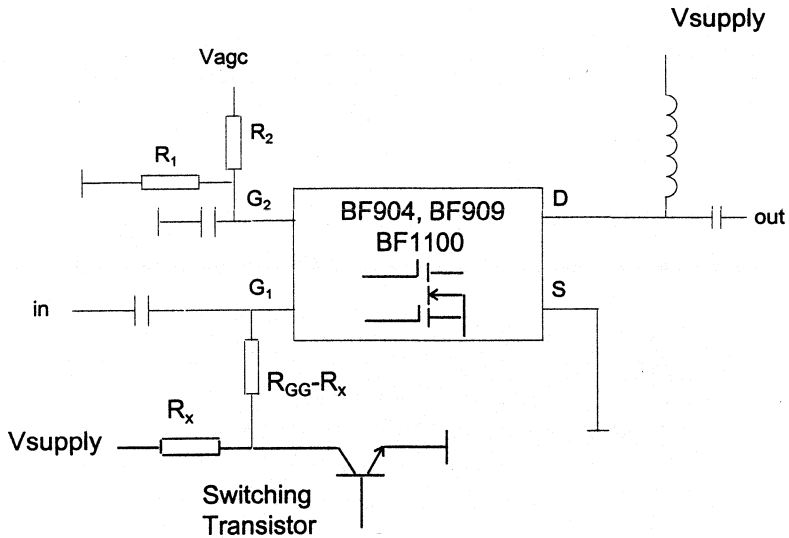


Fig.10: Switching with open collector n.p.n. transistor at Gate1 of the Mosfets BF904, BF909 and BF1100

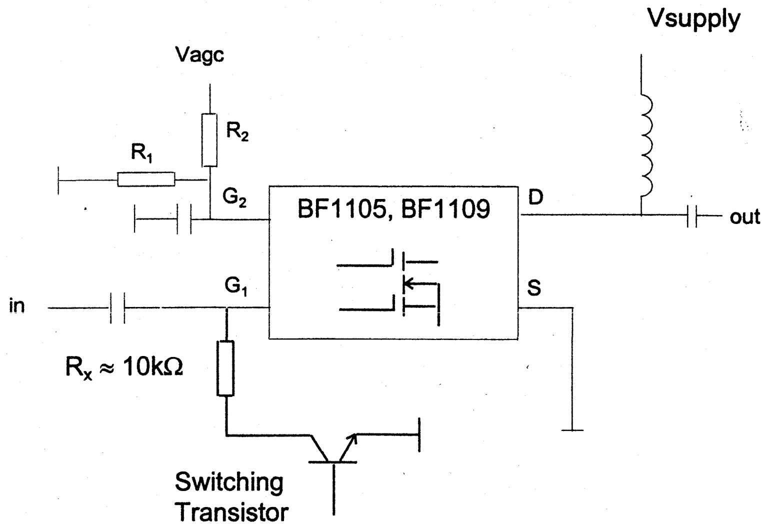
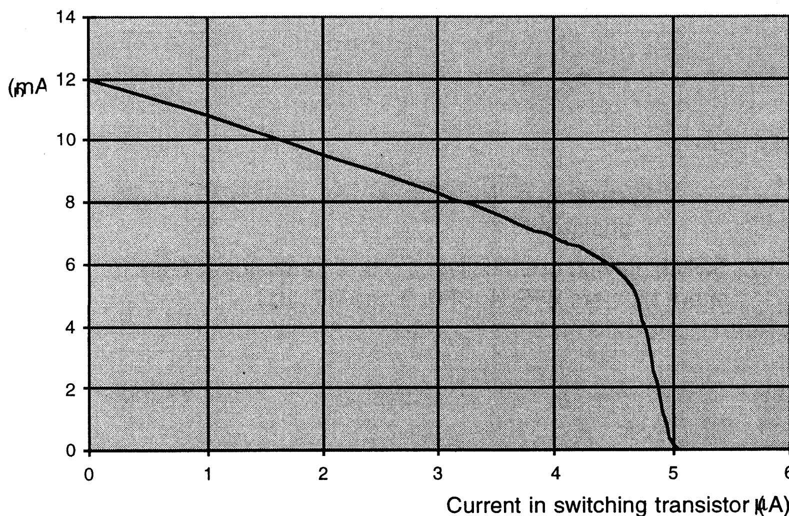


Fig.11: Switching with open collector n.p.n. transistor at Gate1 of the Mosfets BF1105 and BF1109

Application of Philips Dual-gate MOSFETs

The principle of the switching-off in the circuits of the BF998 / BF908 and BF904 / BF909 / BF1100 is switching Gate1 to a voltage lower than the pinch-off voltage of the applied Mosfet.
The principle of the switching-off in the circuit of the BF1105 and BF1109 is different. In this circuit the current flowing through the switching transistor determines the Drain current of the Mosfet (see Graph. 6).

Drain current of the Mosfets BF1105 and BF1109 as function of the current in the switching transistor



Graph 6

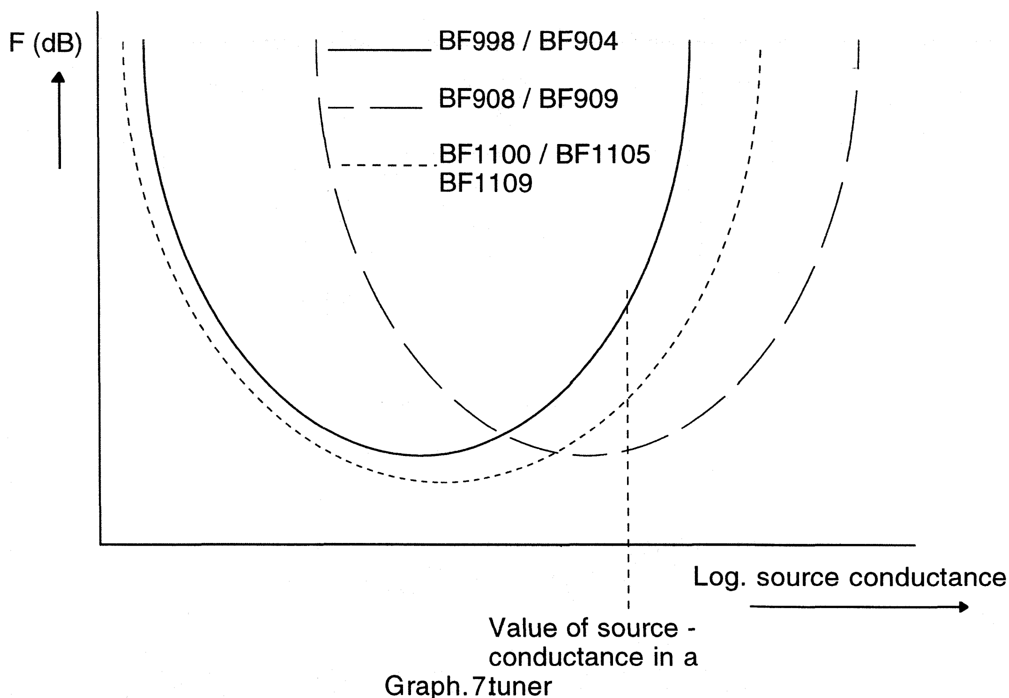
If the Drain current is zero the Mosfet is switched-off. If the current through the switching transistor is zero, the Mosfet is switched-on.
The resistor R_x in the circuit with the BF1105 and BF1109 is choosen ≈ 10kΩ, because this value is high enough to have almost no influence on the noise figure and low enough to ensure the necessary current through the switching transistor.

5. **WHEN USING A MOSFET WITH HIGH TRANSFERCONDUCTANCE?**
In a tuner the source conductance offered to the Gate1 of the Mosfets is relatively high. A Mosfet with high transferconductance (Y_{fs}) has lower noise figures at high source conductances than a Mosfet with low Y_{fs}.
The Mosfets BF908 and BF909 have high Y_{fs}. Appr. 1.75 x the Y_{fs} of the BF998 and BF904.
However, the input- and output capacitances have also been increased with about the same factor.This higher capacitances often give problems in the tuners with frequency range. In spite of that these Mosfets can be used if low noise is required.

Application of Philips Dual-gate MOSFETs

The Mosfets BF1100, BF1105 and BF1109 have low capacitances with a Y_{fs} between that of the BF904 / BF998 and BF908 / BF909.This medium Y_{fs} is combined with the low capacitance of the BF904 and BF998.

The principle of the noise behaviour as a function of the source conductance of the different types of Mosfets is given in Graph. 7.



Graph. 7

From this graph we see that Mosfets with low Y_{fs} have relatively high noise figures at the source conductances offered to the Gate1 of the Mosfets. The Mosfets with the highest Y_{fs} have the lowest noise figure.

6. AGC CHARACTERISTICS

The AGC characteristics of the different Mosfets are measured in the a.c. circuit as given in Fig.12 (next page). The d.c. circuits were as described in chapter 3.
For 12V applications the nominal AGC voltage was choosen 9V, for 9V applications 7.5V and for 5V applications 4V.
All Mosfets are measured at 50MHz. The results of these measurements are given in the Graphs 8 (12V application), 9 (9V application) and 10 (5V application).
From these graphs we see that the Mosfets with partly - and fully integrated bias have a steeper AGC characteristic than the Mosfets without integrated bias.

Application of Philips Dual-gate MOSFETs

However, the steepness of these AGC characteristics is not steeper than the steepness of the AGC characteristics of the Mosfets without integrated bias at 800MHz. Therefore this will not lead to additional problems in a TV set, since the AGC circuit has to be designed for this steep characteristc.
For information about the frequency dependency of the AGC characteristics we have measured the BF998 and the BF1105 also at 800 MHz.
The results of these measurements are given in Graph 11.

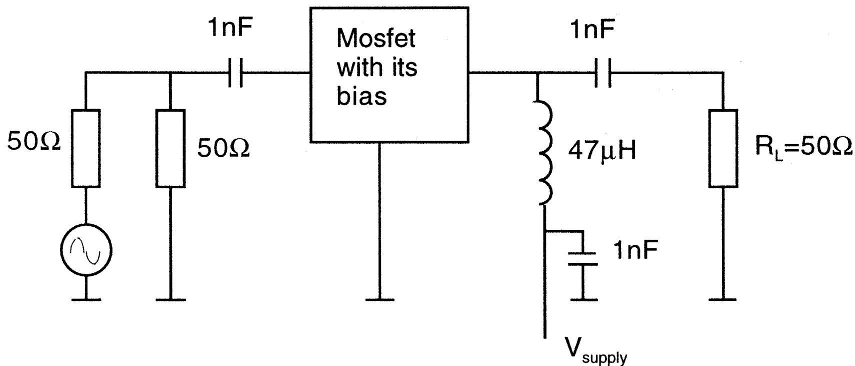
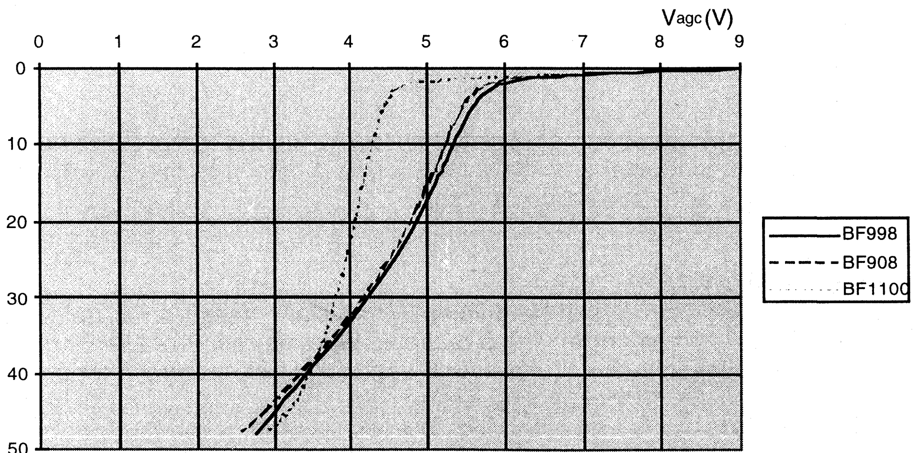
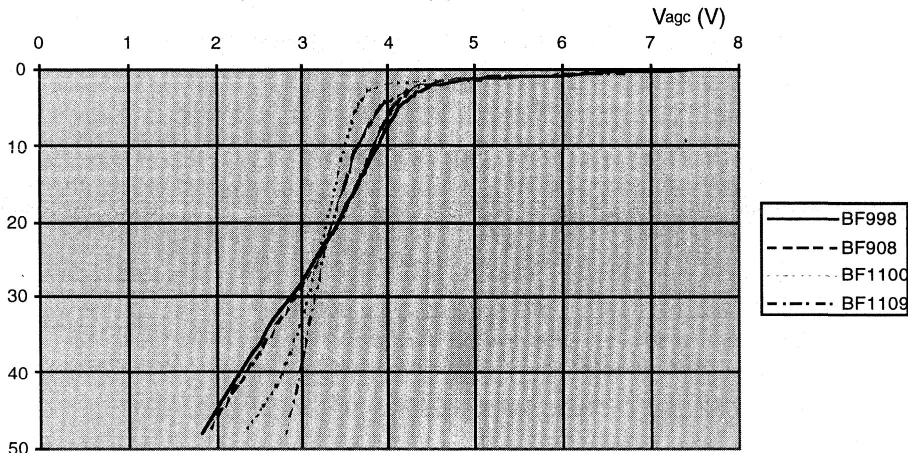


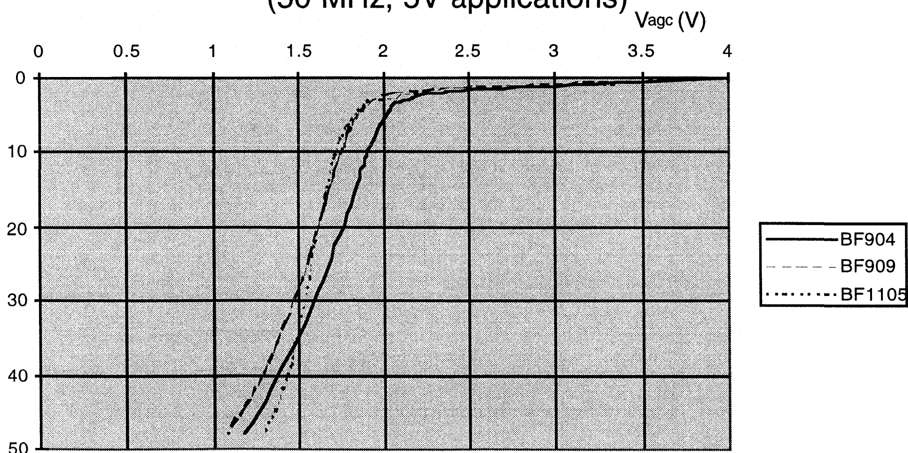
Fig. 12: AGC and cross-modulation test circuit



Graph 8

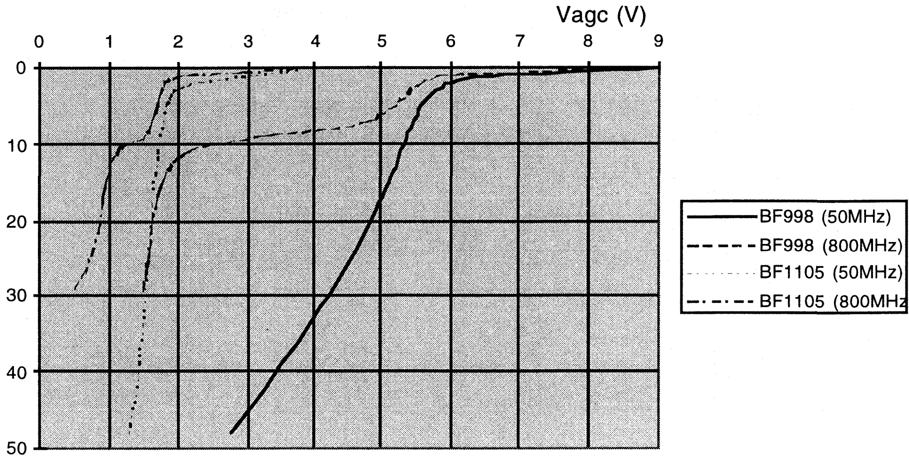


Graph 9



Graph 10

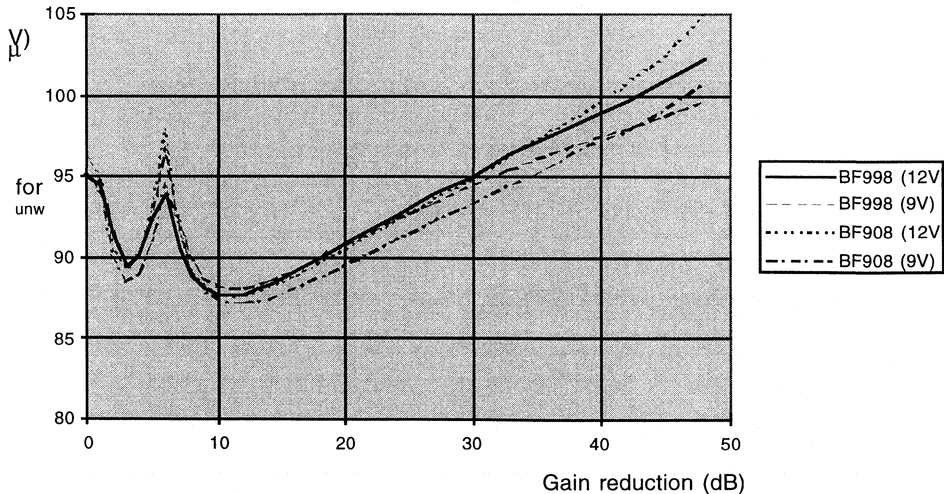
Application of Philips Dual-gate MOSFETs



Graph 11

7. **CROSS-MODULATION PERFORMANCE**

The cross-modulation performance was measured in a circuit of which the principle is given in Fig.12 (page 15).
The results of the cross-modulation measurements in the circuit of Fig.12 are given in the Graphs 12, 13, and 14.
Graph 12 shows the cross-modulation performance of the Mosfets without integrated bias.



Graph 12

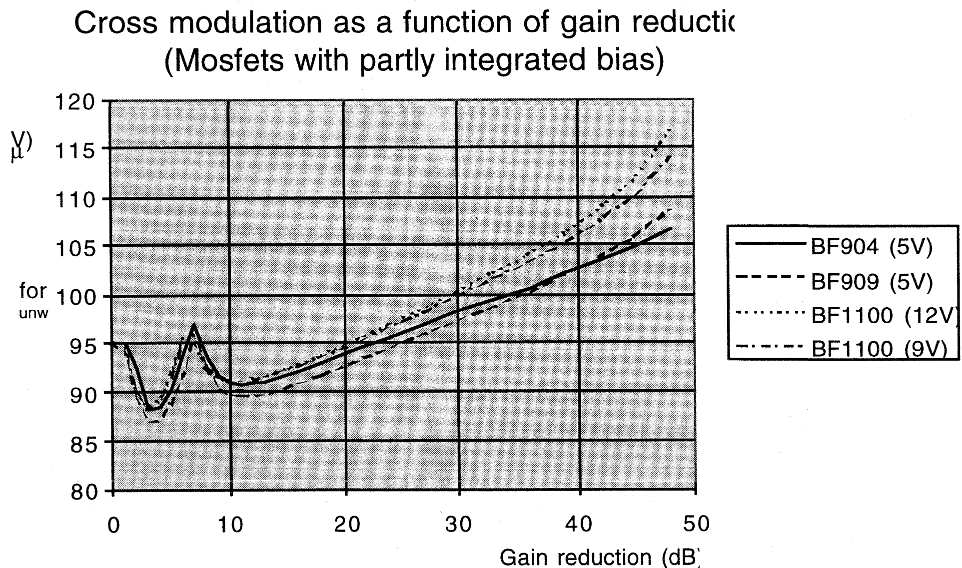
Application of Philips Dual-gate MOSFETs

The difference in the curves of the BF998 and BF908 (at gain reduction > 40dB) is caused by internal capacitances. Internal capacitances of the BF908 are higher than that of the BF998. Due to this the cross-modulation performance after 40 dB gain reduction is extra increasing.

Note: Series inductance in the Source has the same effect as increasing the internal capacitances.

The difference in the performance at 12V and 9V supply voltages are caused by the difference in effective Source resistor. Due to this effective Source resistor, the Gate1 - Source voltage increases 3V in a 12V application and only 2V in a 9V application during AGC.
The higher this voltage-increase, the better the cross-modulation performance.

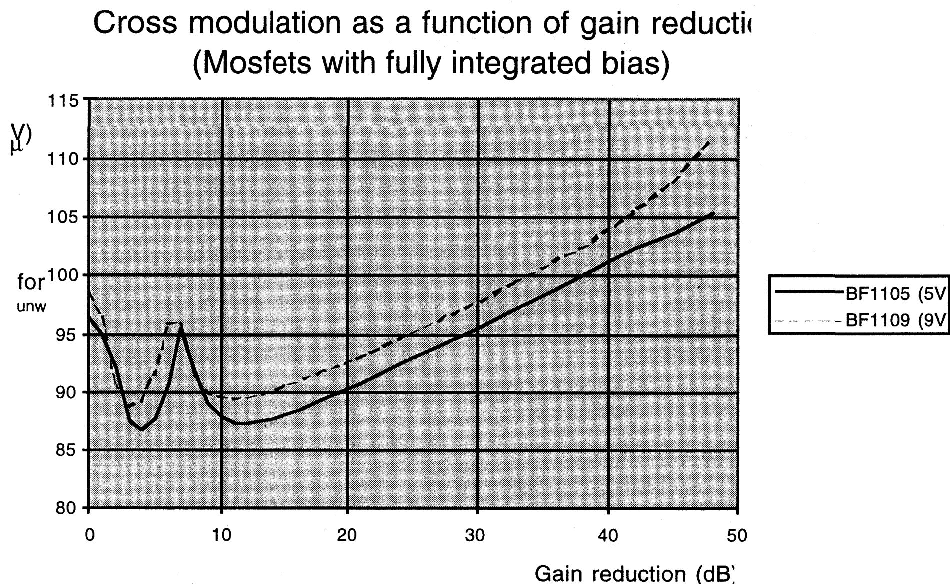
Graph 13 shows the cross-modulation performance of the Mosfets with partly integrated bias.



Graph 13

The difference we see here is also caused by the different increase of the Gate1 - Source voltage during AGC, caused by the different supply voltages.
For the BF904 and BF909, in a 5V application the Gate1 - Source voltage at maximum gain reduction is 5V.
For the BF1100 the Gate1 - Source voltage at maximum gain reduction is 9V in a 9V application and 12V in a 12V application.

Graph 14 shows the cross-modulation performance of the Mosfets with fully integrated bias.



Graph 14

The differences we see here are also caused by the difference in Gate1 - Source voltage at maximum gain reduction.
For the BF1105 this is 5V and for the BF1109 this is 9V.

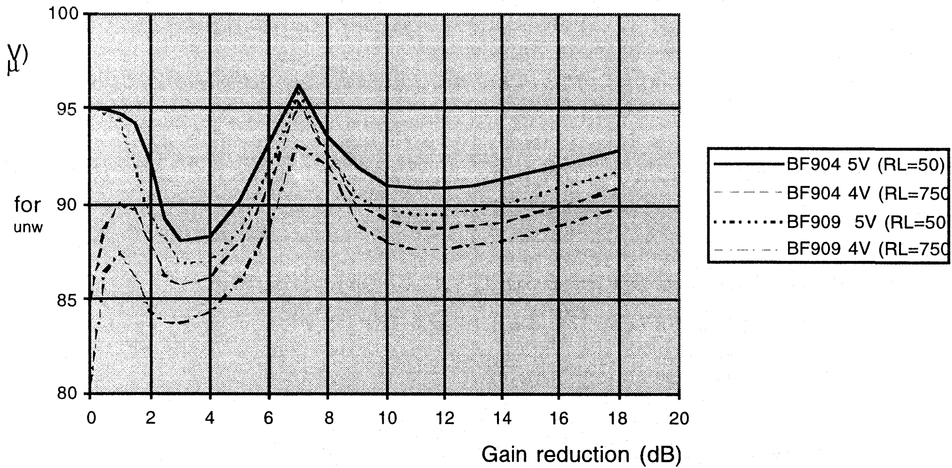
8. INFLUENCE OF DRAIN VOLTAGE AND LOAD IMPEDANCE ON CROSS-MODULATION PERFORMANCE

The Graphs 12, 13 and 14 are measured with a load impedance (R_L) of 50Ω.
The supply voltage and the Drain voltage in this circuit are the same, because no switching transistor and / or bandswitching diode is connected in series with the Drain.
As mentioned in chapter 4, the Drain voltage can be 1V lower than the supply voltage. This will influence the cross-modulation performance, especially at higher values of the load impedance. Therefore we have also measured the cross-modulation performance with a load impedance (R_L) of ≈ 750Ω, and the Drain voltage is 1V lower than the supply voltage.
These measurements are done for the Mosfets with partly integrated bias and the Mosfets with fully integrated bias.
The main differences appear at the first few dB's of gain reduction.
Therefore we have measured these graphs only untill 18 dB gain reduction.
The BF904, BF909 and BF1105 are measured at Drain voltages of 5V and 4V and load impedances of 50Ω and 750Ω.

Application of Philips Dual-gate MOSFETs

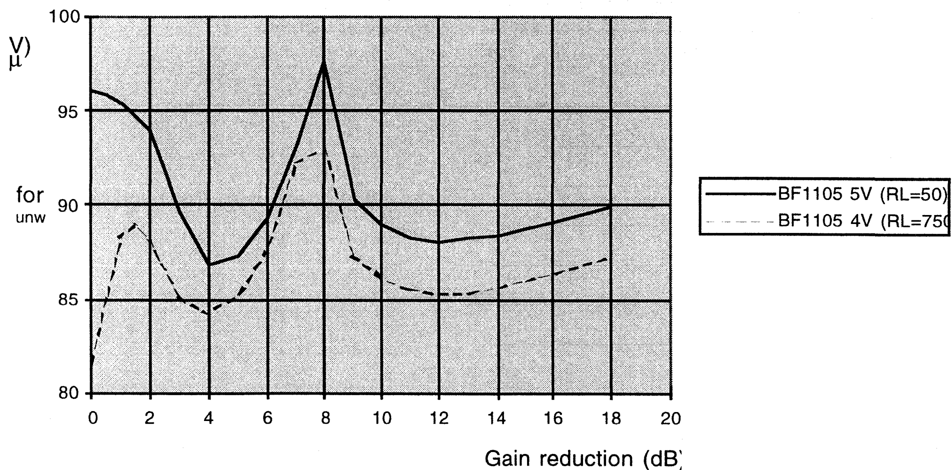
The results of these measurements are given in the Graphs 15 and 16.

Cross modulation as a function of gain reductic
(R_L=50Ω and 750Ω; V_D=5V and 4V)



Graph 15

Cross modulation as a function of gain reductic
(V_D=5V, R_L=50Ω and V_D=4V, R_L=750Ω)

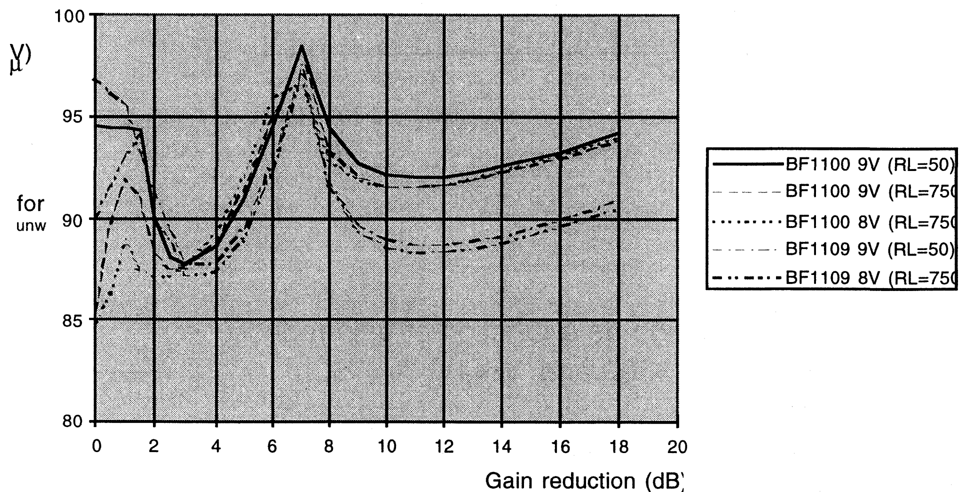


Graph 16

Application of Philips Dual-gate MOSFETs

For the 5V Mosfets the cross-modulation performance is, at 5V Drain voltage, not influenced by the load impedance.

For the 9V Mosfet BF1109 this is also the case.
The results of the Measurements on the 9V Mosfets are given in Graph 17.
For the 9 - 12V Mosfet BF1100 the cross-modulation performance at 9V Drain voltage is influenced by the load impedance.
Therefore we have also given the cross-modulation characteristic of this Mosfet at V_D = 9V and R_L = 750Ω in Graph 17.



Graph 17

9. CONCLUSIONS

For the modern 9V and 5V applications we recommend to use the Mosfets with partly - and fully integrated bias. This because less external components are needed for biasing.
The advantage of the Mosfets with partly integrated bias is that these devices can be used at different voltages and different Drain currents.
The BF1100 can be applied between 9V and 12V and at Drain currents between 5mA and approx. 15mA.
The BF904 can be applied between 3V and 7V, at Drain currents between 5mA and approx. 15mA. The BF909 also between 3V and 7V and between Drain currents of 5mA and approx. 20mA.
It must be taken into account that if the supply voltage is choosen below 5V, the nominal AGC voltage should be choosen at least 0.5V lower than the supply voltage.

The advantage of the Mosfets with fully integrated bias is that the "self biasing" current over a relatively large range is almost independent of the supply voltage.
The cross-modulation performance at low values of gain reduction is strongly dependent on the load impedance offered to the Drain of the Mosfet.
Especially, at Drain voltages lower than the nominal value.
This lower Drain voltage can be caused by a voltage drop over the switching transistor and (eventually) bandswitching diode in series with the Drain.
This can, for a large amount, be compensated by decreasing the nominal Gate2 voltage with the same amount as the above mentioned voltage drop.
Than, the gain will be marginally lower.

If low noise is required the Mosfets with the highest transferconductance can be applied, if the higher capacitance values are not causing problems.
Switching-off for al Mosfets can be done in the Drain with open collector p.n.p. transistors.
The Mosfets with partly integrated bias can also be switched-off at Gate1 with open collector p.n.p. transistors as well as with open collector n.p.n. transistors.
The Mosfets with fully integrated bias can also be switched-off at Gate1, but only with open collector n.p.n. transistors.

DEVICE DATA

in alphanumeric sequence

N-channel field-effect transistors — 2N5484; 2N5485; 2N5486

FEATURES

- Low noise
- Interchangeability of drain and source connections
- High gain.

DESCRIPTION

N-channel, symmetrical, silicon junction FETs in a SOT54 (TO-92) envelope, intended for use in VHF/UHF amplifiers, oscillators and mixers.

PINNING - SOT54 (TO-92)

PIN	DESCRIPTION
1	gate
2	source
3	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	25	V
I_{DSS}	drain current	V_{DS} = 15 V; V_{GS} = 0			
	2N5484		1	5	mA
	2N5485		4	10	mA
	2N5486		8	20	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C	–	400	mW
$V_{GS(off)}$	gate-source cut-off voltage	V_{DS} = 15 V; I_D = 1 nA			
	2N5484		−0.3	−3	V
	2N5485		−0.5	−4	V
	2N5486		−2	−6	V
$\|Y_{fs}\|$	common source transfer admittance	V_{DS} = 15 V; V_{GS} = 0; f = 1 kHz			
	2N5484		3	6	mS
	2N5485		3.5	7	mS
	2N5486		4	8	mS

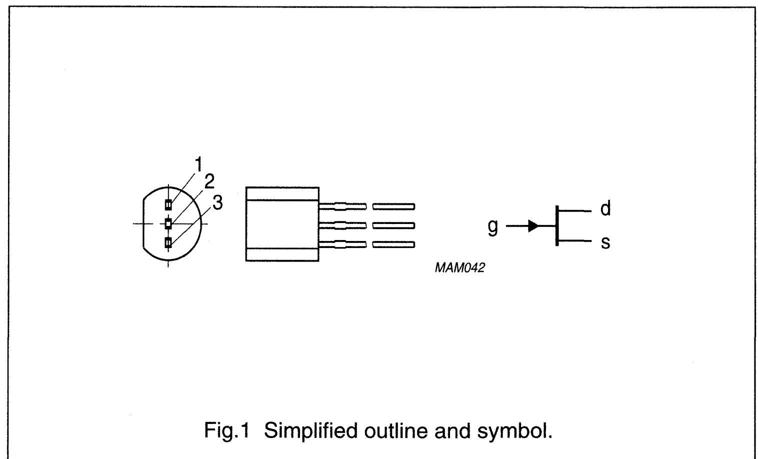


Fig.1 Simplified outline and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	25	V
V_{GSO}	gate-source voltage		–	–25	V
V_{GDO}	gate-drain voltage		–	–25	V
I_G	DC forward gate current		–	10	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C (note 1)	–	400	mW
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	350 K/W

Note

1. Device mounted on a printed circuit board; maximum lead length 3 mm; mounting pad for drain lead minimum 10 mm × 10 mm.

STATIC CHARACTERISTICS

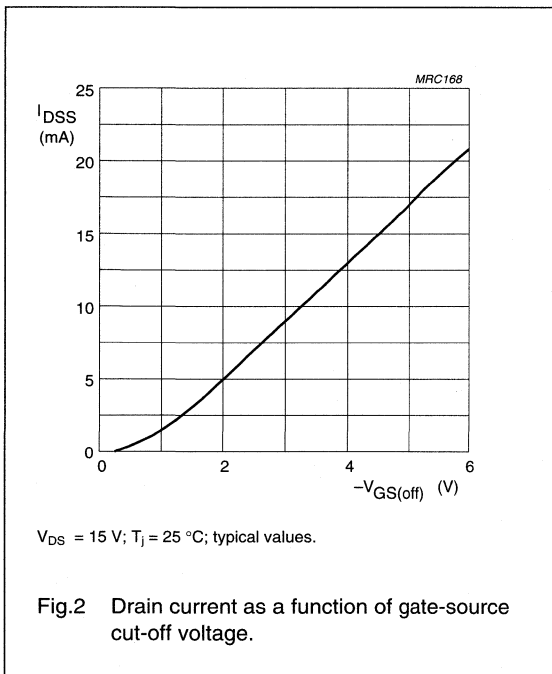
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{(BR)GSS}$	gate-source breakdown voltage	V_{DS} = 0; I_G = –1 μA	–25	–	V
I_{DSS}	drain current	V_{DS} = 15 V; V_{GS} = 0			
	2N5484		1	5	mA
	2N5485		4	10	mA
	2N5486		8	20	mA
I_{GSS}	reverse gate leakage current	V_{DS} = 0; V_{GS} = –15 V	–	–1	nA
V_{GSS}	gate-source forward voltage	V_{DS} = 0; I_G = 1 mA	–	1	V
$V_{GS(off)}$	gate-source cut-off voltage	V_{DS} = 15 V; I_D = 1 nA			
	2N5484		–0.3	–3	V
	2N5485		–0.5	–4	V
	2N5486		–2	–6	V
$\lvert Y_{fs} \rvert$	common source transfer admittance	V_{DS} = 15 V; V_{GS} = 0			
	2N5484		3	6	mS
	2N5485		3.5	7	mS
	2N5486		4	8	mS
$\lvert Y_{os} \rvert$	common source output admittance	V_{DS} = 15 V; V_{GS} = 0			
	2N5484		–	50	μS
	2N5485		–	60	μS
	2N5486		–	75	μS

DYNAMIC CHARACTERISTICS

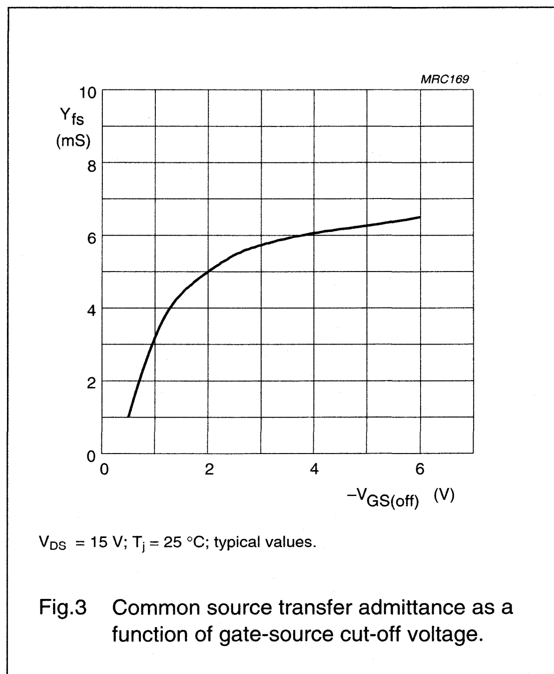
T_j = 25 °C; V_{DS} = 15 V; V_{GS} = 0

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_{is}	input capacitance	f = 1 MHz	–	–	5	pF
C_{os}	output capacitance	f = 1 MHz	–	–	2	pF
C_{rs}	feedback capacitance	f = 1 MHz	–	–	1	pF
g_{is}	common source input conductance					
	2N5484	f = 100 MHz	100	–	–	µS
	2N5485; 2N5486	f = 400 MHz	–	–	1	mS
g_{fs}	common source transfer conductance					
	2N5484	f = 100 MHz	2.5	–	–	mS
	2N5485	f = 400 MHz	3	–	1	mS
	2N5486	f = 400 MHz	3.5	–	1	mS
g_{os}	common source output conductance					
	2N5484	f = 100 MHz	–	–	75	µS
	2N5485; 2N5486	f = 400 MHz	–	–	100	µS
V_n	equivalent input noise voltage	f = 100 Hz	–	5	–	nV/√Hz



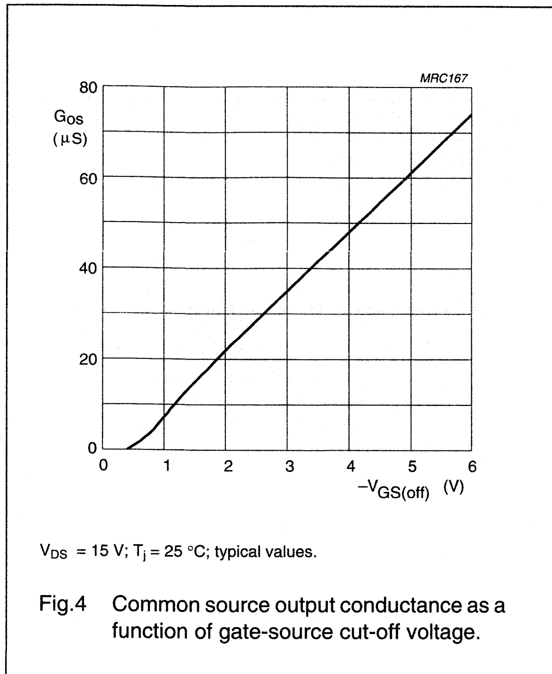
V_{DS} = 15 V; T_j = 25 °C; typical values.

Fig.2 Drain current as a function of gate-source cut-off voltage.



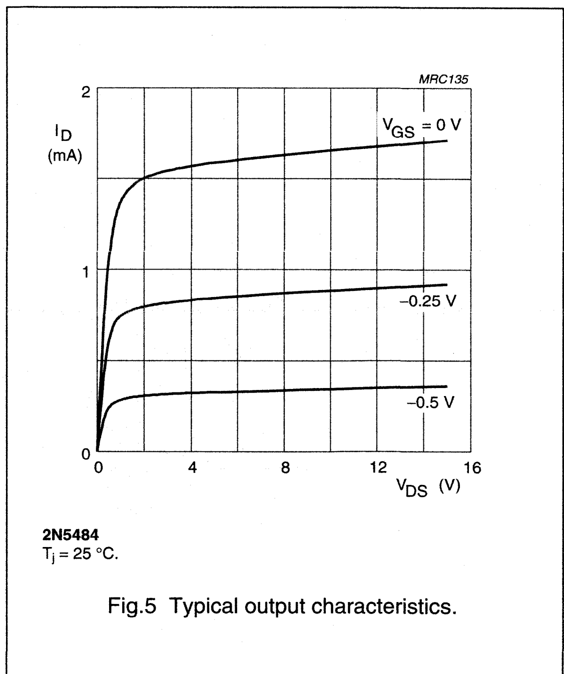
V_{DS} = 15 V; T_j = 25 °C; typical values.

Fig.3 Common source transfer admittance as a function of gate-source cut-off voltage.



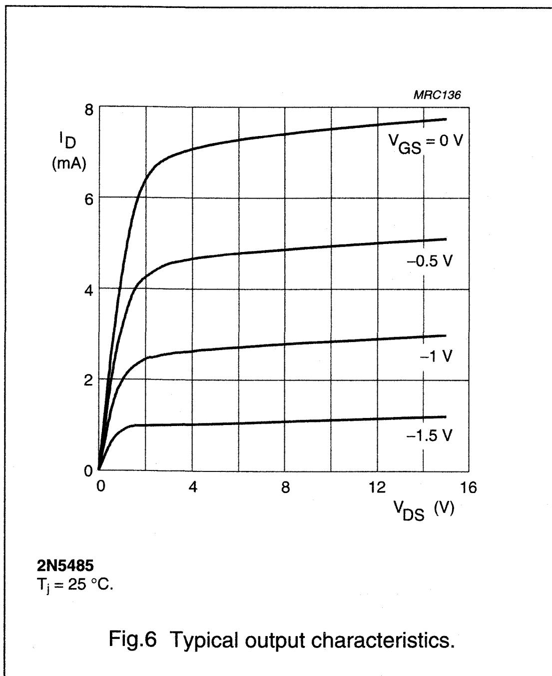
V_{DS} = 15 V; T_j = 25 °C; typical values.

Fig.4 Common source output conductance as a function of gate-source cut-off voltage.



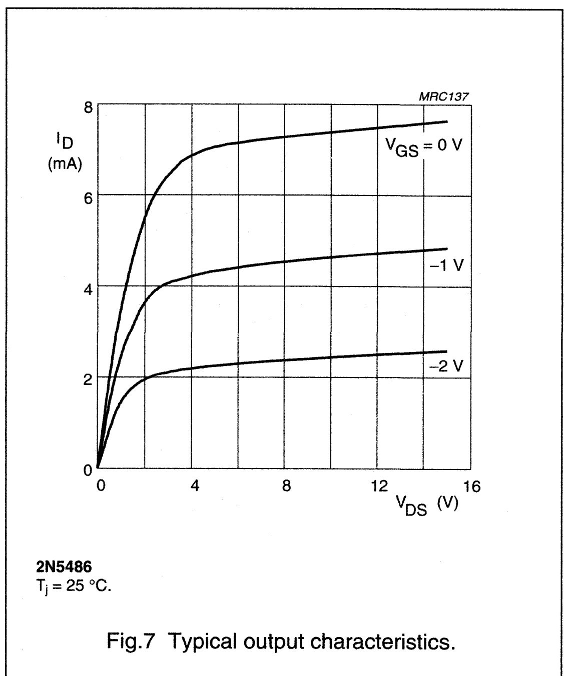
2N5484
T_j = 25 °C.

Fig.5 Typical output characteristics.



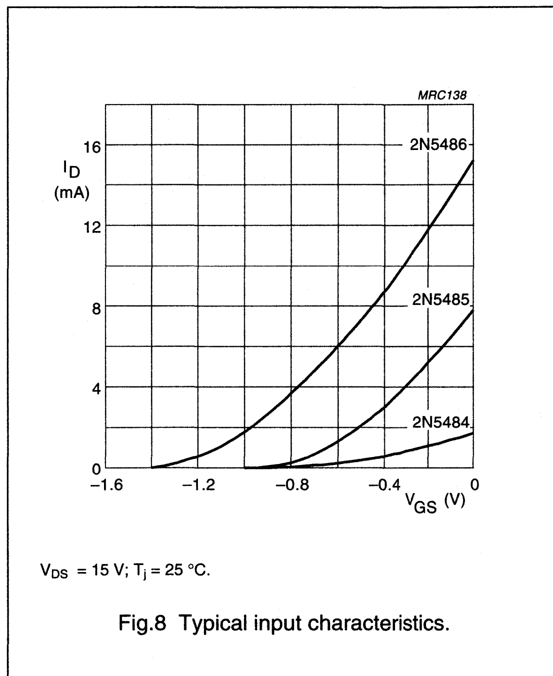
2N5485
T_j = 25 °C.

Fig.6 Typical output characteristics.



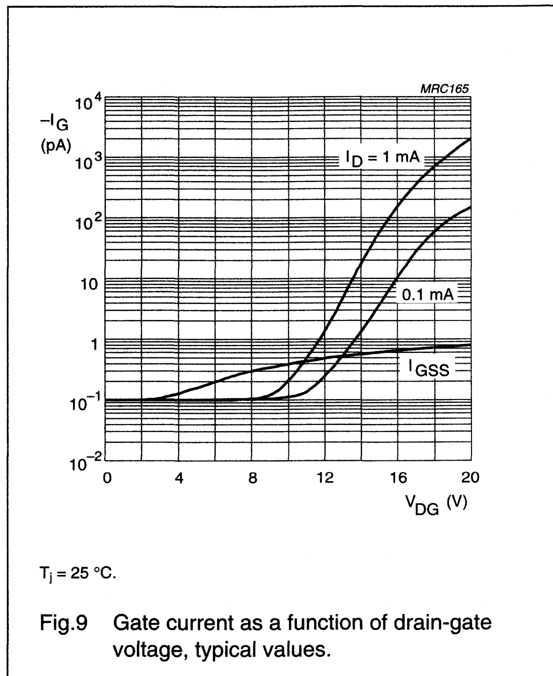
2N5486
T_j = 25 °C.

Fig.7 Typical output characteristics.



V_{DS} = 15 V; T_j = 25 °C.

Fig.8 Typical input characteristics.



T_j = 25 °C.

Fig.9 Gate current as a function of drain-gate voltage, typical values.

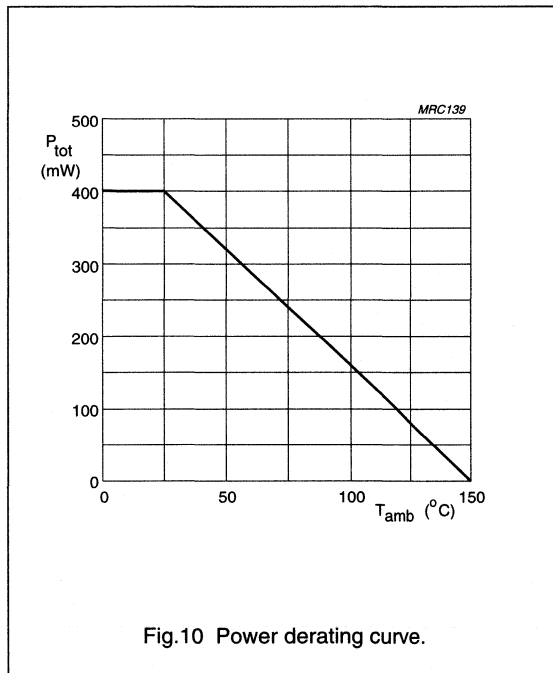
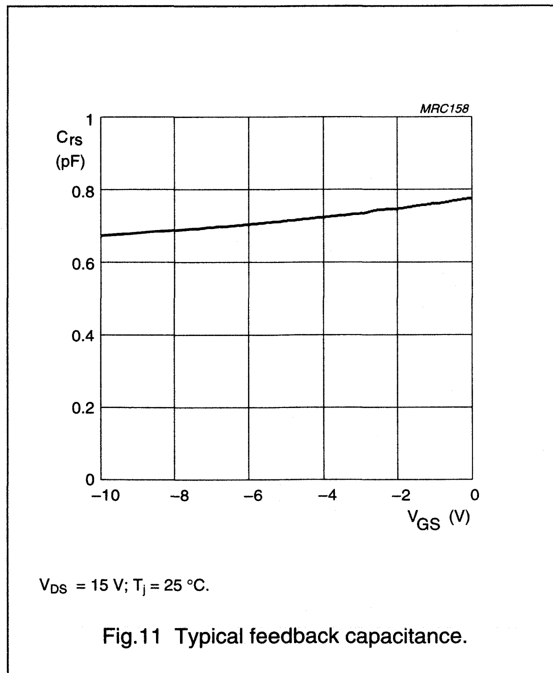
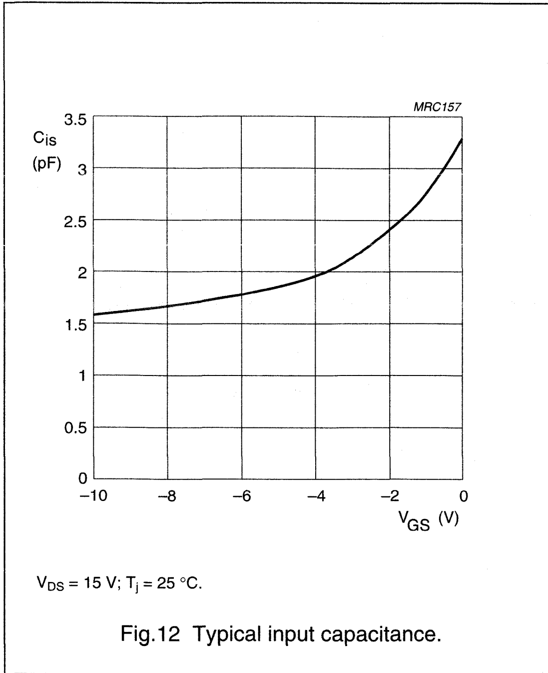


Fig.10 Power derating curve.



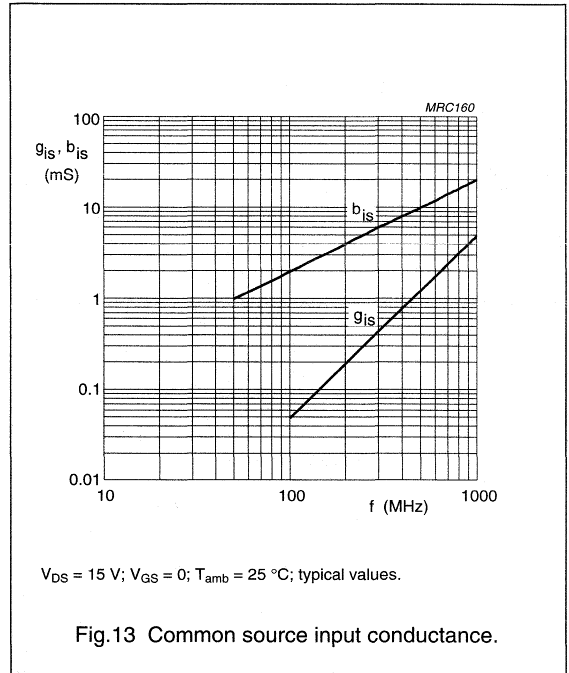
V_{DS} = 15 V; T_j = 25 °C.

Fig.11 Typical feedback capacitance.



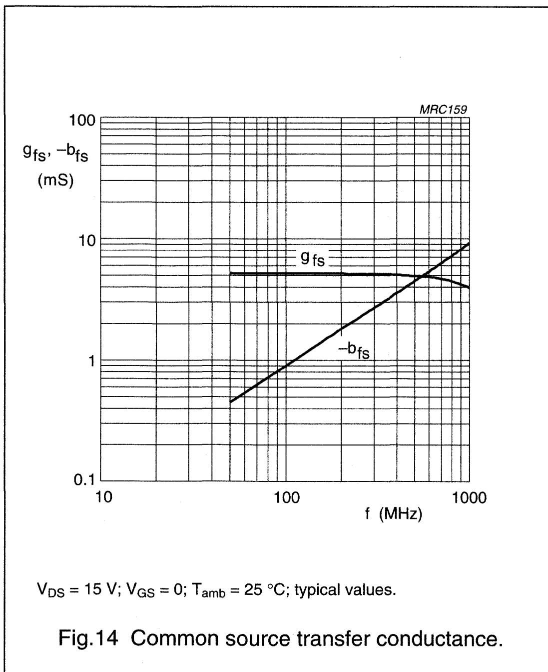
V_{DS} = 15 V; T_j = 25 °C.

Fig.12 Typical input capacitance.



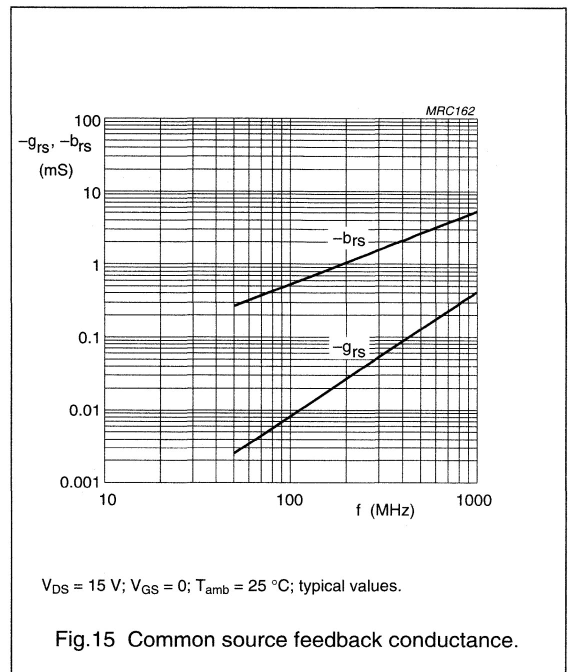
V_{DS} = 15 V; V_{GS} = 0; T_{amb} = 25 °C; typical values.

Fig.13 Common source input conductance.



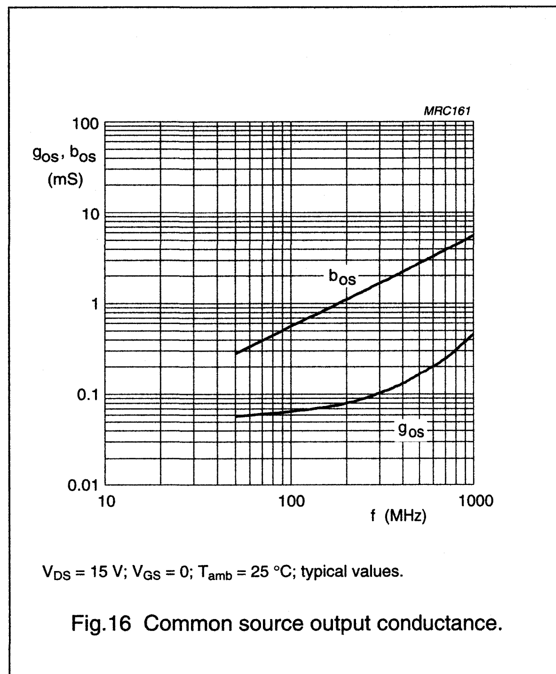
V_{DS} = 15 V; V_{GS} = 0; T_{amb} = 25 °C; typical values.

Fig.14 Common source transfer conductance.



V_{DS} = 15 V; V_{GS} = 0; T_{amb} = 25 °C; typical values.

Fig.15 Common source feedback conductance.



V_{DS} = 15 V; V_{GS} = 0; T_{amb} = 25 °C; typical values.

Fig.16 Common source output conductance.

N-channel silicon field-effect transistors BF245A; BF245B; BF245C

FEATURES

- Interchangeability of drain and source connections
- Frequencies up to 700 MHz.

APPLICATIONS

- LF, HF and DC amplifiers.

DESCRIPTION

General purpose N-channel symmetrical junction field-effect transistors in a plastic TO-92 variant package.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING

PIN	SYMBOL	DESCRIPTION
1	d	drain
2	s	source
3	g	gate

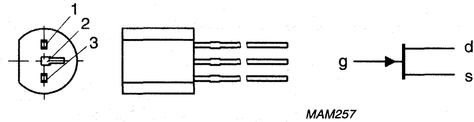


Fig.1 Simplified outline (TO-92 variant) and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DS}	drain-source voltage		–	–	±30	V
V_{GSoff}	gate-source cut-off voltage	I_D = 10 nA; V_{DS} = 15 V	–0.25	–	–8	V
V_{GSO}	gate-source voltage	open drain	–	–	–30	V
I_{DSS}	drain current	V_{DS} = 15 V; V_{GS} = 0				
	BF245A		2	–	6.5	mA
	BF245B		6	–	15	mA
	BF245C		12	–	25	mA
P_{tot}	total power dissipation	T_{amb} = 75 °C	–	–	300	mW
$\lvert y_{fs} \rvert$	forward transfer admittance	V_{DS} = 15 V; V_{GS} = 0; f = 1 kHz; T_{amb} = 25 °C	3	–	6.5	mS
C_{rs}	reverse transfer capacitance	V_{DS} = 20 V; V_{GS} = –1 V; f = 1 MHz; T_{amb} = 25 °C	–	1.1	–	pF

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	±30	V
V_{GDO}	gate-drain voltage	open source	–	–30	V
V_{GSO}	gate-source voltage	open drain	–	–30	V
I_D	drain current		–	25	mA
I_G	gate current		–	10	mA
P_{tot}	total power dissipation	up to T_{amb} = 75 °C;	–	300	mW
		up to T_{amb} = 90 °C; note 1	–	300	mW
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–	150	°C

Note

1. Device mounted on a printed-circuit board, minimum lead length 3 mm, mounting pad for drain lead minimum 10 mm × 10 mm.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	in free air	250	K/W
	thermal resistance from junction to ambient		200	K/W

STATIC CHARACTERISTICS

T_j = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{(BR)GSS}$	gate-source breakdown voltage	I_G = –1 μA; V_{DS} = 0	–30	–	V
V_{GSoff}	gate-source cut-off voltage	I_D = 10 nA; V_{DS} = 15 V	–0.25	–8.0	V
V_{GS}	gate-source voltage	I_D = 200 μA; V_{DS} = 15 V			
	BF245A		–0.4	–2.2	V
	BF245B		–1.6	–3.8	V
	BF245C		–3.2	–7.5	V
I_{DSS}	drain current	V_{DS} = 15 V; V_{GS} = 0; note 1			
	BF245A		2	6.5	mA
	BF245B		6	15	mA
	BF245C		12	25	mA
I_{GSS}	gate cut-off current	V_{GS} = –20 V; V_{DS} = 0	–	–5	nA
		V_{GS} = –20 V; V_{DS} = 0; T_j = 125 °C	–	–0.5	μA

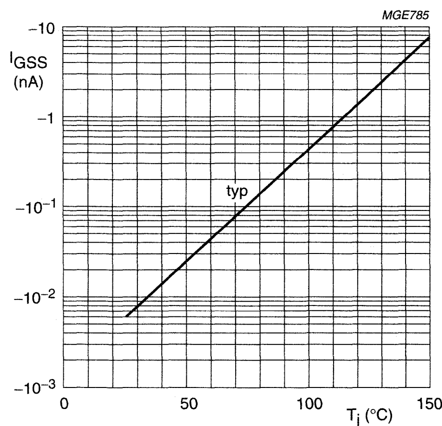
Note

1. Measured under pulse conditions: t_p = 300 μs; $\delta \leq 0.02$.

DYNAMIC CHARACTERISTICS

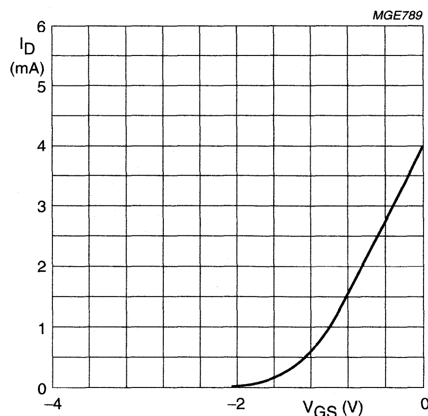
Common source; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_{is}	input capacitance	V_{DS} = 20 V; V_{GS} = −1 V; f = 1 MHz	–	4	–	pF
C_{rs}	reverse transfer capacitance	V_{DS} = 20 V; V_{GS} = −1 V; f = 1 MHz	–	1.1	–	pF
C_{os}	output capacitance	V_{DS} = 20 V; V_{GS} = −1 V; f = 1 MHz	–	1.6	–	pF
g_{is}	input conductance	V_{DS} = 15 V; V_{GS} = 0; f = 200 MHz	–	250	–	μS
g_{os}	output conductance	V_{DS} = 15 V; V_{GS} = 0; f = 200 MHz	–	40	–	μS
$\|y_{fs}\|$	forward transfer admittance	V_{DS} = 15 V; V_{GS} = 0; f = 1 kHz	3	–	6.5	mS
		V_{DS} = 15 V; V_{GS} = 0; f = 200 MHz	–	6	–	mS
$\|y_{rs}\|$	reverse transfer admittance	V_{DS} = 15 V; V_{GS} = 0; f = 200 MHz	–	1.4	–	mS
$\|y_{os}\|$	output admittance	V_{DS} = 15 V; V_{GS} = 0; f = 1 kHz	–	25	–	μS
f_{gfs}	cut-off frequency	V_{DS} = 15 V; V_{GS} = 0; g_{fs} = 0.7 of its value at 1 kHz	–	700	–	MHz
F	noise figure	V_{DS} = 15 V; V_{GS} = 0; f = 100 MHz; R_G = 1 kΩ (common source); input tuned to minimum noise	–	1.5	–	dB



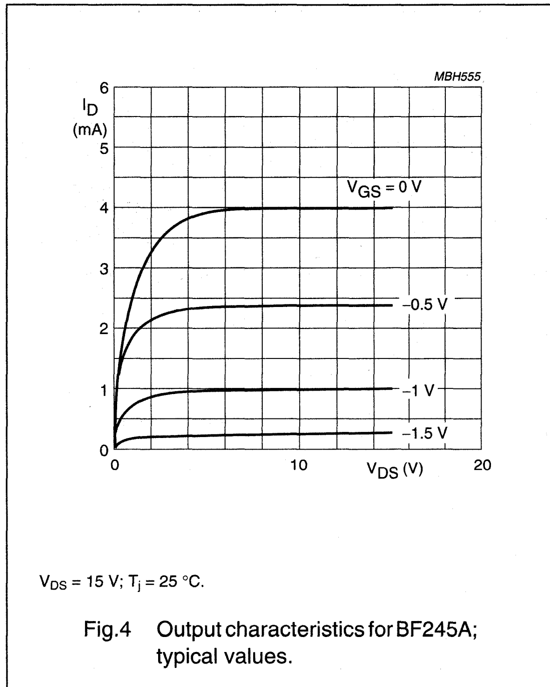
V_{DS} = 0; V_{GS} = −20 V.

Fig.2 Gate leakage current as a function of junction temperature; typical values.



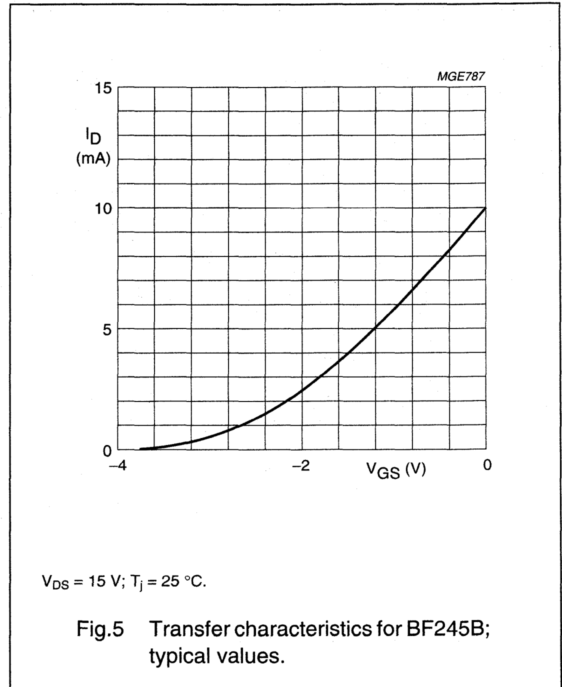
V_{DS} = 15 V; T_j = 25 °C.

Fig.3 Transfer characteristics for BF245A; typical values.



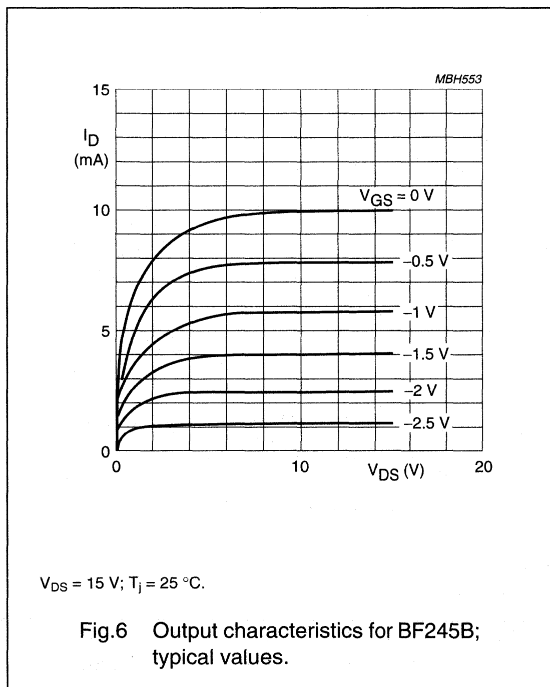
V_{DS} = 15 V; T_j = 25 °C.

Fig.4 Output characteristics for BF245A; typical values.



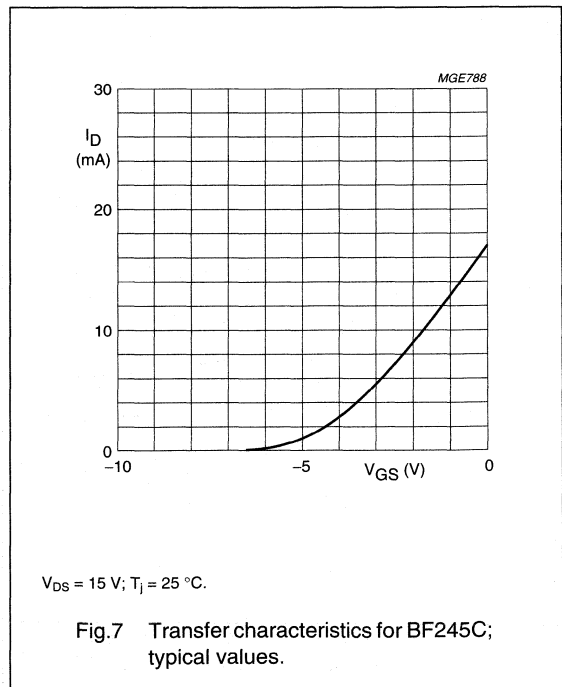
V_{DS} = 15 V; T_j = 25 °C.

Fig.5 Transfer characteristics for BF245B; typical values.



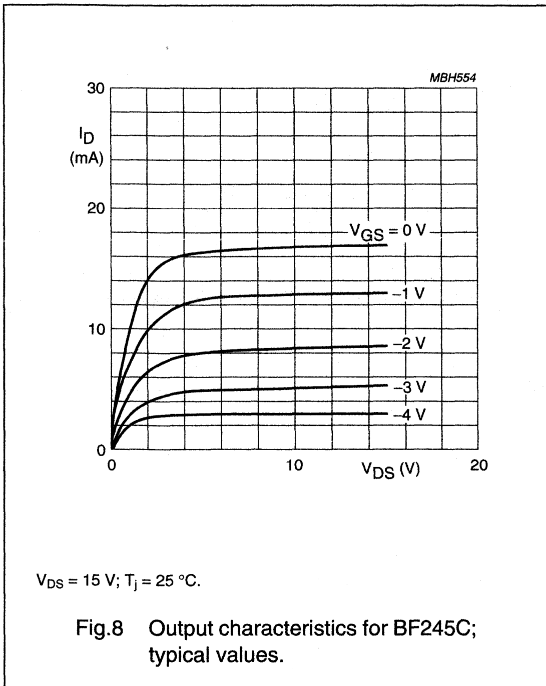
V_{DS} = 15 V; T_j = 25 °C.

Fig.6 Output characteristics for BF245B; typical values.



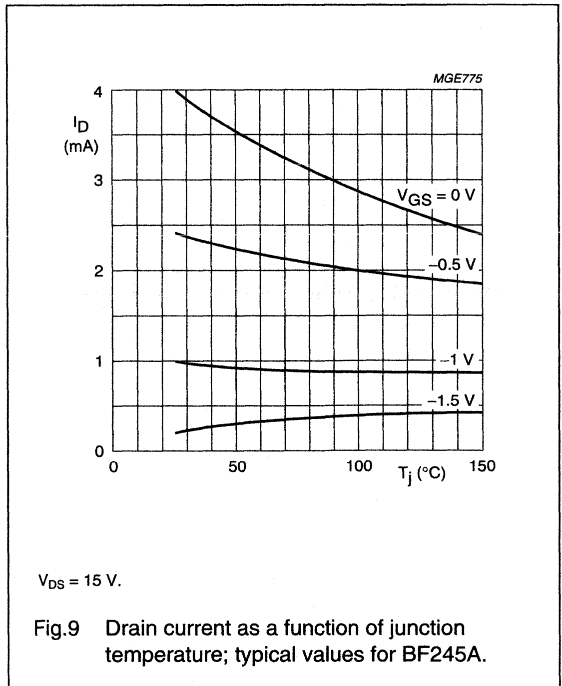
V_{DS} = 15 V; T_j = 25 °C.

Fig.7 Transfer characteristics for BF245C; typical values.



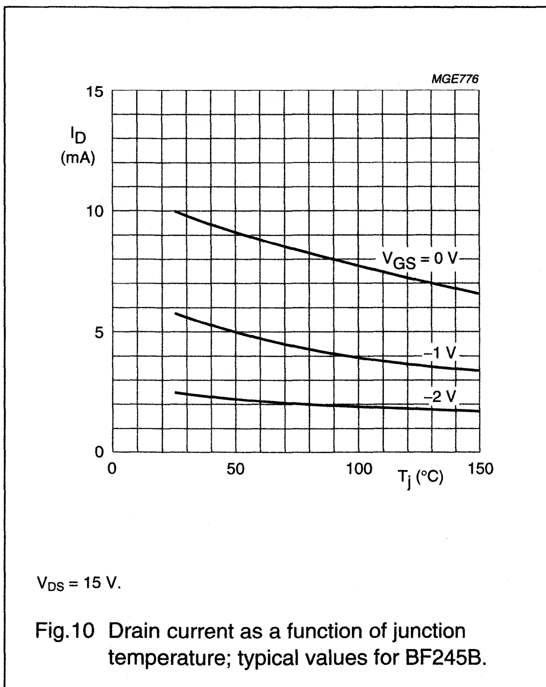
V_{DS} = 15 V; T_j = 25 °C.

Fig.8 Output characteristics for BF245C; typical values.



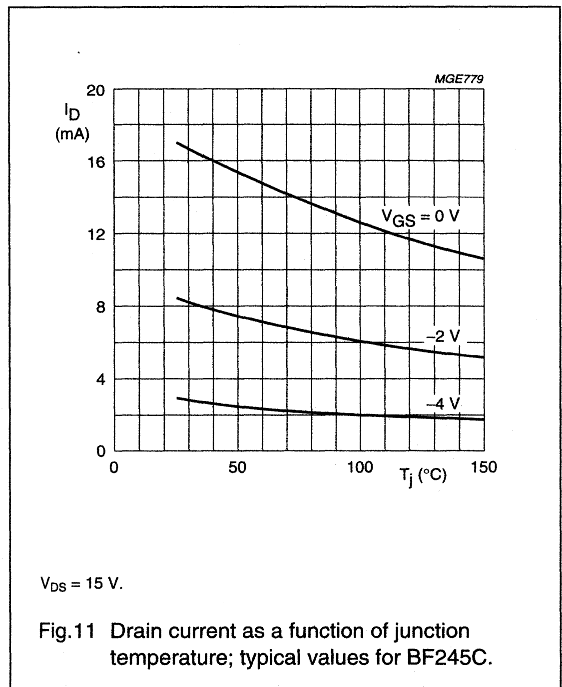
V_{DS} = 15 V.

Fig.9 Drain current as a function of junction temperature; typical values for BF245A.



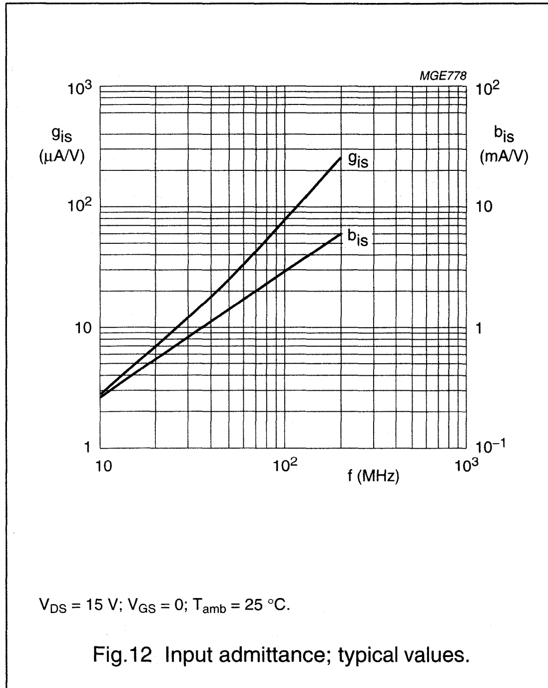
V_{DS} = 15 V.

Fig.10 Drain current as a function of junction temperature; typical values for BF245B.



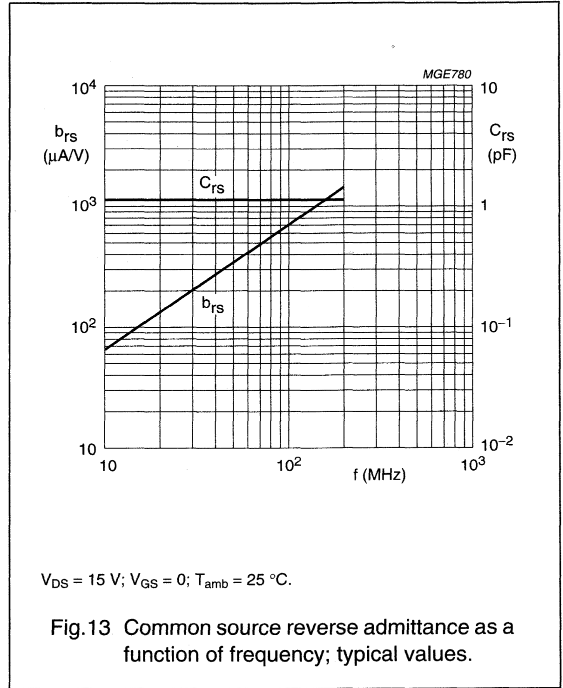
V_{DS} = 15 V.

Fig.11 Drain current as a function of junction temperature; typical values for BF245C.



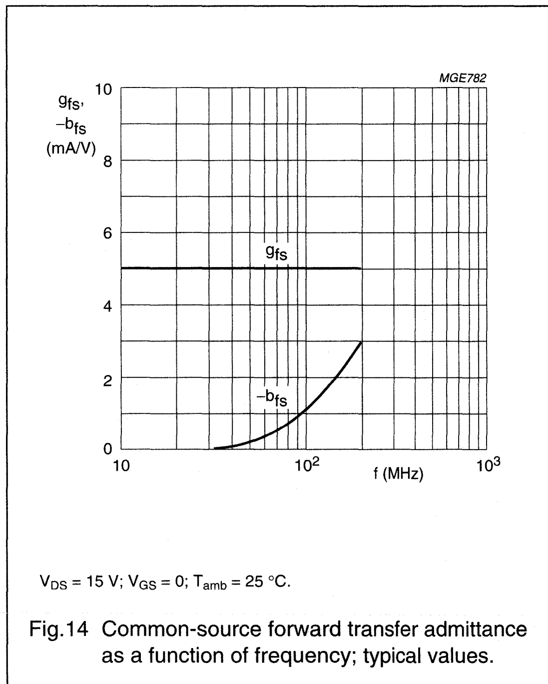
V_{DS} = 15 V; V_{GS} = 0; T_{amb} = 25 °C.

Fig.12 Input admittance; typical values.



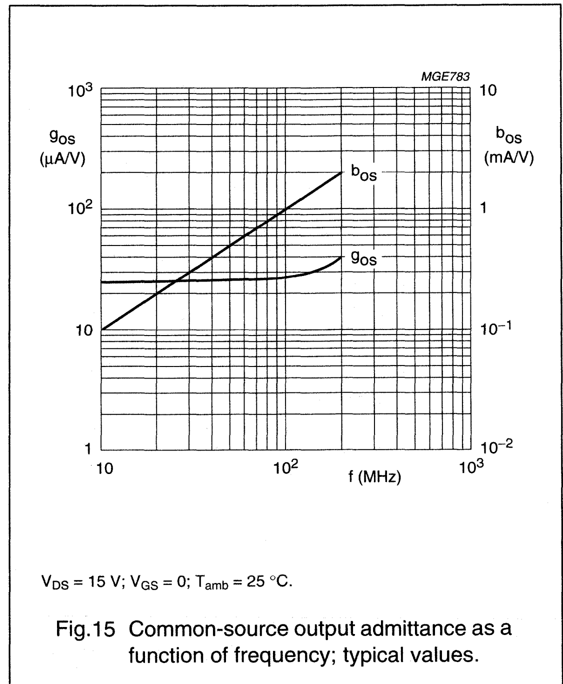
V_{DS} = 15 V; V_{GS} = 0; T_{amb} = 25 °C.

Fig.13 Common source reverse admittance as a function of frequency; typical values.



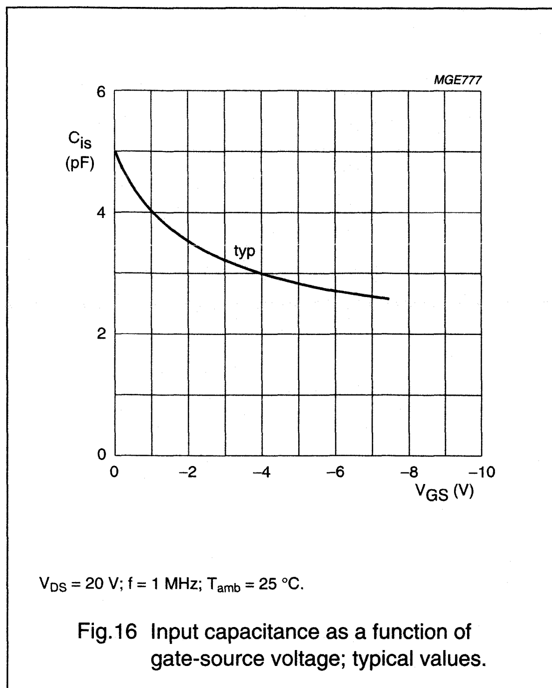
V_{DS} = 15 V; V_{GS} = 0; T_{amb} = 25 °C.

Fig.14 Common-source forward transfer admittance as a function of frequency; typical values.



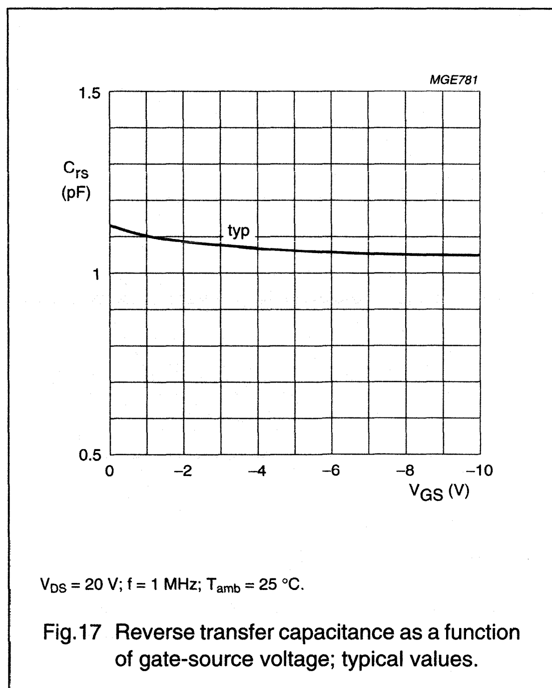
V_{DS} = 15 V; V_{GS} = 0; T_{amb} = 25 °C.

Fig.15 Common-source output admittance as a function of frequency; typical values.



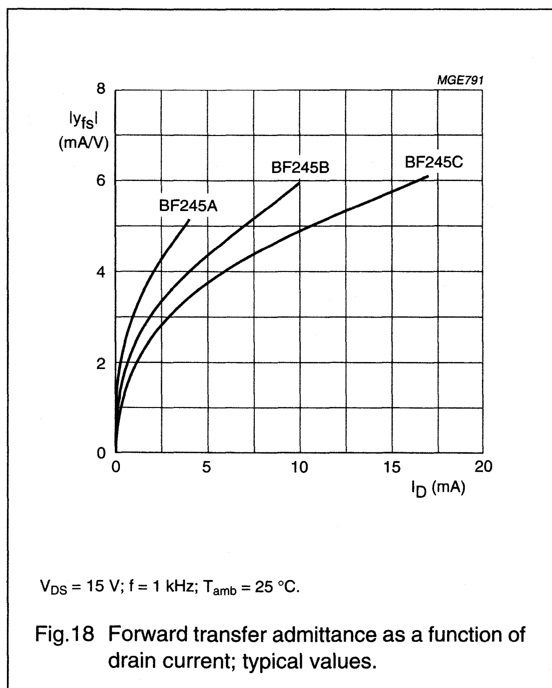
V_{DS} = 20 V; f = 1 MHz; T_{amb} = 25 °C.

Fig.16 Input capacitance as a function of gate-source voltage; typical values.



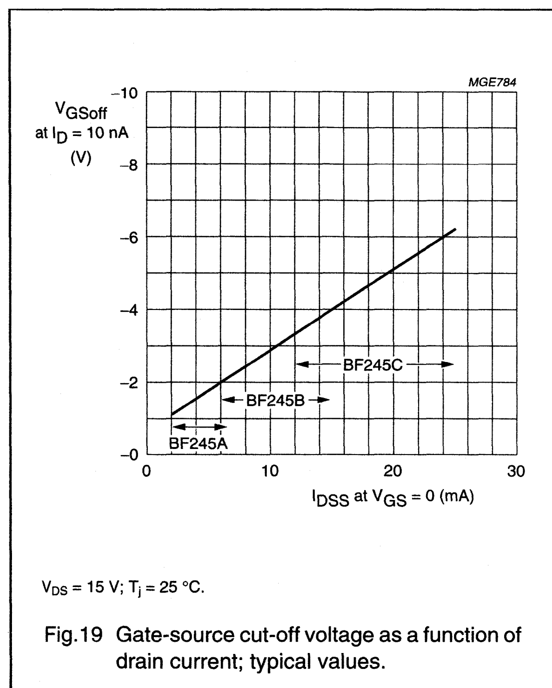
V_{DS} = 20 V; f = 1 MHz; T_{amb} = 25 °C.

Fig.17 Reverse transfer capacitance as a function of gate-source voltage; typical values.



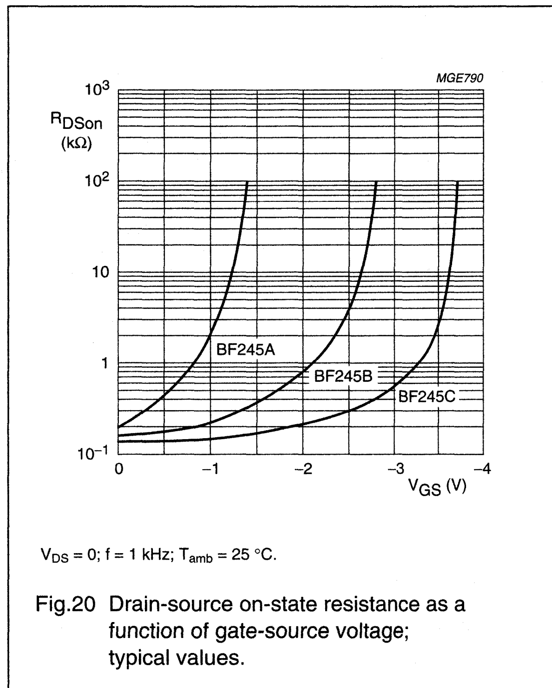
V_{DS} = 15 V; f = 1 kHz; T_{amb} = 25 °C.

Fig.18 Forward transfer admittance as a function of drain current; typical values.



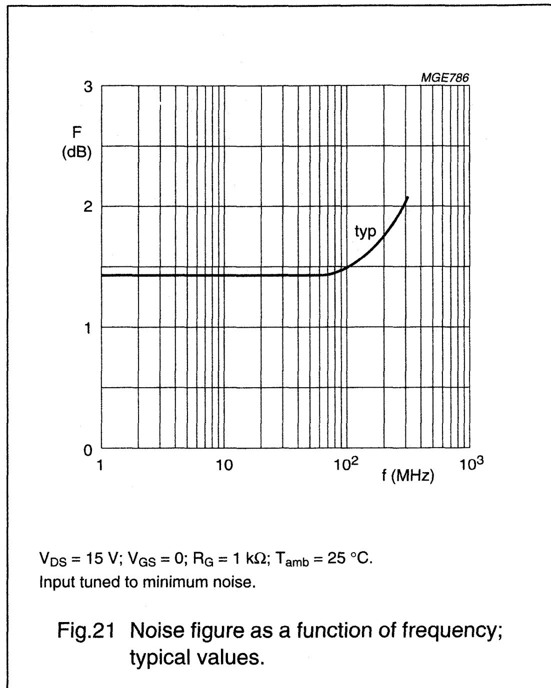
V_{DS} = 15 V; T_j = 25 °C.

Fig.19 Gate-source cut-off voltage as a function of drain current; typical values.



V_{DS} = 0; f = 1 kHz; T_{amb} = 25 °C.

Fig.20 Drain-source on-state resistance as a function of gate-source voltage; typical values.



V_{DS} = 15 V; V_{GS} = 0; R_G = 1 kΩ; T_{amb} = 25 °C.
Input tuned to minimum noise.

Fig.21 Noise figure as a function of frequency; typical values.

N-channel silicon field-effect transistors BF410A to D

DESCRIPTION

Asymmetrical N-channel planar epitaxial junction field-effect transistors in a plastic TO-92 variant; intended for applications up to the VHF range.

These FETs can be supplied in four I_{DSS} groups. Special features are the low feedback capacitance and the low noise figure. Thanks to these special features the BF410 is very suitable for applications such as the RF stages in FM portables (type A), car radios (type B) and mains radios (type C) or the mixer stage (type D).

PINNING - TO-92 VARIANT

1 = drain

2 = source

3 = gate

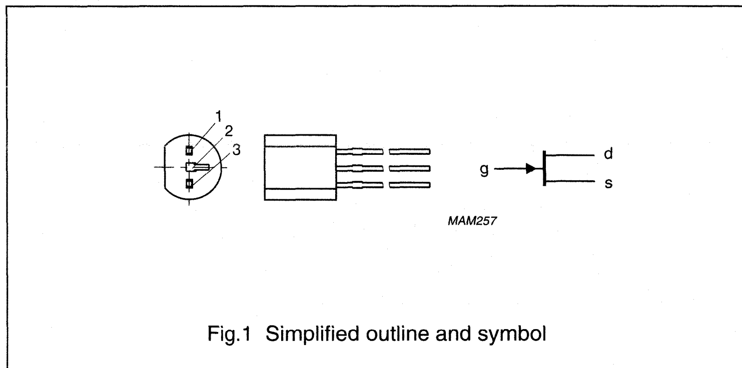


Fig.1 Simplified outline and symbol

QUICK REFERENCE DATA

Parameter	Symbol		BF410A	B	C	D	Unit
Drain-source voltage	V_{DS}	max.	20				V
Drain current (DC or average)	I_D	max.	30				mA
Total power dissipation up to T_{amb} = 75 °C	P_{tot}	max.	300				mW
Drain current V_{DS} = 10 V; V_{GS} = 0	I_{DSS}	min.	0.7	2.5	6	10	mA
		max.	3.0	7.0	12	18	mA
Transfer admittance V_{DS} = 10 V; V_{GS} = 0; f = 1 kHz	$\lvert y_{fs} \rvert$	min.	2.5	4	6	7	mS
Feedback capacitance V_{DS} = 10 V; V_{GS} = 0	C_{rs}	typ.	0.5	0.5	–	–	pF
V_{DS} = 10 V; I_D = 5 mA	C_{rs}	typ.	–	–	0.5	0.5	pF
Noise figure at optimum source admittance G_S = 1 mS; $-B_S$ = 3 mS; f = 100 MHz V_{DS} = 10 V; V_{GS} = 0	F	typ.	1.5	1.5	–	–	dB
V_{DS} = 10 V; I_D = 5 mA	F	typ.	–	–	1.5	1.5	dB

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20	V
Drain-gate voltage (open source)	V_{DGO}	max.	20	V
Drain current (DC or average)	I_D	max.	30	mA
Gate current	$\pm I_G$	max.	10	mA
Total power dissipation up to T_{amb} = 75 °C	P_{tot}	max.	300	mW
Storage temperature range	T_{stg}		−65 to +150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j\text{-}a}$	=	250	K/W

STATIC CHARACTERISTICS

T_{amb} = 25 °C

			BF410A	B	C	D	
Gate cut-off current $-V_{GS}$ = 0.2 V; V_{DS} = 0	$-I_{GSS}$	max.	10	10	10	10	nA
Gate-drain breakdown voltage I_S = 0; $-I_D$ = 10 μA	$-V_{(BR)GDO}$	min.	20	20	20	20	V
Drain current V_{DS} = 10 V; V_{GS} = 0	I_{DSS}	min.	0.7	2.5	6	10	mA
		max.	3.0	7.0	12	18	mA
Gate-source cut-off voltage I_D = 10 μA; V_{DS} = 10 V	$-V_{(P)GS}$	typ.	0.8	1.5	2.2	3	V

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): V_{DS} = 10 V; V_{GS} = 0; T_{amb} = 25 °C for BF410A and B
V_{DS} = 10 V; I_D = 5 mA; T_{amb} = 25 °C for BF410C and D

y-parameters (common source)			**BF410A**	**B**	**C**	**D**	
Input capacitance at f = 1 MHz	C_{is}	max.	5	5	5	5	pF
Input conductance at f = 100 MHz	g_{is}	typ.	100	90	60	50	μS
Feedback capacitance at f = 1 MHz	C_{rs}	typ.	0.5	0.5	0.5	0.5	pF
		max.	0.7	0.7	0.7	0.7	pF
Transfer admittance at f = 1 kHz	$\|y_{fs}\|$	min.	2.5	4.0	4.0	3.5	mS
V_{GS} = 0 instead of I_D = 5 mA	$\|y_{fs}\|$	min.	–	–	6.0	7.0	mS
Transfer admittance at f = 100 MHz	$\|y_{fs}\|$	typ.	3.5	5.5	5.0	5.0	mS
Output capacitance at f = 1 MHz	C_{os}	max.	3	3	3	3	pF
Output conductance at f = 1 MHz	g_{os}	max.	60	80	100	120	μS
Output conductance at f = 100 MHz	g_{os}	typ.	35	55	70	90	μS
Noise figure at optimum source admittance G_S = 1 mS; $-B_S$ = 3 mS; f = 100 MHz	F	typ.	1.5	1.5	1.5	1.5	dB

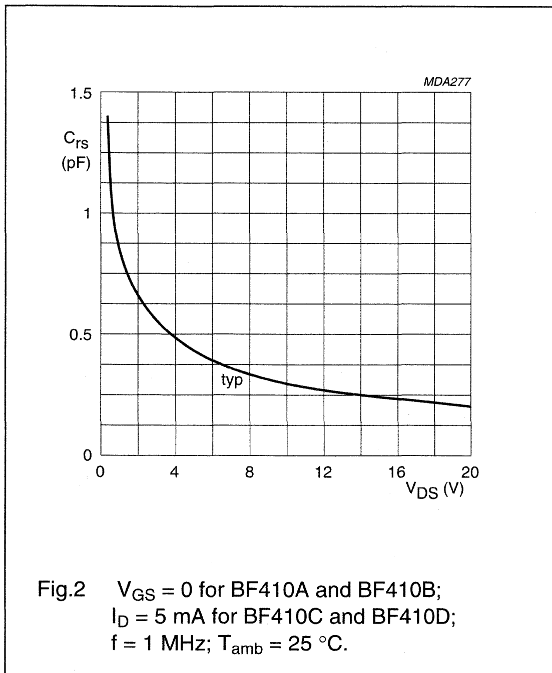


Fig.2 V_{GS} = 0 for BF410A and BF410B; I_D = 5 mA for BF410C and BF410D; f = 1 MHz; T_{amb} = 25 °C.

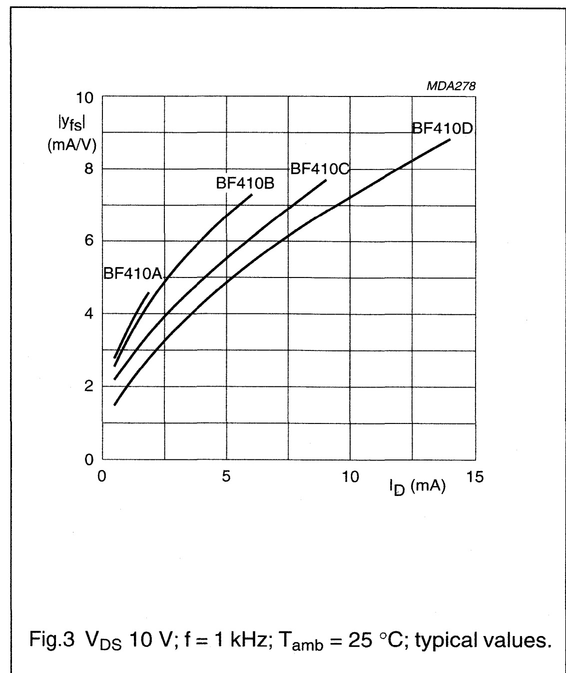


Fig.3 V_{DS} 10 V; f = 1 kHz; T_{amb} = 25 °C; typical values.

N-channel silicon field-effect transistors — BF510 to 513

DESCRIPTION

Asymmetrical N-channel planar epitaxial junction field-effect transistors in the miniature plastic envelope intended for applications up to the v.h.f. range in hybrid thick and thin-film circuits. Special features are the low feedback capacitance and the low noise figure. These features make the product very suitable for applications such as the r.f. stages in f.m. portables (BF510), car radios (BF511) and mains radios (BF512) or the mixer stage (BF513).

PINNING - SOT23

1 = gate
2 = drain
3 = source

MARKING CODE

BF510 = S6p
BF511 = S7p
BF512 = S8p
BF513 = S9p

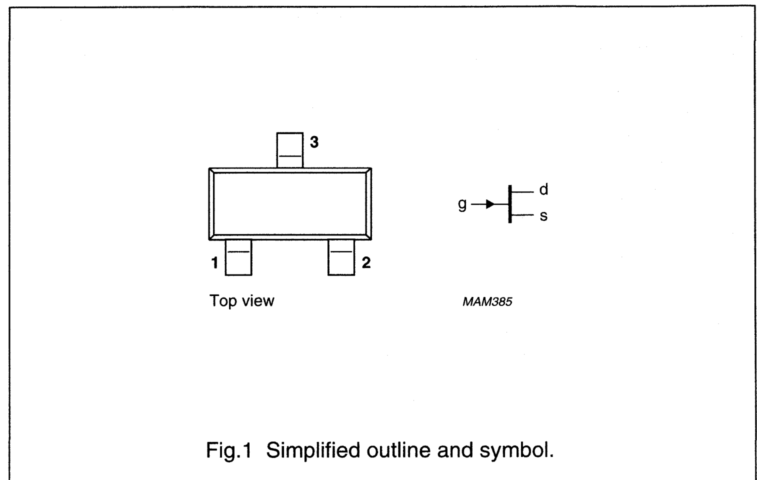


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.		20			V
Drain current (DC or average)	I_D	max.		30			mA
Total power dissipation up to T_{amb} = 40 °C	P_{tot}	max.		250			mW
			BF510	**511**	**512**	**513**	
Drain current		>	0.7	2.5	6	10	mA
V_{DS} = 10 V; V_{GS} = 0	I_{DSS}	<	3.0	7.0	12	18	mA
Transfer admittance (common source) V_{DS} = 10 V; V_{GS} = 0; f = 1 kHz	$\|y_{fs}\|$	>	2.5	4	6	7	mS
Feedback capacitance							
V_{DS} = 10 V; V_{GS} = 0	C_{rs}	typ.	0.3	0.3	–	–	pF
V_{DS} = 10 V; I_D = 5 mA	C_{rs}	typ.	–	–	0.3	0.3	pF
Noise figure at optimum source admittance G_S = 1 mS; $-B_S$ = 3 mS; f = 100 MHz							
V_{DS} = 10 V; V_{GS} = 0	F	typ.	1.5	1.5	–	–	dB
V_{DS} = 10 V; I_D = 5 mA	F	typ.	–	–	1.5	1.5	dB

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20	V
Drain-gate voltage (open source)	V_{DGO}	max.	20	V
Drain current (DC or average)	I_D	max.	30	mA
Gate current	$\pm I_G$	max.	10	mA
Total power dissipation up to T_{amb} = 40 °C (note 1)	P_{tot}	max.	250	mW
Storage temperature range	T_{stg}	−65 to + 150		°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	430	K/W

Note

1. Mounted on a ceramic substrate of 8 mm × 10 mm × 0.7 mm.

STATIC CHARACTERISTICS

T_{amb} = 25 °C

			BF510	511	512	513	
Gate cut-off current							
$-V_{GS}$ = 0.2 V; V_{DS} = 0	$-I_{GSS}$	<	10	10	10	10	nA
Gate-drain breakdown voltage							
I_S = 0; $-I_D$ = 10 μA	$-V_{(BR)GDO}$	>	20	20	20	20	V
Drain current							
V_{DS} = 10 V; V_{GS} = 0	I_{DSS}	>	0.7	2.5	6	10	mA
		<	3.0	7.0	12	18	mA
Gate-source cut-off voltage							
I_D = 10 μA; V_{DS} = 10 V	$-V_{(P)GS}$	typ.	0.8	1.5	2.2	3	V

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): V_{DS} = 10 V; V_{GS} = 0; T_{amb} = 25 °C for BF510 and BF511
V_{DS} = 10 V; I_D = 5 mA; T_{amb} = 25 °C for BF512 and BF513

y-parameters (common source)			BF510	511	512	513	
Input capacitance at f = 1 MHz	C_{is}	<	5	5	5	5	pF
Input conductance at f = 100 MHz	g_{is}	typ.	100	90	60	50	µS
Feedback capacitance at f = 1 MHz	C_{rs}	typ.	0.4	0.4	0.4	0.4	pF
		<	0.5	0.5	0.5	0.5	pF
Transfer admittance at f = 1 kHz	$\lvert y_{fs} \rvert$	>	2.5	4.0	4.0	3.5	mS
V_{GS} = 0 instead of I_D = 5 mA	$\lvert y_{fs} \rvert$	>	–	–	6.0	7.0	mS
Transfer admittance at f = 100 MHz	$\lvert y_{fs} \rvert$	typ.	3.5	5.5	5.0	5.0	mS
Output capacitance at f = 1 MHz	C_{os}	<	3	3	3	3	pF
Output conductance at f = 1 MHz	g_{os}	<	60	80	100	120	µS
Output conductance at f = 100 MHz	g_{os}	typ.	35	55	70	90	µS
Noise figure at optimum source admittance G_S = 1 mS; $-B_S$ = 3 mS; f = 100 MHz	F	typ.	1.5	1.5	1.5	1.5	dB

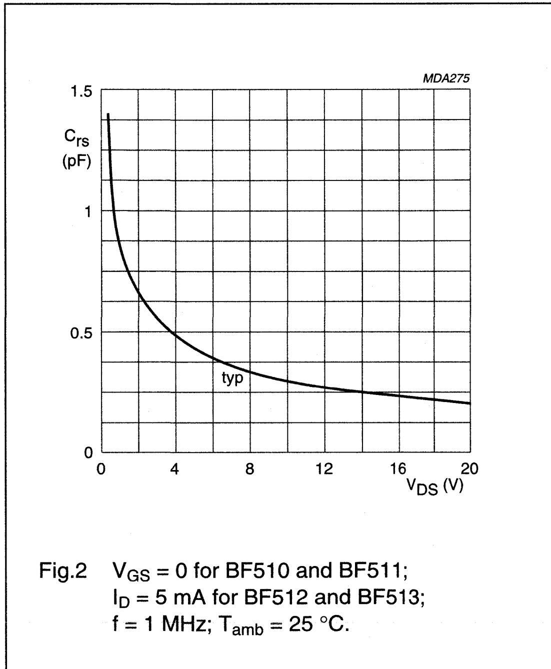


Fig.2 V_{GS} = 0 for BF510 and BF511; I_D = 5 mA for BF512 and BF513; f = 1 MHz; T_{amb} = 25 °C.

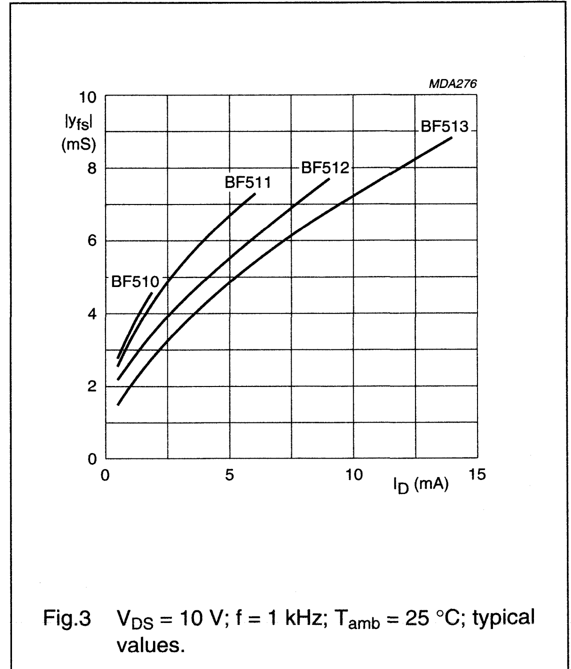


Fig.3 V_{DS} = 10 V; f = 1 kHz; T_{amb} = 25 °C; typical values.

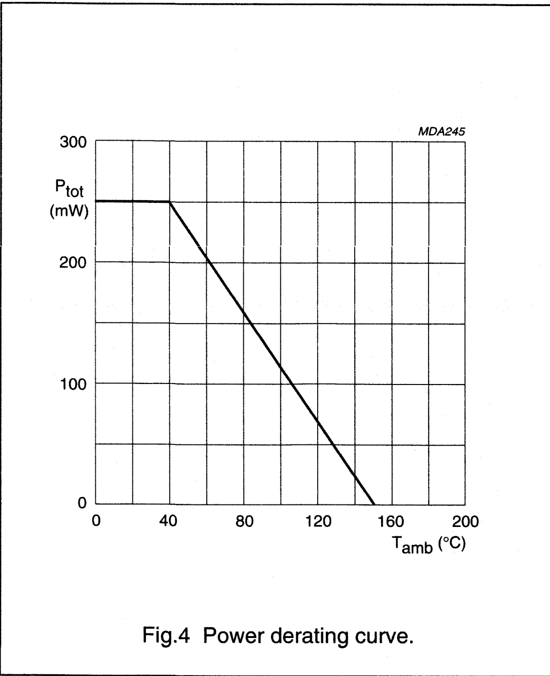


Fig.4 Power derating curve.

N-channel silicon junction field-effect transistors

BF545A; BF545B; BF545C

FEATURES

- Low leakage level (typ. 500 fA)
- High gain
- Low cut-off voltage (max. 2.2 V for BF545A).

APPLICATIONS

- Impedance converters in e.g. electret microphones and infra-red detectors
- VHF amplifiers in oscillators and mixers.

DESCRIPTION

N-channel symmetrical silicon junction field-effect transistors in a SOT23 package.

PINNING - SOT23

PIN	SYMBOL	DESCRIPTION
1	s	source
2	d	drain
3	g	gate

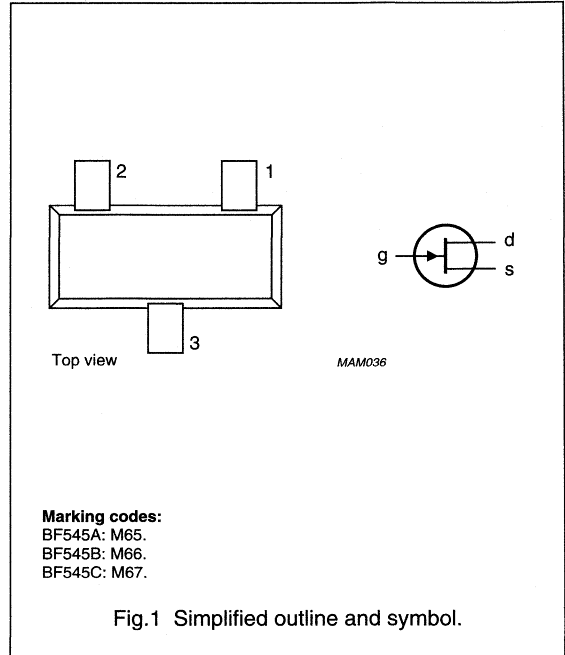


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	±30	V
V_{GSoff}	gate-source cut-off voltage	I_D = 1 μA; V_{DS} = 15 V	–0.4	–7.8	V
I_{DSS}	drain current	V_{GS} = 0; V_{DS} = 15 V			
	BF545A		2	6.5	mA
	BF545B		6	15	mA
	BF545C		12	25	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C	–	250	mW
$\lvert y_{fs} \rvert$	forward transfer admittance	V_{GS} = 0; V_{DS} = 15 V	3	6.5	mS

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	±30	V
V_{GSO}	gate-source voltage	open drain	–	–30	V
V_{GDO}	gate-drain voltage (DC)	open source	–	–30	V
I_G	forward gate current (DC)		–	10	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C; note 1	–	250	mW
T_{stg}	storage temperature		–65	150	°C
T_j	operating junction temperature		–	150	°C

Note

1. Device mounted on an FR4 printed-circuit board, maximum lead length 4 mm; mounting pad for the drain lead 10 mm^2.

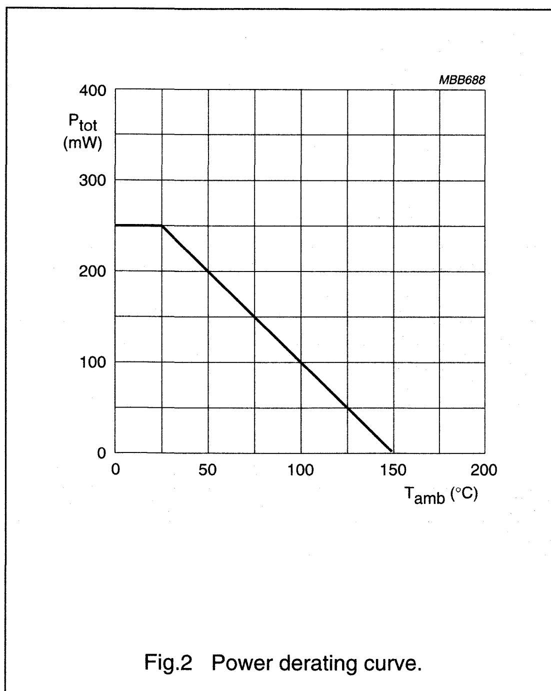


Fig.2 Power derating curve.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient; note 1	500	K/W

Note

1. Device mounted on an FR4 printed-circuit board, maximum lead length 4 mm; mounting pad for the drain lead 10 mm^2.

STATIC CHARACTERISTICS

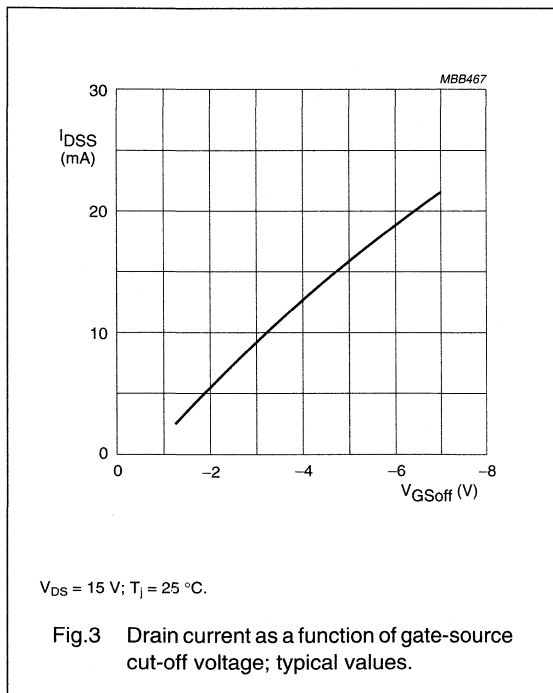
T_j = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)GSS}$	gate-source breakdown voltage	I_G = −1 μA; V_{DS} = 0	−30	−	−	V
V_{GSoff}	gate-source cut-off voltage	I_D = 200 μA; V_{DS} = 15 V				
	BF545A		−0.4	−	−2.2	V
	BF545B		−1.6	−	−3.8	V
	BF545C		−3.2	−	−7.8	V
		I_D = 1 μA; V_{DS} = 15 V	−0.4	−	−7.5	V
I_{DSS}	drain current	V_{GS} = 0; V_{DS} = 15 V				
	BF545A		2	−	6.5	mA
	BF545B		6	−	15	mA
	BF545C		12	−	25	mA
I_{GSS}	gate leakage current	V_{GS} = −20 V; V_{DS} = 0	−	−0.5	−1000	pA
		V_{GS} = −20 V; V_{DS} = 0; T_j = 125 °C	−	−	−100	nA
$\lvert y_{fs} \rvert$	forward transfer admittance	V_{GS} = 0; V_{DS} = 15 V	3	−	6.5	mS
$\lvert y_{os} \rvert$	common source output admittance	V_{GS} = 0; V_{DS} = 15 V	−	40	−	μS

DYNAMIC CHARACTERISTICS

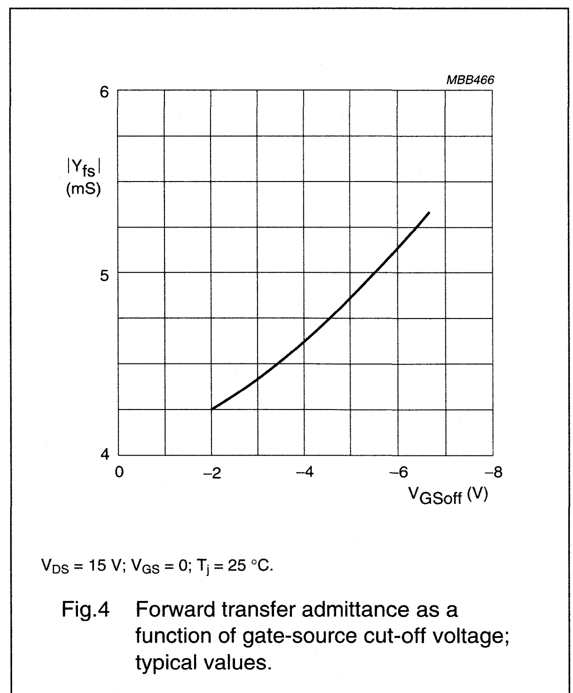
T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	TYP.	UNIT
C_{is}	input capacitance	V_{DS} = 15 V; V_{GS} = −10 V; f = 1 MHz	1.7	pF
		V_{DS} = 15 V; V_{GS} = 0; f = 1 MHz	3	pF
C_{rs}	reverse transfer capacitance	V_{DS} = 15 V; V_{GS} = −10 V; f = 1 MHz	0.8	pF
		V_{DS} = 15 V; V_{GS} = 0; f = 1 MHz	0.9	pF
g_{is}	common source input conductance	V_{DS} = 10 V; I_D = 1 mA; f = 100 MHz	15	μS
		V_{DS} = 10 V; I_D = 1 mA; f = 450 MHz	300	μS
g_{fs}	common source transfer conductance	V_{DS} = 10 V; I_D = 1 mA; f = 100 MHz	2	mS
		V_{DS} = 10 V; I_D = 1 mA; f = 450 MHz	1.8	mS
g_{rs}	common source reverse conductance	V_{DS} = 10 V; I_D = 1 mA; f = 100 MHz	−6	μS
		V_{DS} = 10 V; I_D = 1 mA; f = 450 MHz	−40	μS
g_{os}	common source output conductance	V_{DS} = 10 V; I_D = 1 mA; f = 100 MHz	30	μS
		V_{DS} = 10 V; I_D = 1 mA; f = 450 MHz	60	μS



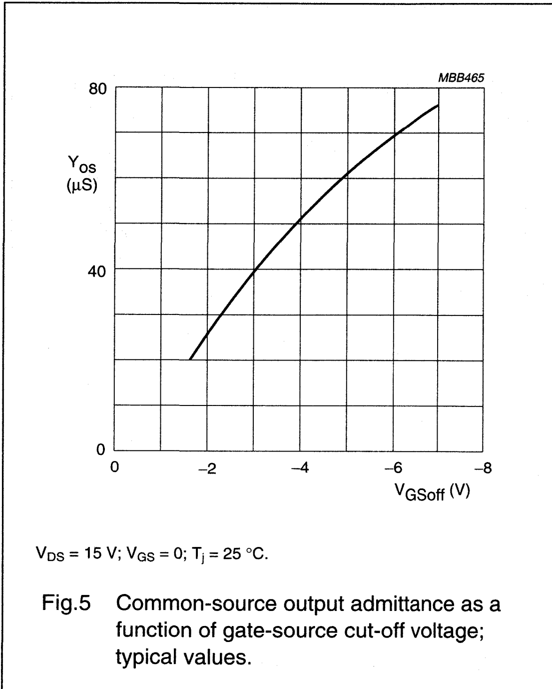
V_{DS} = 15 V; T_j = 25 °C.

Fig.3 Drain current as a function of gate-source cut-off voltage; typical values.



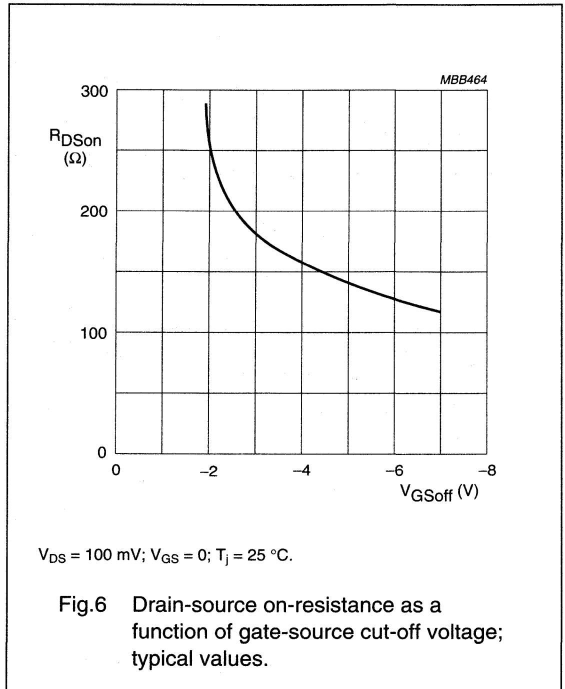
V_{DS} = 15 V; V_{GS} = 0; T_j = 25 °C.

Fig.4 Forward transfer admittance as a function of gate-source cut-off voltage; typical values.



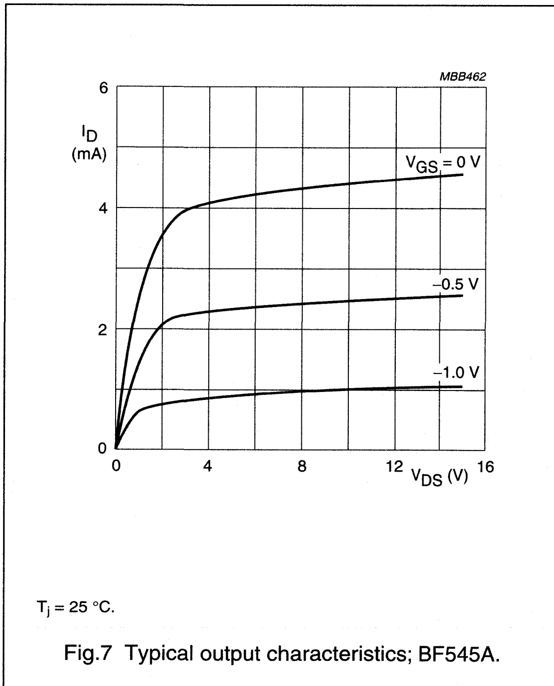
V_{DS} = 15 V; V_{GS} = 0; T_j = 25 °C.

Fig.5 Common-source output admittance as a function of gate-source cut-off voltage; typical values.



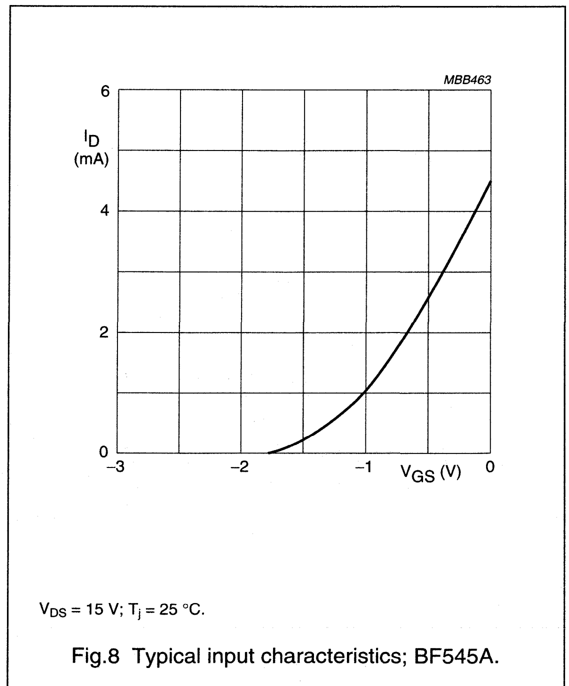
V_{DS} = 100 mV; V_{GS} = 0; T_j = 25 °C.

Fig.6 Drain-source on-resistance as a function of gate-source cut-off voltage; typical values.



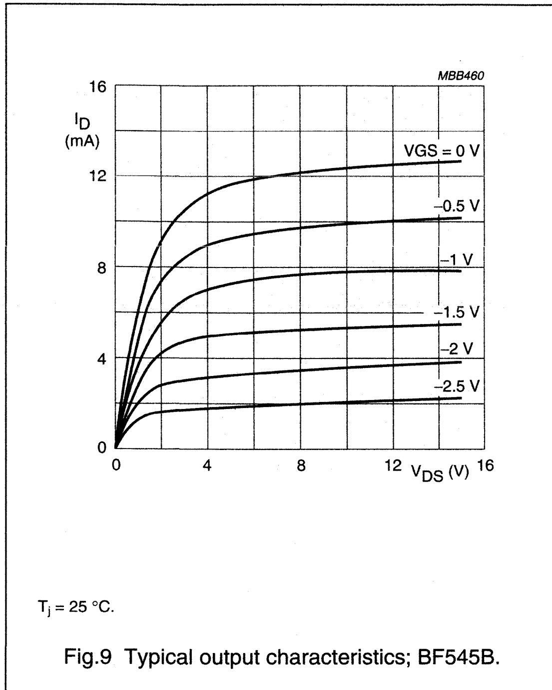
T_j = 25 °C.

Fig.7 Typical output characteristics; BF545A.



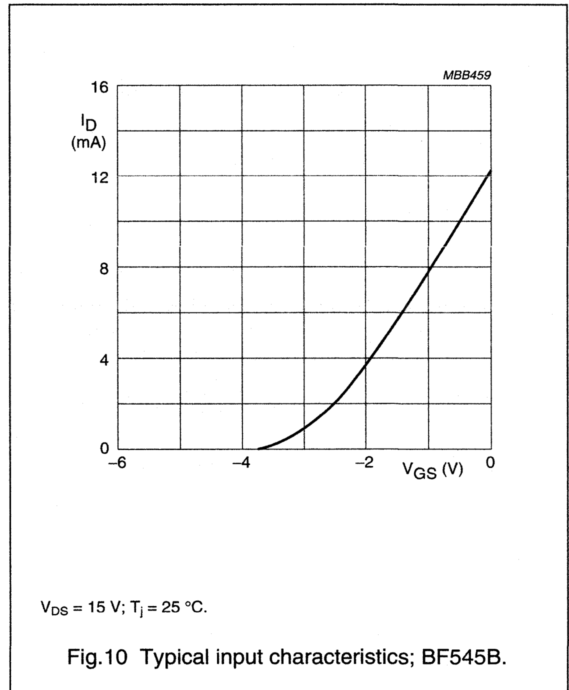
V_{DS} = 15 V; T_j = 25 °C.

Fig.8 Typical input characteristics; BF545A.



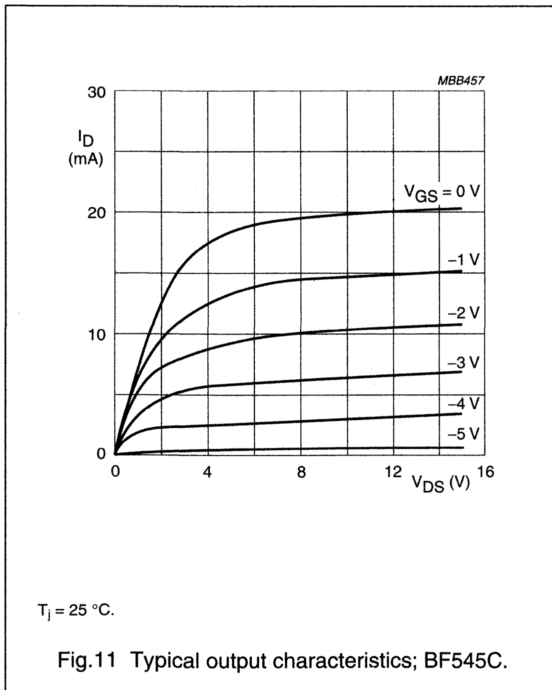
T_j = 25 °C.

Fig.9 Typical output characteristics; BF545B.



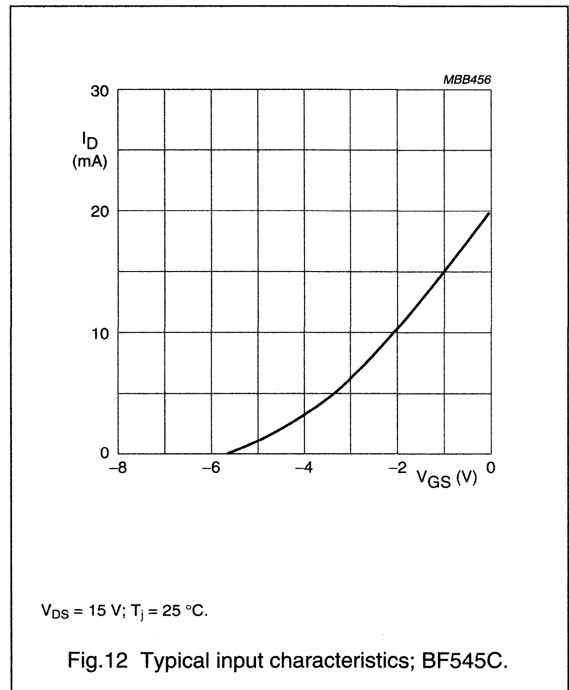
V_{DS} = 15 V; T_j = 25 °C.

Fig.10 Typical input characteristics; BF545B.



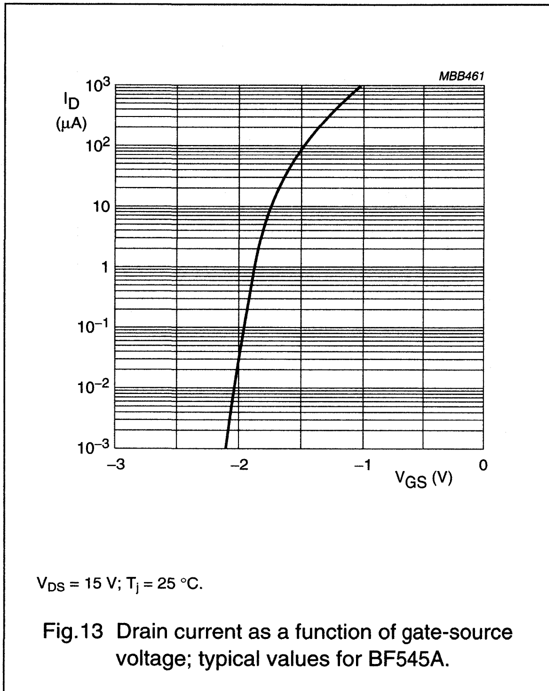
T_j = 25 °C.

Fig.11 Typical output characteristics; BF545C.



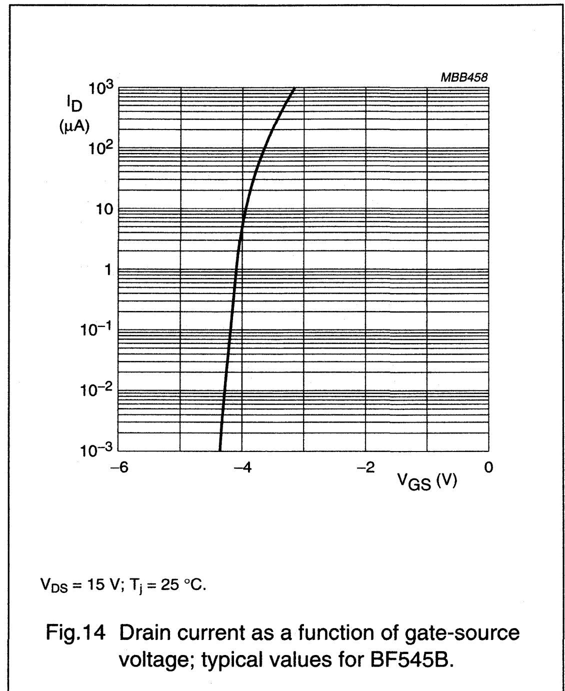
V_{DS} = 15 V; T_j = 25 °C.

Fig.12 Typical input characteristics; BF545C.



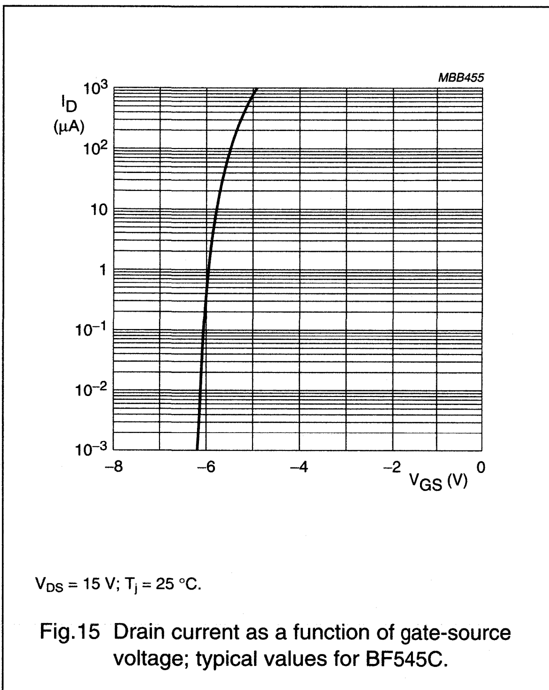
V_{DS} = 15 V; T_j = 25 °C.

Fig.13 Drain current as a function of gate-source voltage; typical values for BF545A.



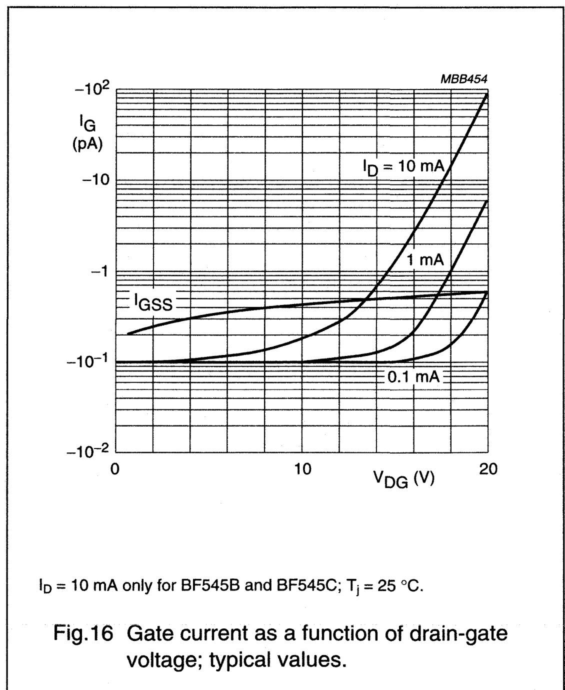
V_{DS} = 15 V; T_j = 25 °C.

Fig.14 Drain current as a function of gate-source voltage; typical values for BF545B.



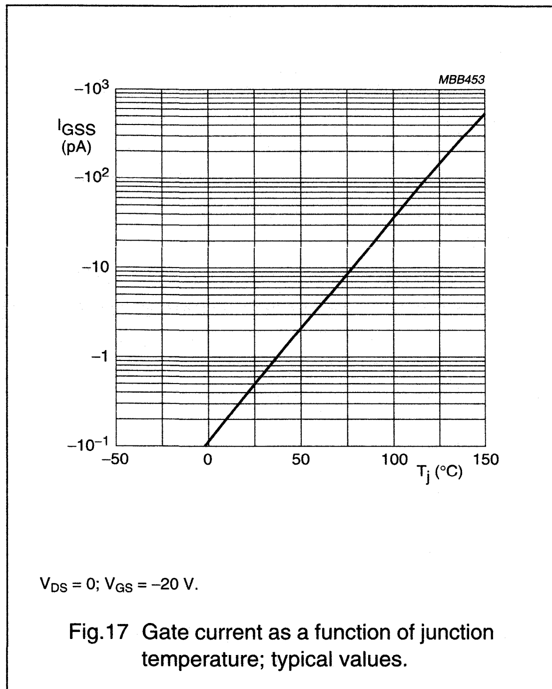
V_{DS} = 15 V; T_j = 25 °C.

Fig.15 Drain current as a function of gate-source voltage; typical values for BF545C.



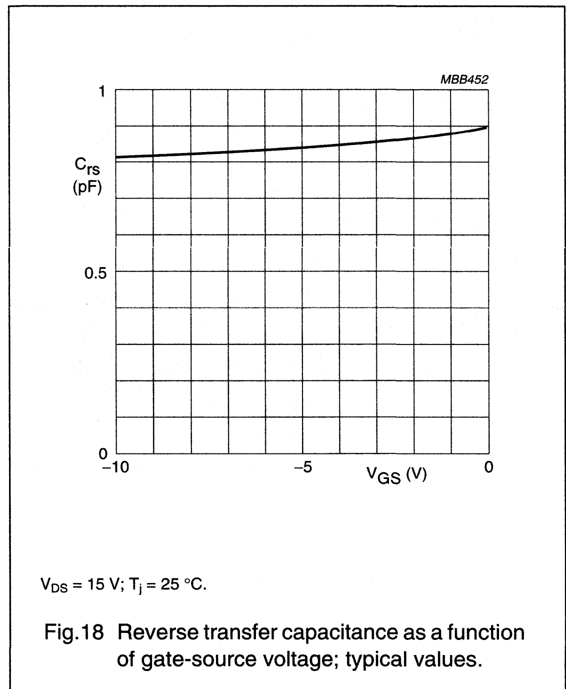
I_D = 10 mA only for BF545B and BF545C; T_j = 25 °C.

Fig.16 Gate current as a function of drain-gate voltage; typical values.



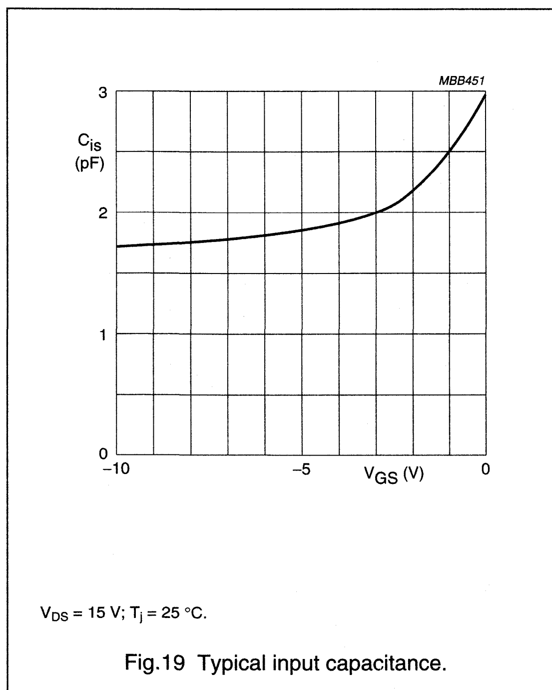
$V_{DS} = 0$; $V_{GS} = -20$ V.

Fig.17 Gate current as a function of junction temperature; typical values.



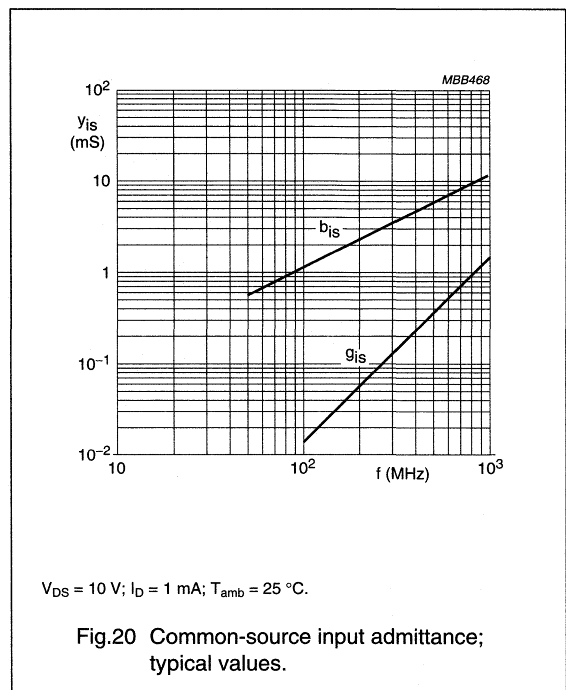
$V_{DS} = 15$ V; $T_j = 25$ °C.

Fig.18 Reverse transfer capacitance as a function of gate-source voltage; typical values.



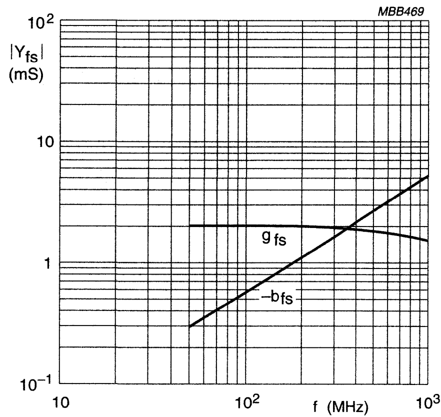
$V_{DS} = 15$ V; $T_j = 25$ °C.

Fig.19 Typical input capacitance.



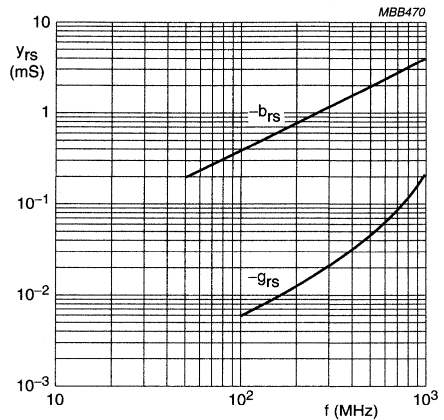
$V_{DS} = 10$ V; $I_D = 1$ mA; $T_{amb} = 25$ °C.

Fig.20 Common-source input admittance; typical values.



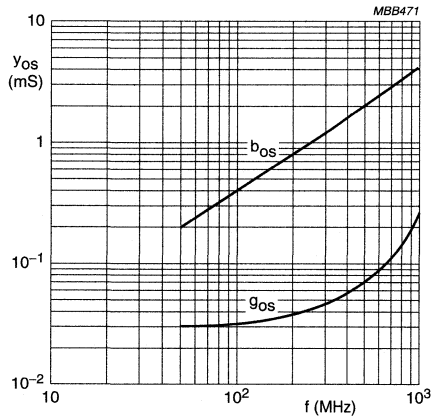
V_{DS} = 10 V; I_D = 1 mA; T_{amb} = 25 °C.

Fig.21 Common-source forward transfer admittance; typical values.



V_{DS} = 10 V; I_D = 1 mA; T_{amb} = 25 °C.

Fig.22 Common-source reverse transfer admittance; typical values.



V_{DS} = 10 V; I_D = 1 mA; T_{amb} = 25 °C.

Fig.23 Common-source output admittance; typical values.

N-channel silicon junction field-effect transistors

BF556A; BF556B; BF556C

FEATURES

- Low leakage level (typ. 500 fA)
- High gain
- Low cut-off voltage.

APPLICATIONS

- Impedance converters in e.g. electret microphones and infra-red detectors
- VHF amplifiers in oscillators and mixers.

DESCRIPTION

N-channel symmetrical silicon junction field-effect transistors in a SOT23 package.

PINNING - SOT23

PIN	SYMBOL	DESCRIPTION
1	s	source
2	d	drain
3	g	gate'

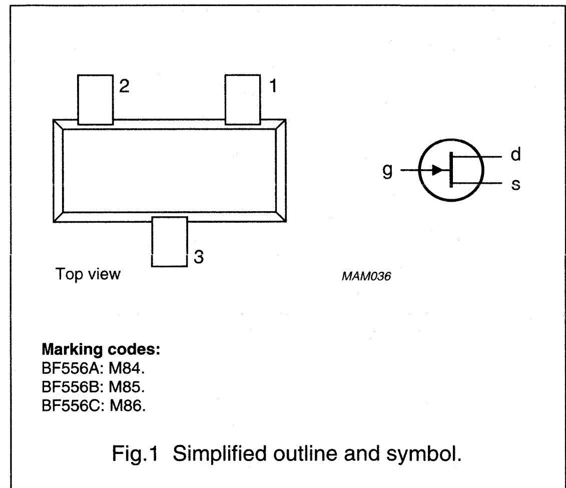


Fig.1 Simplified outline and symbol.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	±30	V
V_{GSoff}	gate-source cut-off voltage	I_D = 200 μA; V_{DS} = 15 V	–0.5	–7.5	V
I_{DSS}	drain current	V_{GS} = 0; V_{DS} = 15 V			
	BF556A		3	7	mA
	BF556B		6	13	mA
	BF556C		11	18	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C	–	250	mW
$\lvert y_{fs} \rvert$	forward transfer admittance	V_{GS} = 0; V_{DS} = 15 V	4.5	–	mS

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	±30	V
V_{GSO}	gate-source voltage	open drain	–	–30	V
V_{GDO}	gate-drain voltage (DC)	open source	–	–30	V
I_G	forward gate current (DC)		–	10	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C; note 1	–	250	mW
T_{stg}	storage temperature		–65	150	°C
T_j	operating junction temperature		–	150	°C

Note

1. Device mounted on an FR4 printed-circuit board, maximum lead length 4 mm; mounting pad for the drain lead 10 mm^2.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient; note 1	500	K/W

Note

1. Device mounted on an FR4 printed-circuit board, maximum lead length 4 mm; mounting pad for the drain lead 10 mm^2.

STATIC CHARACTERISTICS

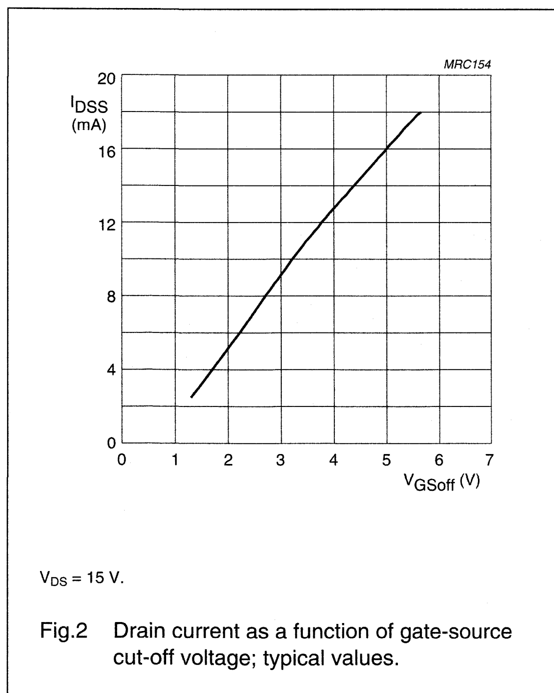
T_j = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)GSS}$	gate-source breakdown voltage	I_G = –1 µA; V_{DS} = 0	–30	–	–	V
V_{GSoff}	gate-source cut-off voltage	I_D = 200 µA; V_{DS} = 15 V	–0.5		–7.5	V
I_{DSS}	drain current	V_{GS} = 0; V_{DS} = 15 V				
	BF556A		3	–	7	mA
	BF556B		6	–	13	mA
	BF556C		11	–	18	mA
I_{GSS}	gate leakage current	V_{GS} = –20 V; V_{DS} = 0	–	–0.5	–5000	pA
$\|y_{fs}\|$	forward transfer admittance	V_{GS} = 0; V_{DS} = 15 V	4.5	–	–	mS
$\|y_{os}\|$	common source output admittance	V_{GS} = 0; V_{DS} = 15 V	–	40	–	µS

DYNAMIC CHARACTERISTICS

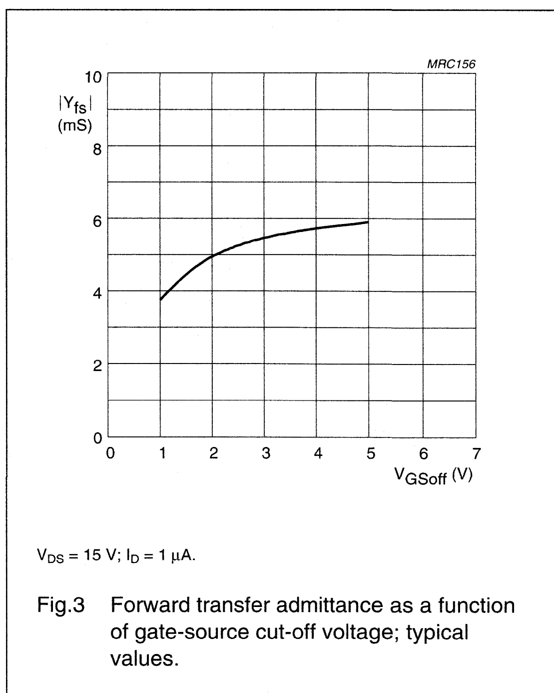
T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	TYP.	UNIT
C_{is}	input capacitance	V_{DS} = 15 V; V_{GS} = −10 V; f = 1 MHz	1.7	pF
		V_{DS} = 15 V; V_{GS} = 0; f = 1 MHz	3	pF
C_{rs}	reverse transfer capacitance	V_{DS} = 15 V; V_{GS} = −10 V; f = 1 MHz	0.8	pF
		V_{DS} = 15 V; V_{GS} = 0; f = 1 MHz	0.9	pF
g_{is}	common source input conductance	V_{DS} = 10 V; I_D = 1 mA; f = 100 MHz	15	µS
		V_{DS} = 10 V; I_D = 1 mA; f = 450 MHz	300	µS
g_{fs}	common source transfer conductance	V_{DS} = 10 V; I_D = 1 mA; f = 100 MHz	2	mS
		V_{DS} = 10 V; I_D = 1 mA; f = 450 MHz	1.8	mS
g_{rs}	common source reverse conductance	V_{DS} = 10 V; I_D = 1 mA; f = 100 MHz	−6	µS
		V_{DS} = 10 V; I_D = 1 mA; f = 450 MHz	−40	µS
g_{os}	common source output conductance	V_{DS} = 10 V; I_D = 1 mA; f = 100 MHz	30	µS
		V_{DS} = 10 V; I_D = 1 mA; f = 450 MHz	60	µS
V_n	equivalent input noise voltage	V_{DS} = 10 V; I_D = 1 mA; f = 100 Hz	40	nV/√Hz



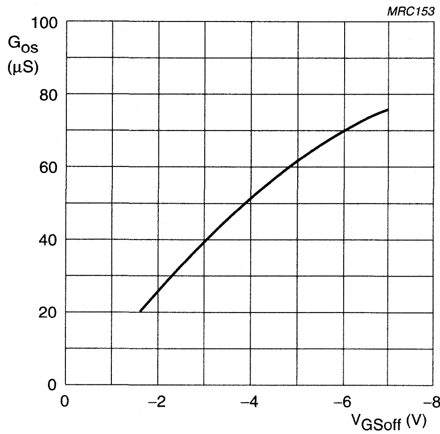
V_{DS} = 15 V.

Fig.2 Drain current as a function of gate-source cut-off voltage; typical values.



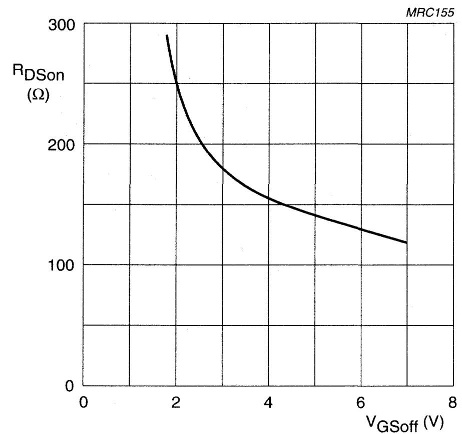
V_{DS} = 15 V; I_D = 1 µA.

Fig.3 Forward transfer admittance as a function of gate-source cut-off voltage; typical values.



V_{DS} = 15 V.

Fig.4 Common-source output conductance as a function of gate-source cut-off voltage; typical values.



V_{DS} = 100 mV; V_{GS} = 0.

Fig.5 Drain-source on-state resistance as a function of gate-source cut-off voltage; typical values.

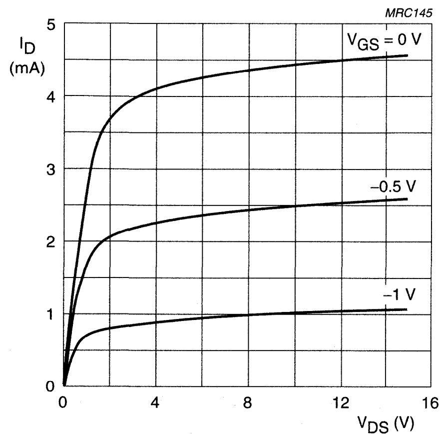


Fig.6 Typical output characteristics; BF556A.

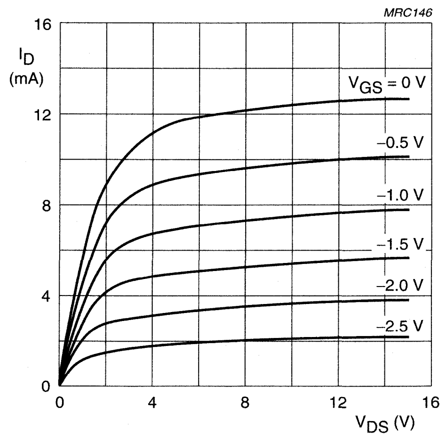


Fig.7 Typical output characteristics; BF556B.

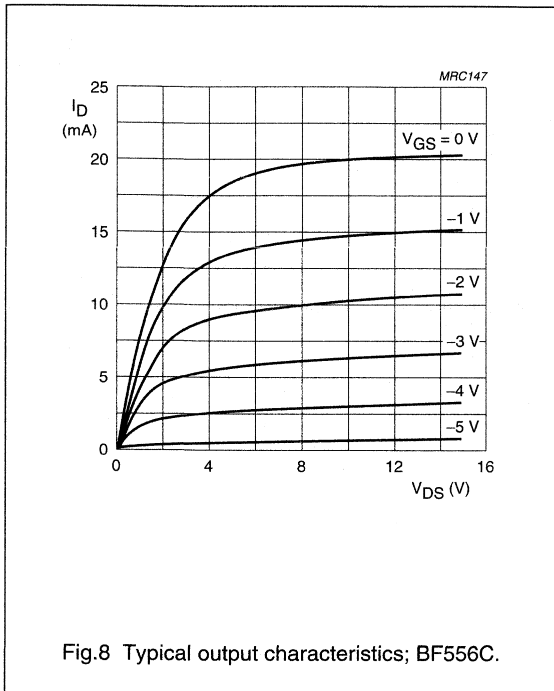
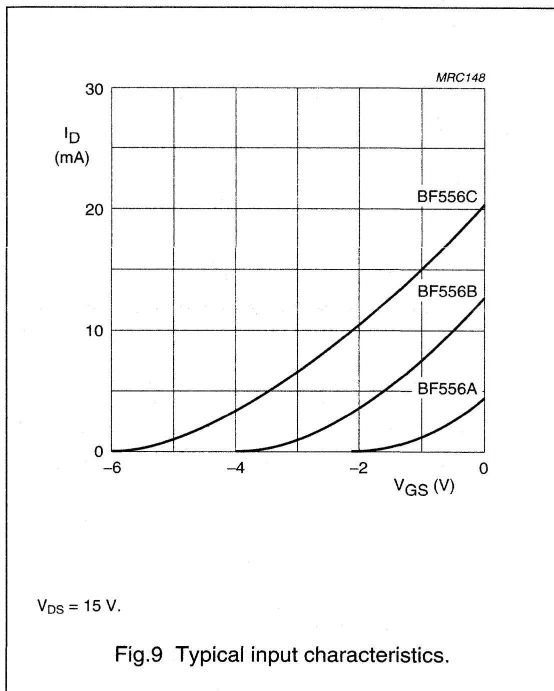
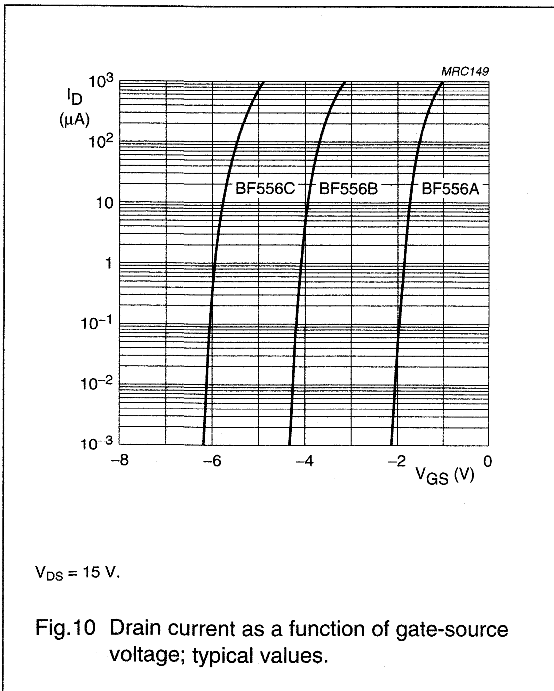


Fig.8 Typical output characteristics; BF556C.



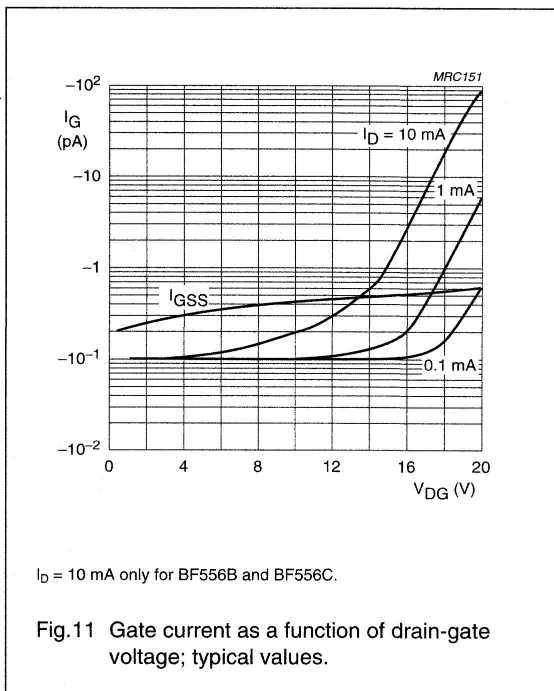
V_{DS} = 15 V.

Fig.9 Typical input characteristics.



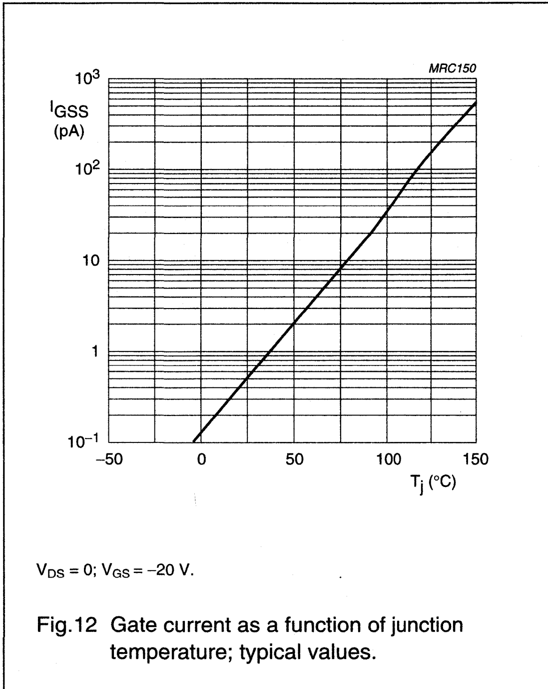
V_{DS} = 15 V.

Fig.10 Drain current as a function of gate-source voltage; typical values.



I_D = 10 mA only for BF556B and BF556C.

Fig.11 Gate current as a function of drain-gate voltage; typical values.



$V_{DS} = 0$; $V_{GS} = -20$ V.

Fig.12 Gate current as a function of junction temperature; typical values.

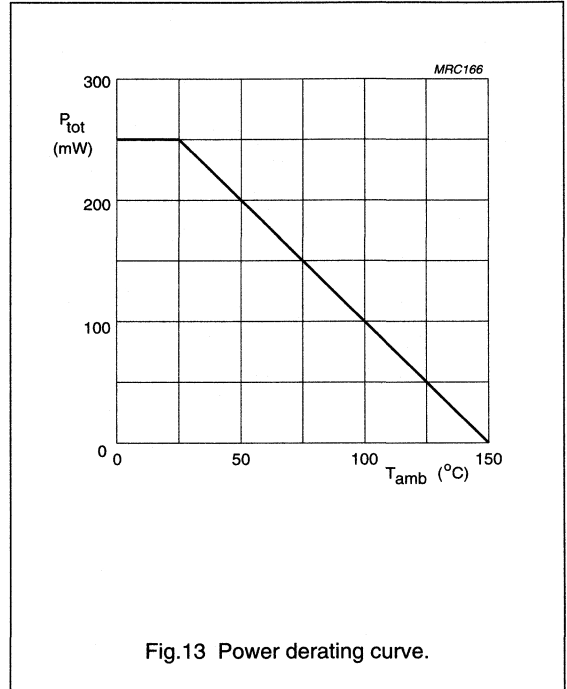
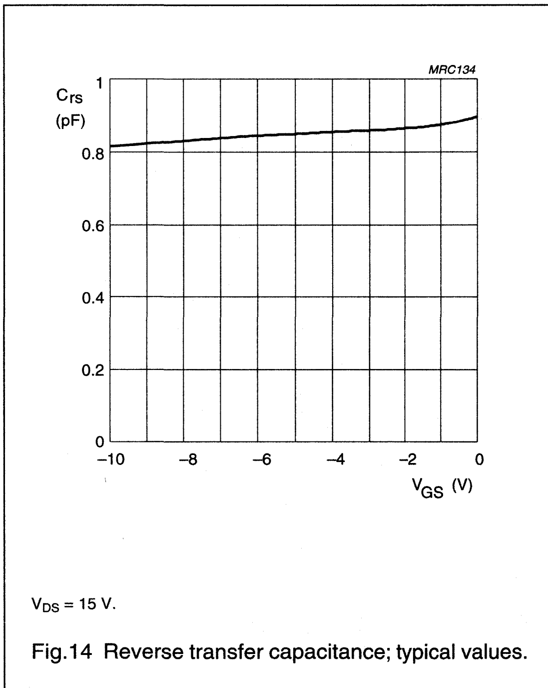
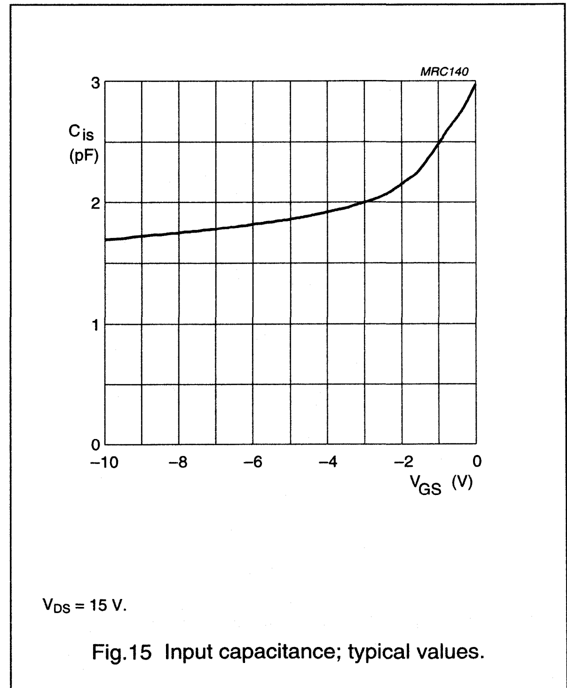


Fig.13 Power derating curve.



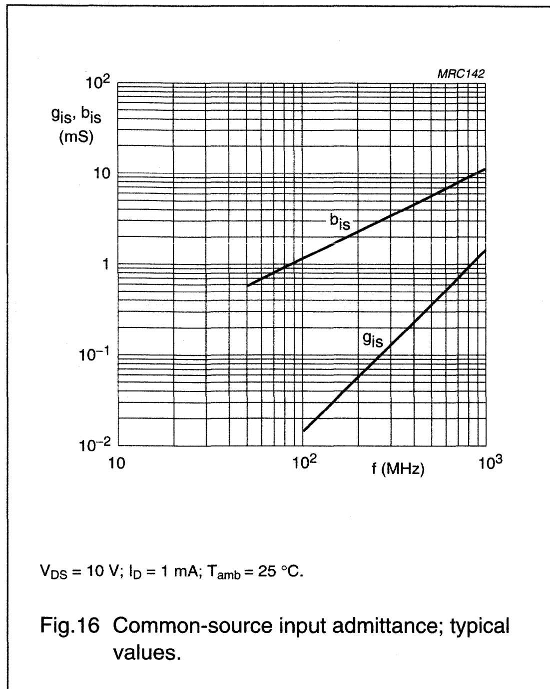
$V_{DS} = 15$ V.

Fig.14 Reverse transfer capacitance; typical values.



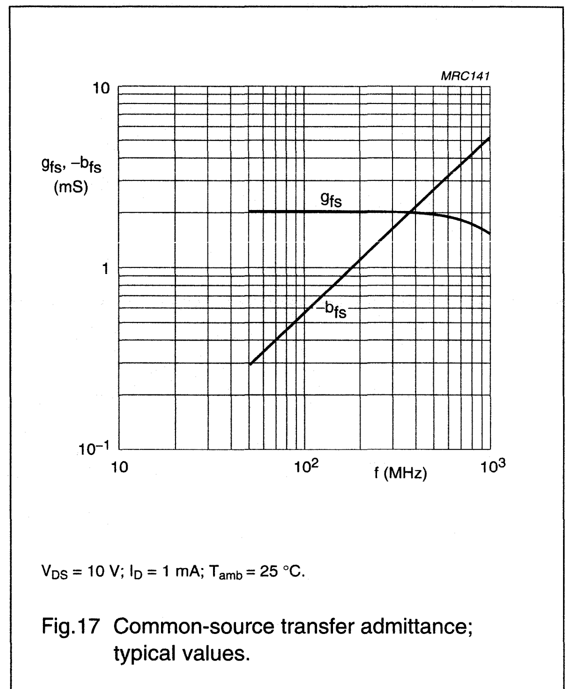
$V_{DS} = 15$ V.

Fig.15 Input capacitance; typical values.



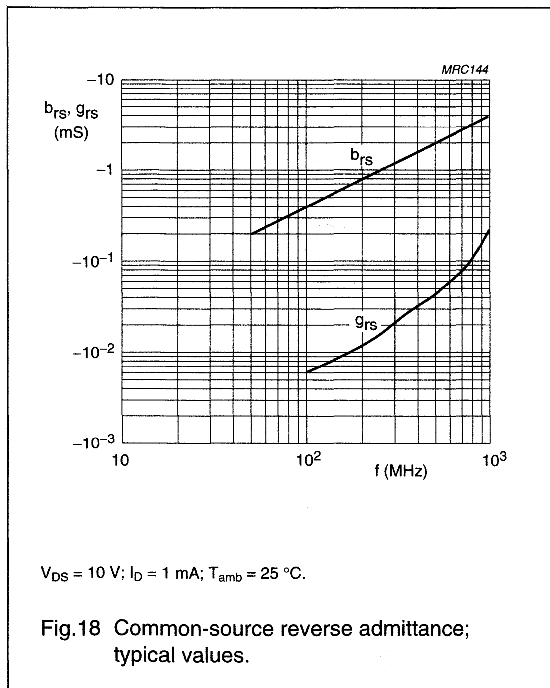
V_{DS} = 10 V; I_D = 1 mA; T_{amb} = 25 °C.

Fig.16 Common-source input admittance; typical values.



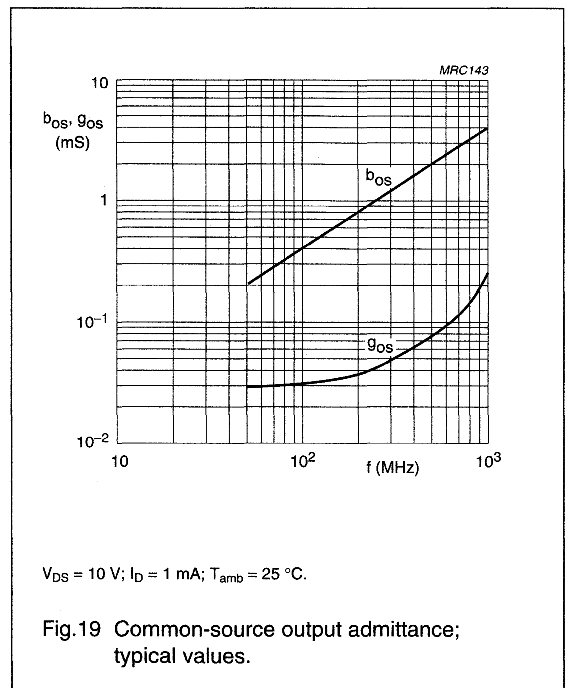
V_{DS} = 10 V; I_D = 1 mA; T_{amb} = 25 °C.

Fig.17 Common-source transfer admittance; typical values.



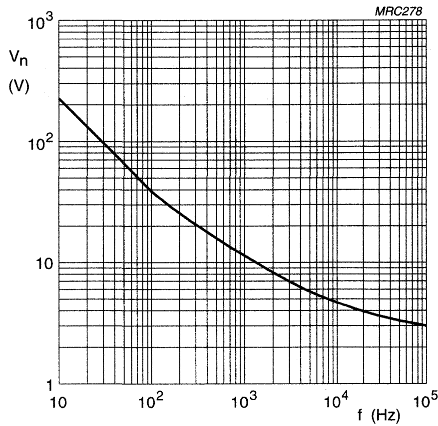
V_{DS} = 10 V; I_D = 1 mA; T_{amb} = 25 °C.

Fig.18 Common-source reverse admittance; typical values.



V_{DS} = 10 V; I_D = 1 mA; T_{amb} = 25 °C.

Fig.19 Common-source output admittance; typical values.



V_{DS} = 10 V; I_D = 1 mA.

Fig.20 Equivalent noise voltage as a function of frequency.

N-channel junction FETs BF851A; BF851B; BF851C

FEATURES

- High transfer admittance
- Low input capacitance
- Low feedback capacitance
- Low noise.

APPLICATIONS

- Preamplifiers for AM tuners in car radios.

DESCRIPTION

N-channel symmetrical junction field effect transistors in a SOT54 (TO-92) package.

PINNING - SOT54 (TO-92)

PIN	SYMBOL	DESCRIPTION
1	g	gate
2	s	source
3	d	drain

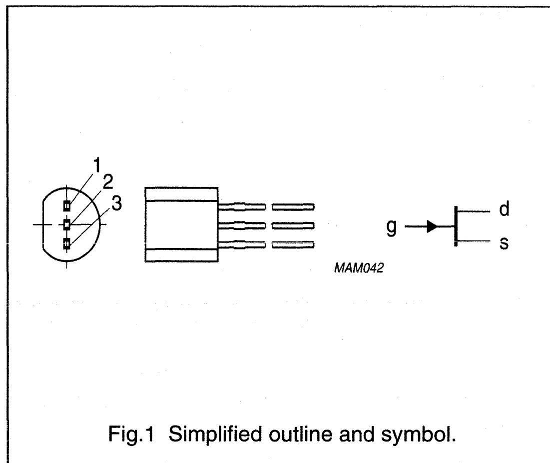


Fig.1 Simplified outline and symbol.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	25	V
I_{DSS}	drain current	$V_{GS} = 0$; $V_{DS} = 8$ V			
	BF851A		2	6.5	mA
	BF851B		6	15	mA
	BF851C		12	25	mA
P_{tot}	total power dissipation	up to $T_{amb} = 40$ °C	–	400	mW
$\lvert y_{fs} \rvert$	forward transfer admittance	$V_{GS} = 0$; $V_{DS} = 8$ V			
	BF851A		12	20	mS
	BF851B		16	25	mS
	BF851C		20	30	mS
C_{iss}	input capacitance	f = 1 MHz	–	10	pF
C_{rss}	reverse transfer capacitance	f = 1 MHz	–	3	pF

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	25	V
V_{GSO}	gate-source voltage	open drain	–	25	V
V_{DGO}	drain-gate voltage (DC)	open source	–	25	V
I_G	forward gate current (DC)		–	10	mA
P_{tot}	total power dissipation	up to T_{amb} = 40 °C; note 1	–	400	mW
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–	150	°C

Note

1. Device mounted on an epoxy printed-circuit board; maximum lead length 4 mm; mounting pad for the drain lead minimum 10 mm^2.

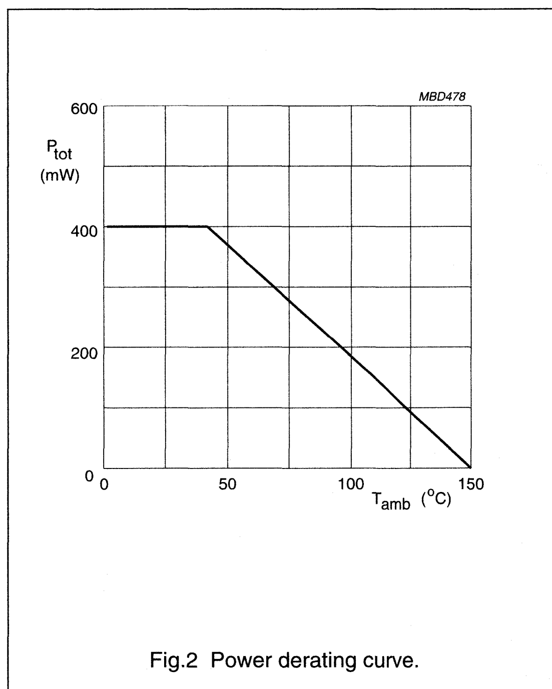


Fig.2 Power derating curve.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient; note 1	250	K/W

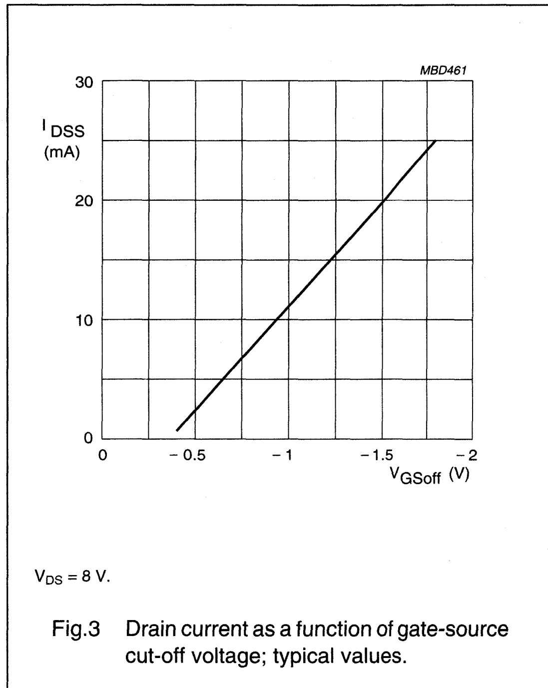
Note

1. Device mounted on an epoxy printed-circuit board; maximum lead length 4 mm; mounting pad for the drain lead minimum 10 mm^2.

CHARACTERISTICS

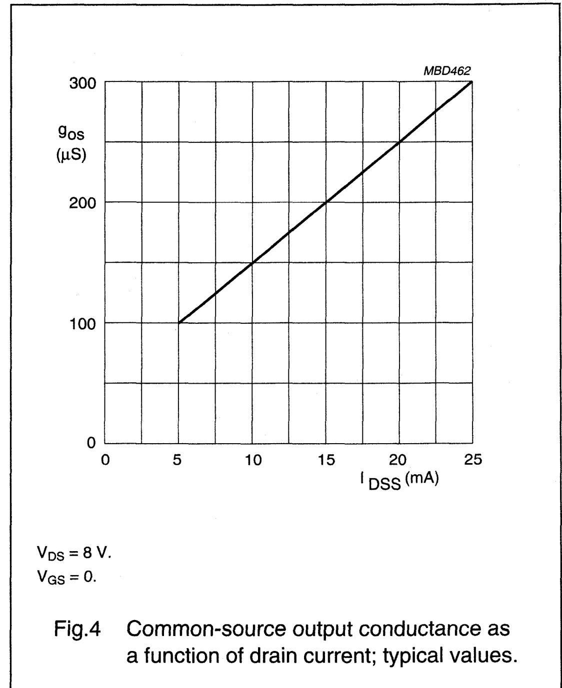
T_j = 25 °C; V_{DS} = 8 V; V_{GS} = 0; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)GSS}$	gate-source breakdown voltage	I_G = −1 μA	−25	−	−	V
V_{GSoff}	gate-source cut-off voltage	I_D = 1 μA				
	BF851A		−0.2	−	−1	V
	BF851B		−0.5	−	−1.5	V
	BF851C		−0.8	−	−2	V
V_{GSS}	gate-source forward voltage	V_{DS} = 0; I_G = 1 mA	−	−	1	V
I_{DSS}	drain current					
	BF851A		2	−	6.5	mA
	BF851B		6	−	15	mA
	BF851C		12	−	25	mA
I_{GSS}	gate cut-off current	V_{GS} = −20 V; V_{DS} = 0	−	−	−1	nA
$\|y_{fs}\|$	forward transfer admittance					
	BF851A		12	−	20	mS
	BF851B		16	−	25	mS
	BF851C		20	−	30	mS
g_{os}	common source output conductance					
	BF851A		−	−	200	μS
	BF851B		−	−	250	μS
	BF851C		−	−	300	μS
C_{iss}	input capacitance	f = 1 MHz	−	−	10	pF
C_{rss}	reverse transfer capacitance	f = 1 MHz	−	2.4	3	pF
$V_n/\sqrt{B}$	equivalent input noise voltage	V_{GS} = 0; f = 1 MHz	−	1.5	−	nV/√Hz



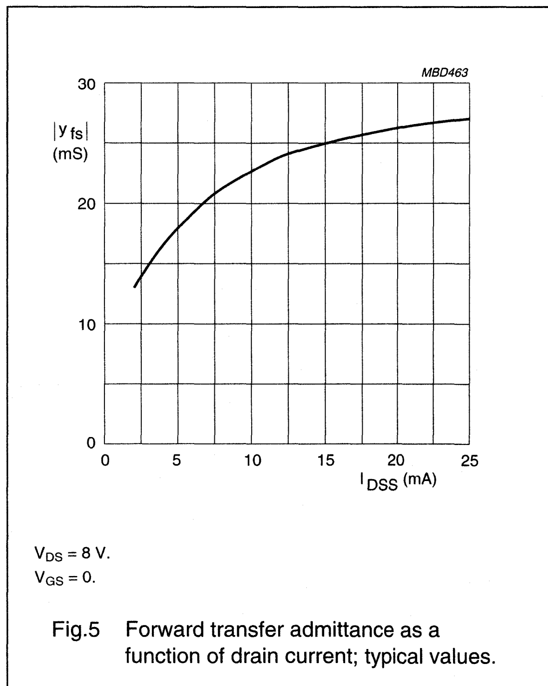
V_{DS} = 8 V.

Fig.3 Drain current as a function of gate-source cut-off voltage; typical values.



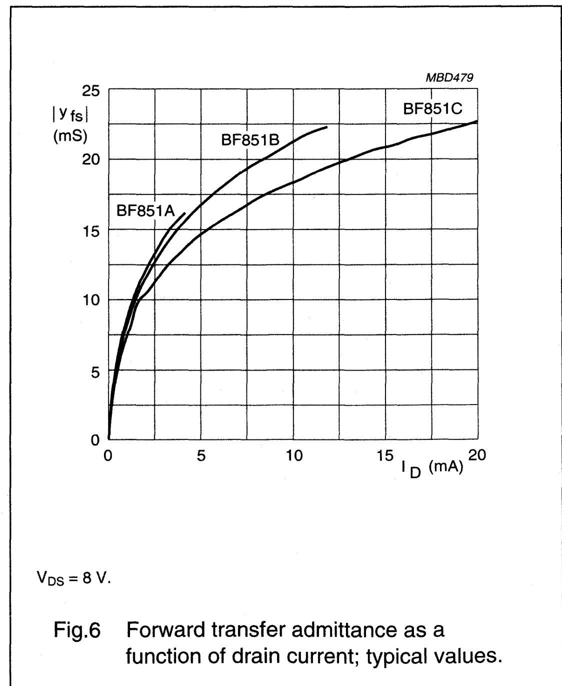
V_{DS} = 8 V.
V_{GS} = 0.

Fig.4 Common-source output conductance as a function of drain current; typical values.



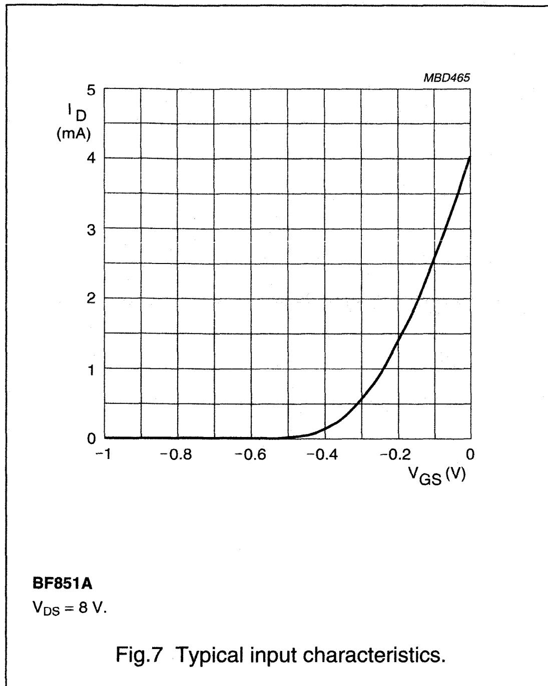
V_{DS} = 8 V.
V_{GS} = 0.

Fig.5 Forward transfer admittance as a function of drain current; typical values.



V_{DS} = 8 V.

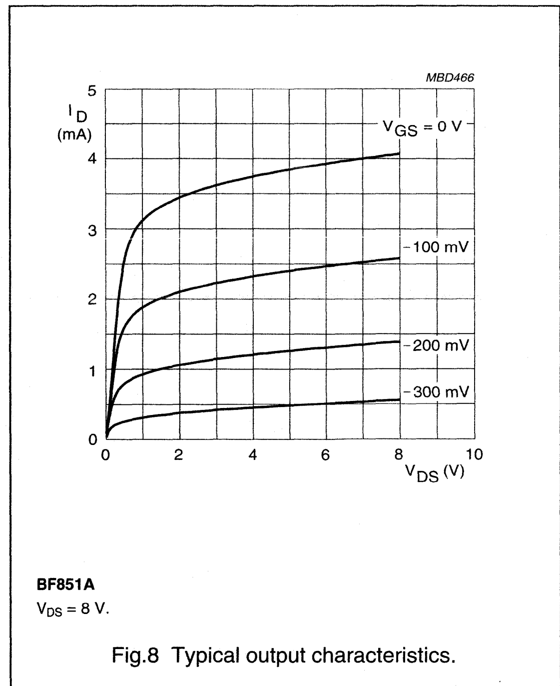
Fig.6 Forward transfer admittance as a function of drain current; typical values.



BF851A

V_{DS} = 8 V.

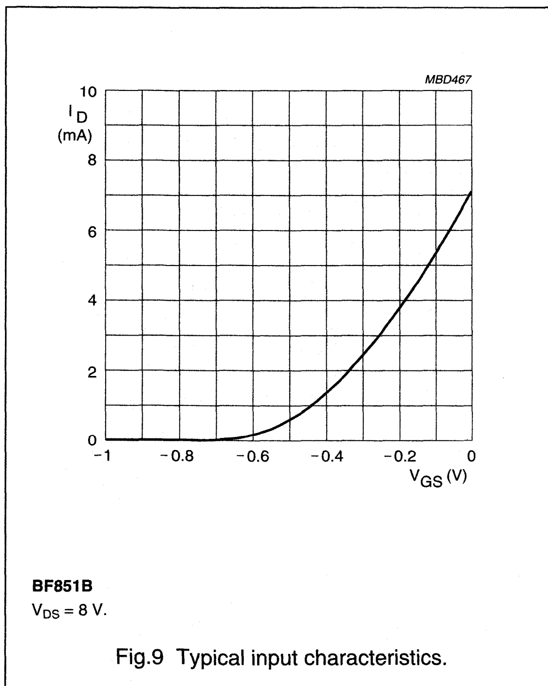
Fig.7 Typical input characteristics.



BF851A

V_{DS} = 8 V.

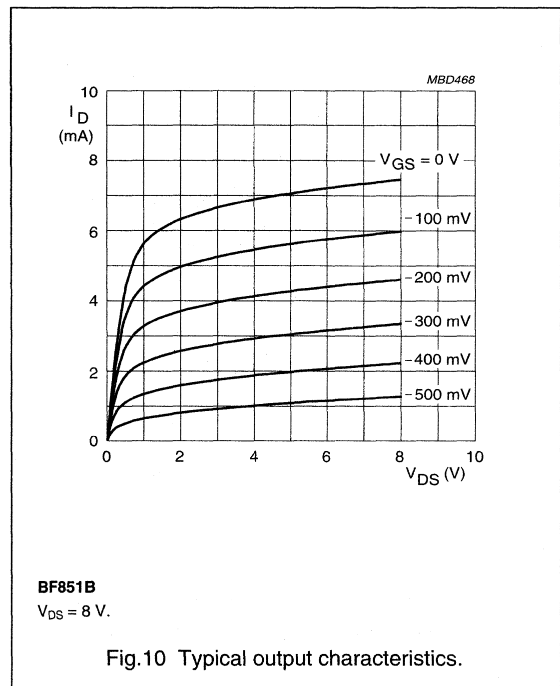
Fig.8 Typical output characteristics.



BF851B

V_{DS} = 8 V.

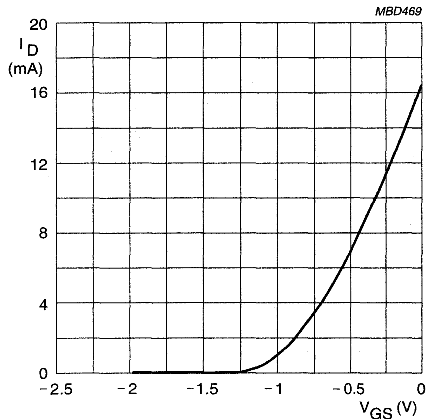
Fig.9 Typical input characteristics.



BF851B

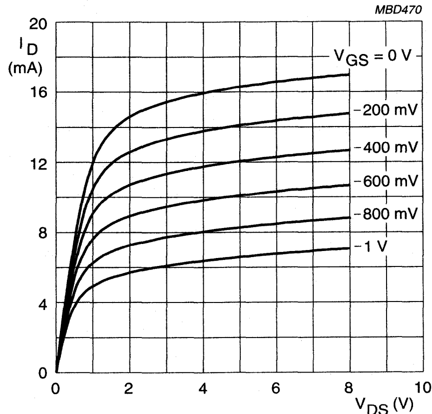
V_{DS} = 8 V.

Fig.10 Typical output characteristics.



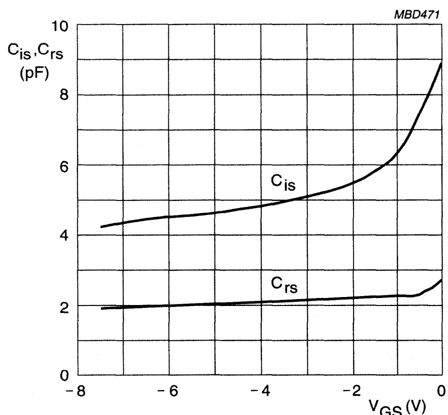
BF851C
V_{DS} = 8 V.

Fig.11 Typical input characteristics.



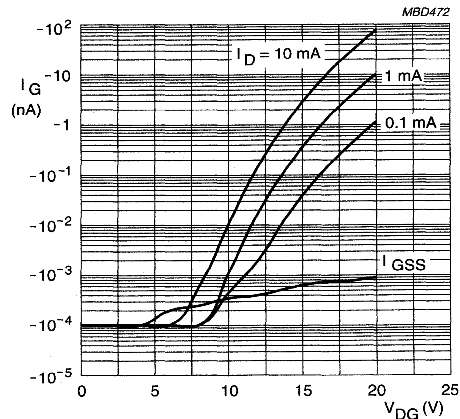
BF851C
V_{DS} = 8 V.

Fig.12 Typical output characteristics.



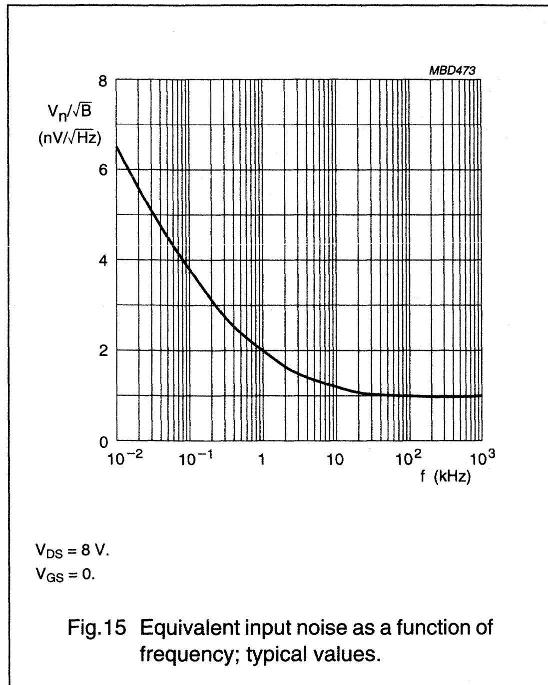
V_{DS} = 8 V.
f = 1 MHz.

Fig.13 Input and reverse transfer capacitance as functions of gate-source voltage; typical values.



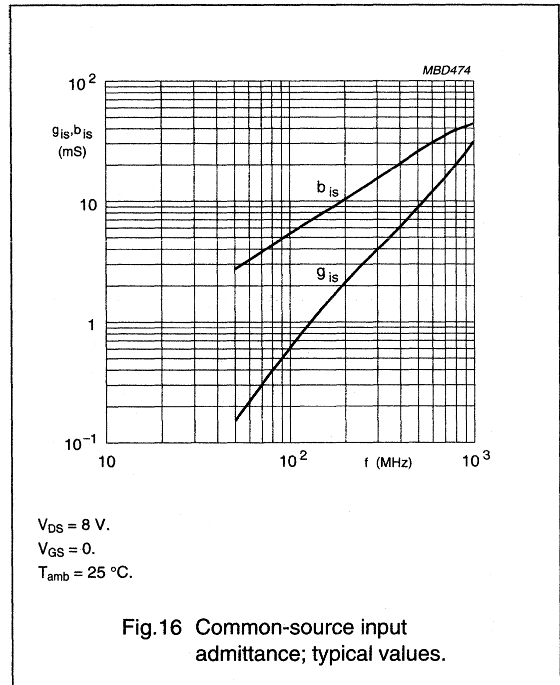
V_{DS} = 8 V.

Fig.14 Gate current as a function of drain-gate voltage; typical values.



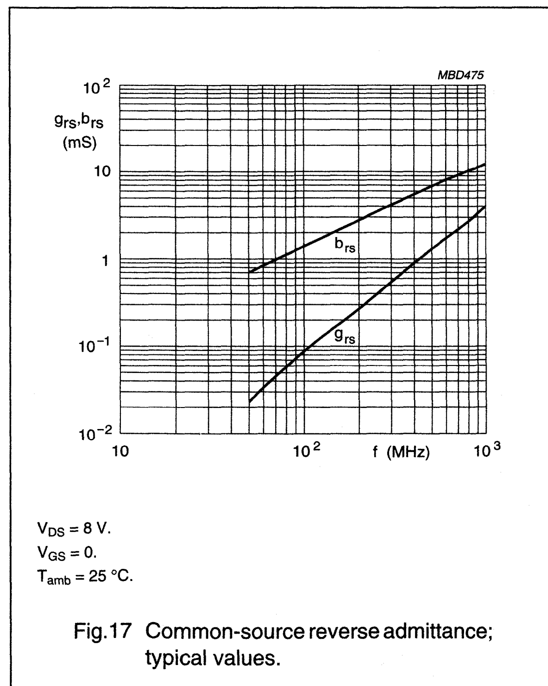
V_{DS} = 8 V.
V_{GS} = 0.

Fig.15 Equivalent input noise as a function of frequency; typical values.



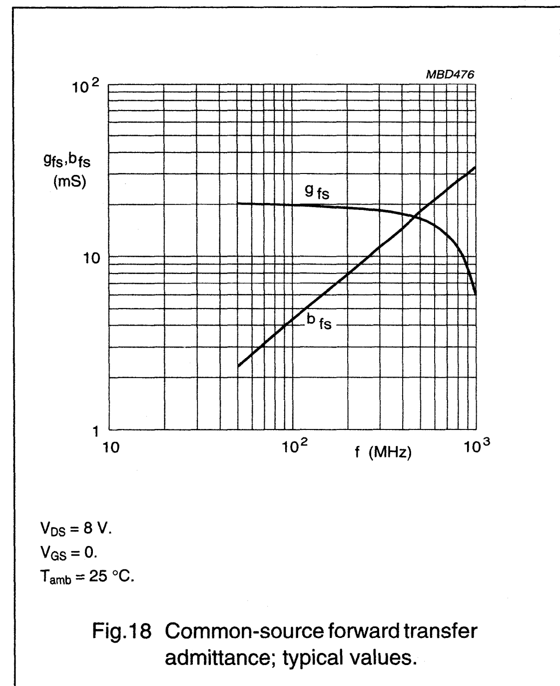
V_{DS} = 8 V.
V_{GS} = 0.
T_{amb} = 25 °C.

Fig.16 Common-source input admittance; typical values.



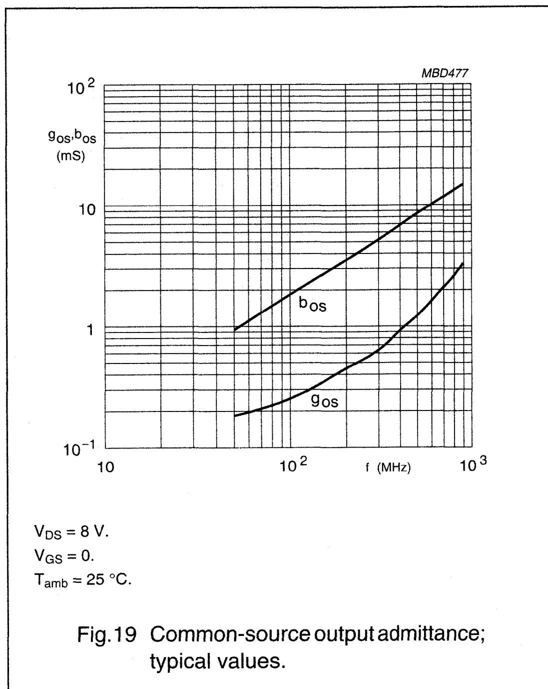
V_{DS} = 8 V.
V_{GS} = 0.
T_{amb} = 25 °C.

Fig.17 Common-source reverse admittance; typical values.



V_{DS} = 8 V.
V_{GS} = 0.
T_{amb} = 25 °C.

Fig.18 Common-source forward transfer admittance; typical values.



V_{DS} = 8 V.
V_{GS} = 0.
T_{amb} = 25 °C.

Fig.19 Common-source output admittance; typical values.

FEATURES

- High transfer admittance
- Low input capacitance
- Low feedback capacitance
- Low noise.

APPLICATIONS

- Preamplifiers for AM tuners in car radios.

DESCRIPTION

N-channel symmetrical junction field effect transistors in a SOT23 package.

PINNING - SOT23

PIN	SYMBOL	DESCRIPTION
1	s	source
2	d	drain
3	g	gate

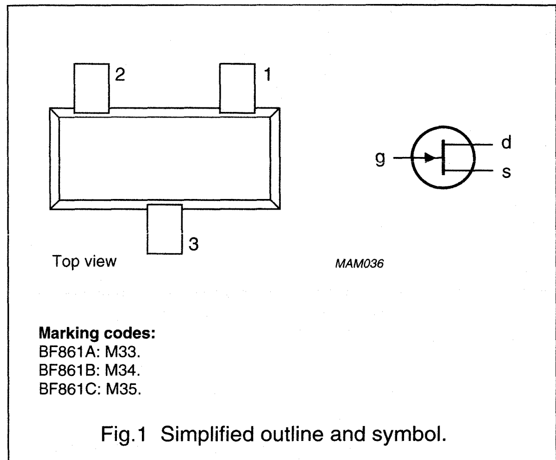


Fig.1 Simplified outline and symbol.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	25	V
I_{DSS}	drain current	$V_{GS} = 0$; $V_{DS} = 8$ V			
	BF861A		2	6.5	mA
	BF861B		6	15	mA
	BF861C		12	25	mA
P_{tot}	total power dissipation	up to $T_{amb} = 25$ °C	–	250	mW
$\lvert y_{fs} \rvert$	forward transfer admittance	$V_{GS} = 0$; $V_{DS} = 8$ V			
	BF861A		12	20	mS
	BF861B		16	25	mS
	BF861C		20	30	mS
C_{iss}	input capacitance	f = 1 MHz	–	10	pF
C_{rss}	reverse transfer capacitance	f = 1 MHz	–	2.7	pF

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	25	V
V_{GSO}	gate-source voltage	open drain	–	25	V
V_{DGO}	drain-gate voltage (DC)	open source	–	25	V
I_G	forward gate current (DC)		–	10	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C; note 1	–	250	mW
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–	150	°C

Note

1. Device mounted on an FR4 printed-circuit board.

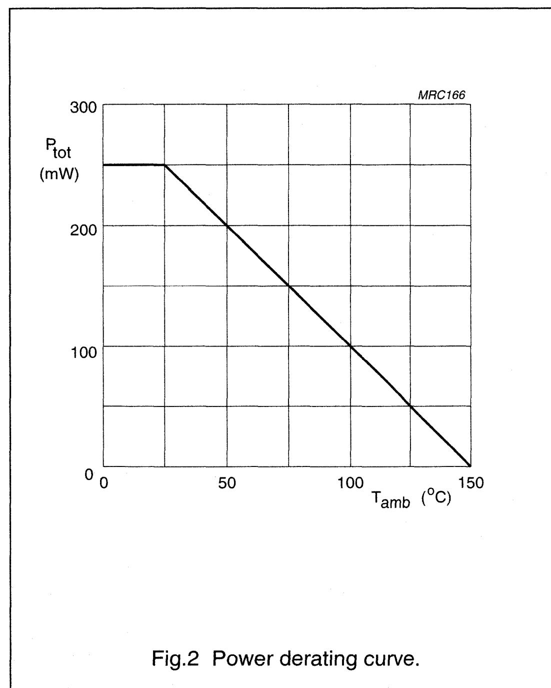


Fig.2 Power derating curve.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient; note 1	500	K/W

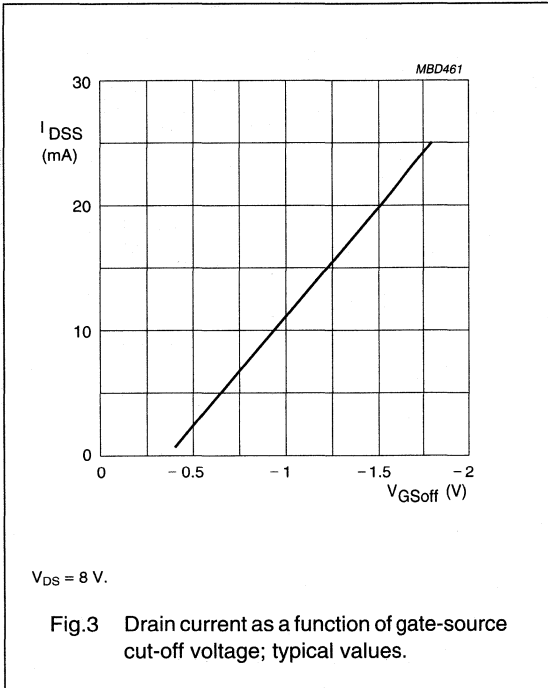
Note

1. Device mounted on an FR4 printed-circuit board.

CHARACTERISTICS

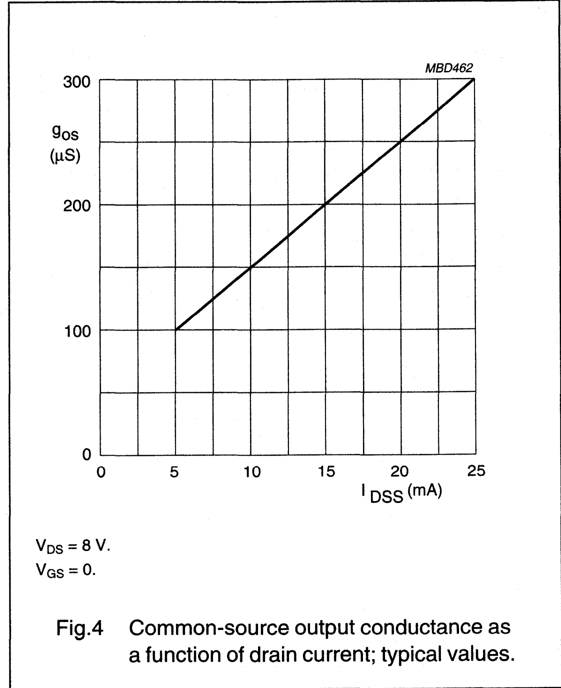
T_j = 25 °C; V_{DS} = 8 V; V_{GS} = 0; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)GSS}$	gate-source breakdown voltage	$I_G = -1\ \mu A$	−25	−	−	V
V_{GSoff}	gate-source cut-off voltage	$I_D = 1\ \mu A$				
	BF861A		−0.2	−	−1	V
	BF861B		−0.5	−	−1.5	V
	BF861C		−0.8	−	−2	V
V_{GSS}	gate-source forward voltage	$V_{DS} = 0$; $I_G = 1$ mA	−	−	1	V
I_{DSS}	drain current					
	BF861A		2	−	6.5	mA
	BF861B		6	−	15	mA
	BF861C		12	−	25	mA
I_{GSS}	gate cut-off current	$V_{GS} = -20$ V; $V_{DS} = 0$	−	−	−1	nA
$\|y_{fs}\|$	forward transfer admittance					
	BF861A		12	−	20	mS
	BF861B		16	−	25	mS
	BF861C		20	−	30	mS
g_{os}	common source output conductance					
	BF861A		−	−	200	μS
	BF861B		−	−	250	μS
	BF861C		−	−	300	μS
C_{iss}	input capacitance	f = 1 MHz	−	−	10	pF
C_{rss}	reverse transfer capacitance	f = 1 MHz	−	2.1	2.7	pF
$V_n/\sqrt{B}$	equivalent input noise voltage	$V_{GS} = 0$; f = 1 MHz	−	1.5	−	nV/√Hz



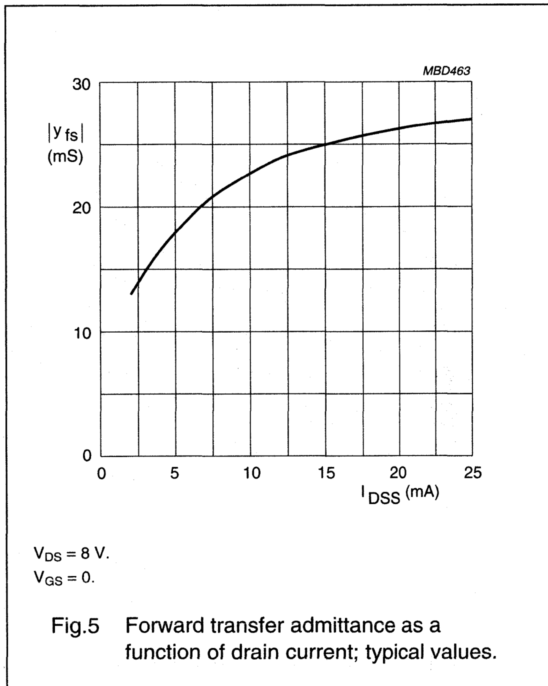
V_{DS} = 8 V.

Fig.3 Drain current as a function of gate-source cut-off voltage; typical values.



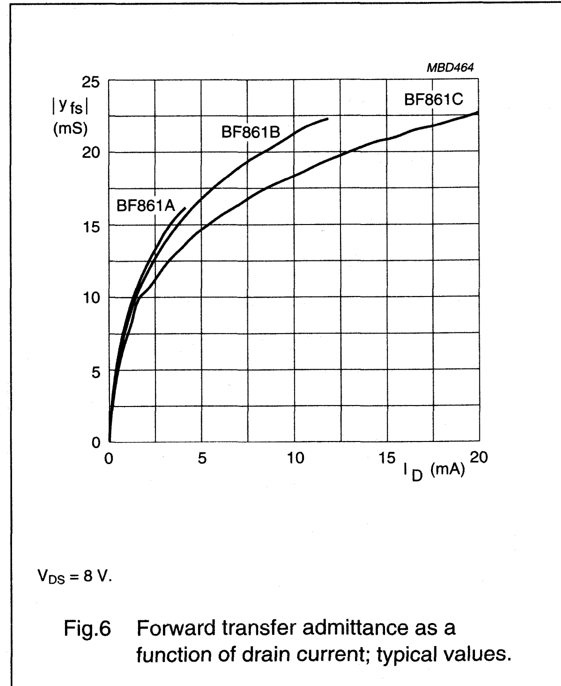
V_{DS} = 8 V.
V_{GS} = 0.

Fig.4 Common-source output conductance as a function of drain current; typical values.



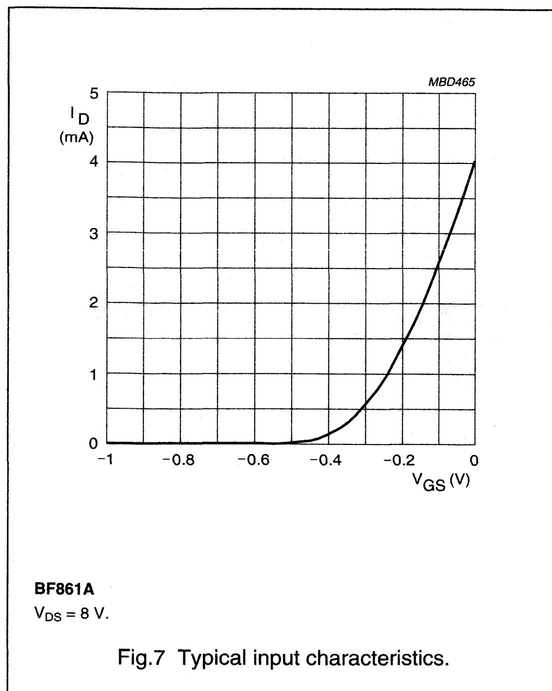
V_{DS} = 8 V.
V_{GS} = 0.

Fig.5 Forward transfer admittance as a function of drain current; typical values.



V_{DS} = 8 V.

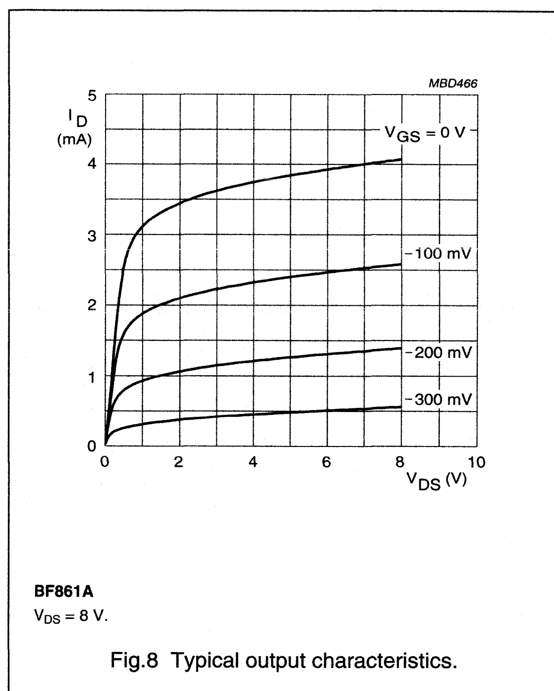
Fig.6 Forward transfer admittance as a function of drain current; typical values.



BF861A

V_{DS} = 8 V.

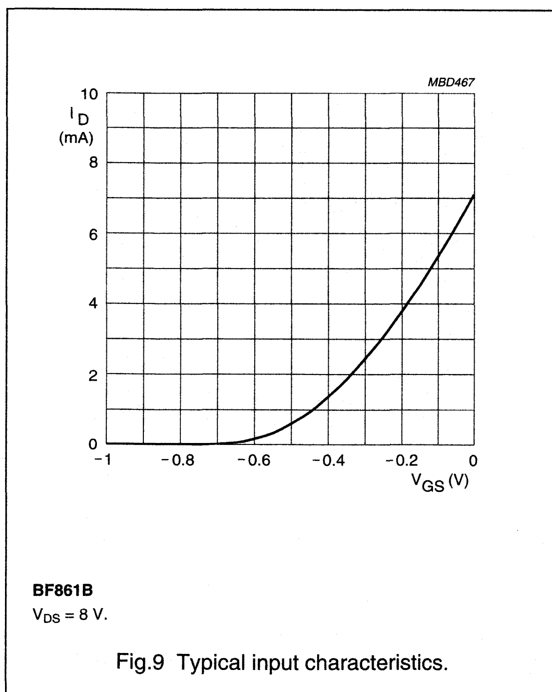
Fig.7 Typical input characteristics.



BF861A

V_{DS} = 8 V.

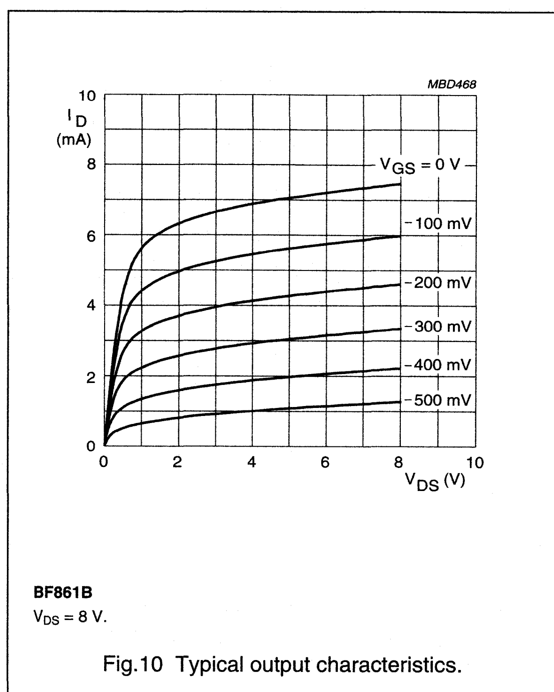
Fig.8 Typical output characteristics.



BF861B

V_{DS} = 8 V.

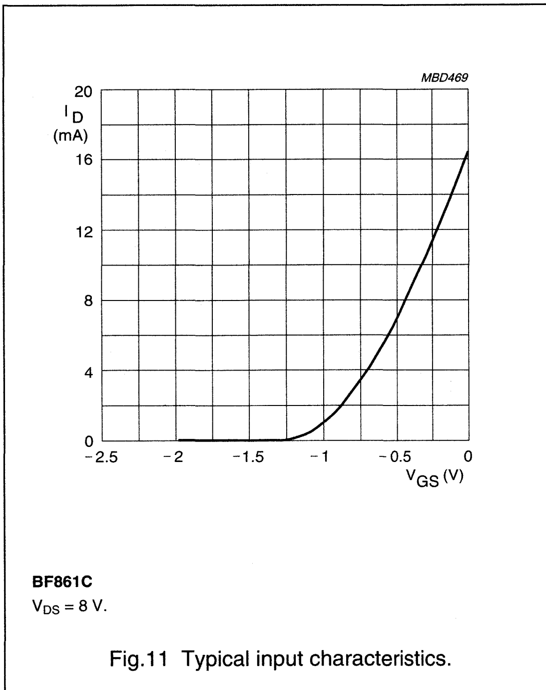
Fig.9 Typical input characteristics.



BF861B

V_{DS} = 8 V.

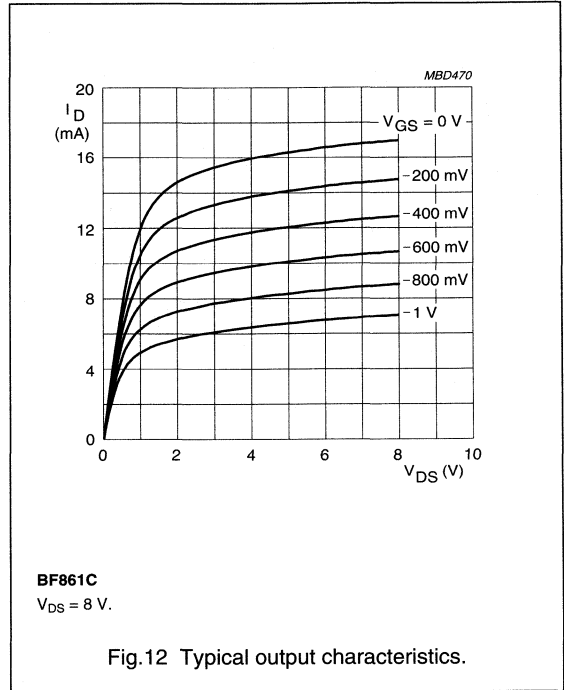
Fig.10 Typical output characteristics.



BF861C

$V_{DS} = 8$ V.

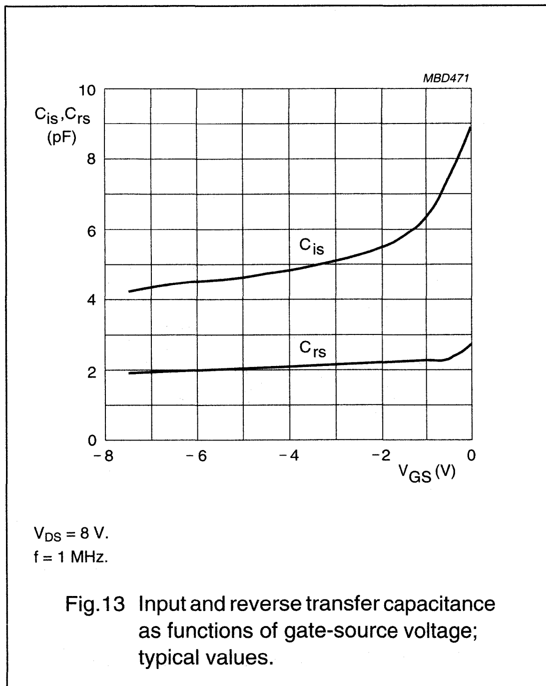
Fig.11 Typical input characteristics.



BF861C

$V_{DS} = 8$ V.

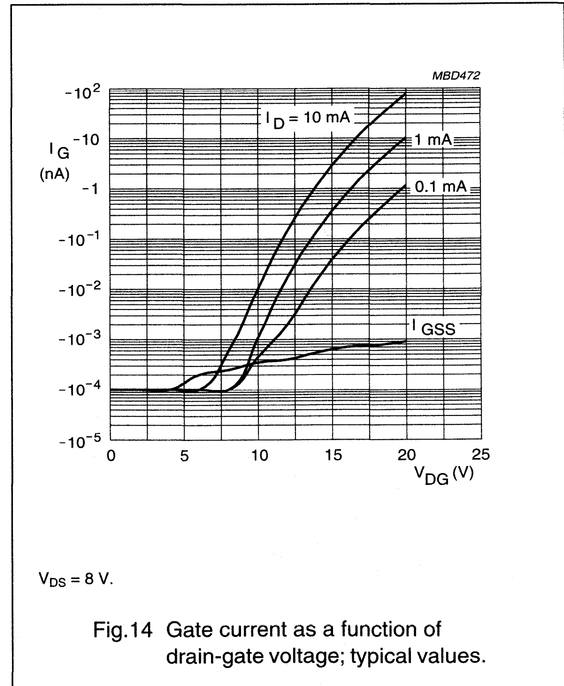
Fig.12 Typical output characteristics.



$V_{DS} = 8$ V.

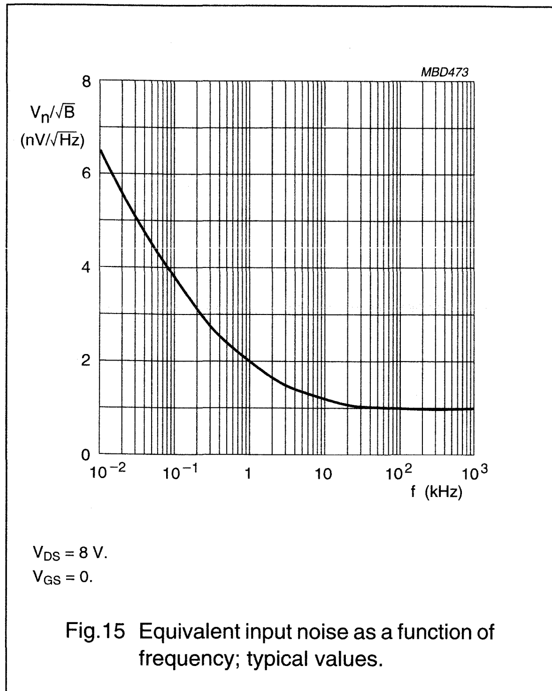
f = 1 MHz.

Fig.13 Input and reverse transfer capacitance as functions of gate-source voltage; typical values.



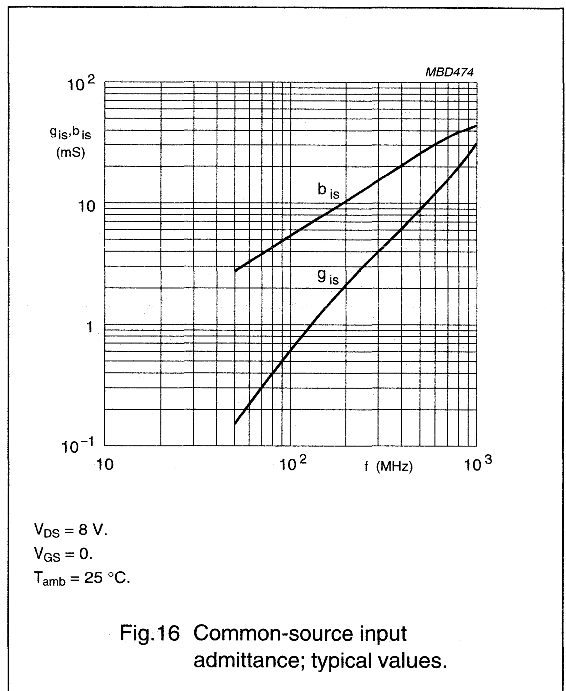
$V_{DS} = 8$ V.

Fig.14 Gate current as a function of drain-gate voltage; typical values.



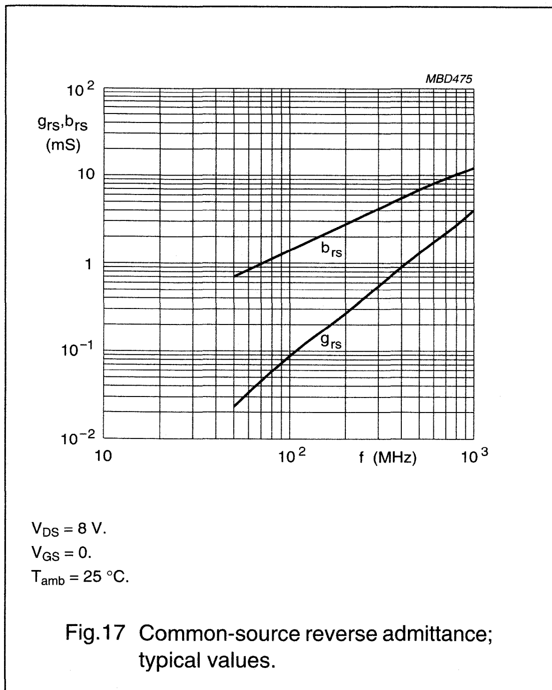
V_{DS} = 8 V.
V_{GS} = 0.

Fig.15 Equivalent input noise as a function of frequency; typical values.



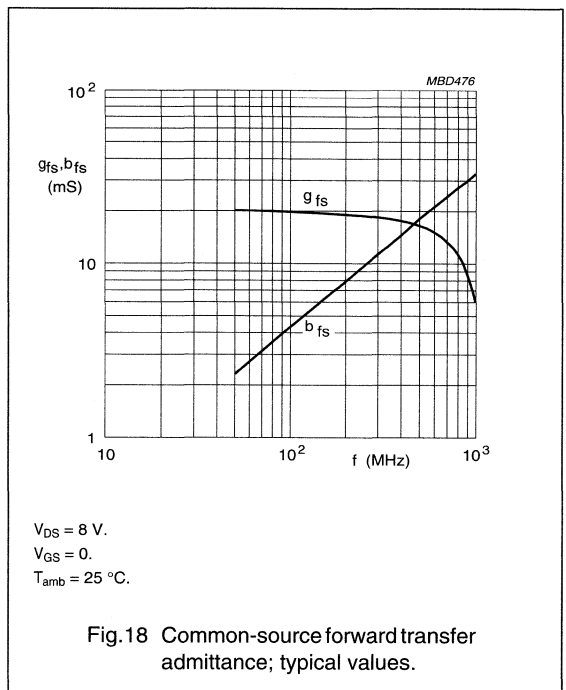
V_{DS} = 8 V.
V_{GS} = 0.
T_{amb} = 25 °C.

Fig.16 Common-source input admittance; typical values.



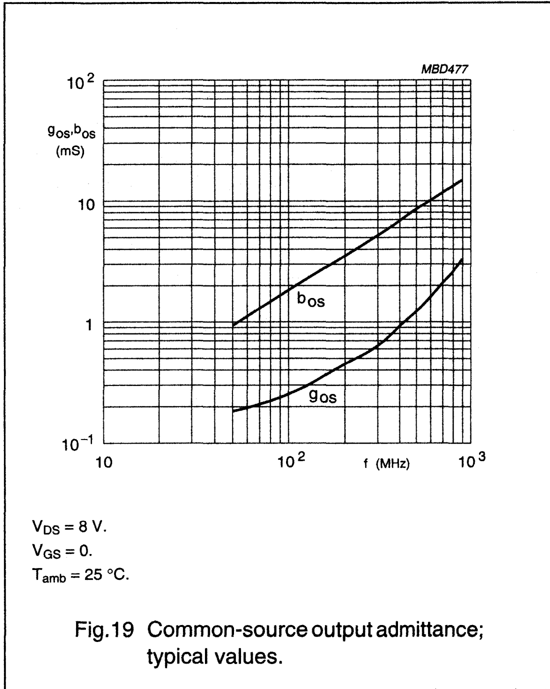
V_{DS} = 8 V.
V_{GS} = 0.
T_{amb} = 25 °C.

Fig.17 Common-source reverse admittance; typical values.



V_{DS} = 8 V.
V_{GS} = 0.
T_{amb} = 25 °C.

Fig.18 Common-source forward transfer admittance; typical values.



V_{DS} = 8 V.
V_{GS} = 0.
T_{amb} = 25 °C.

Fig.19 Common-source output admittance; typical values.

Silicon n-channel dual gate MOS-FETs — BF901; BF901R

FEATURES

- Intended for low voltage operation
- Short channel transistor with high ratio $|Y_{fs}|:C_{is}$
- Low noise gain-controlled amplifier to 1 GHz
- BF901R has reverse pinning.

DESCRIPTION

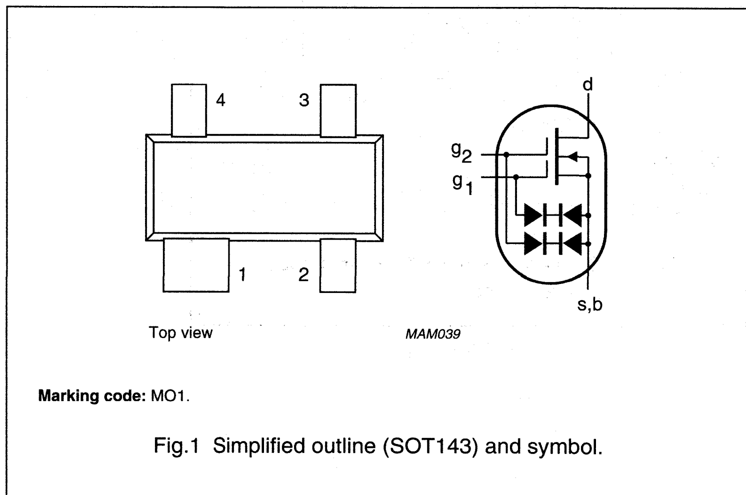
Enhancement type field-effect transistors in plastic microminiature SOT143 and SOT143R envelopes, with source and substrate interconnected. They are intended for UHF and VHF applications, such as television tuners and professional communications equipment especially suited for low voltage operation. These MOS-FET tetrodes are protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

PINNING

PIN	DESCRIPTION
1	source
2	drain
3	gate 2
4	gate 1

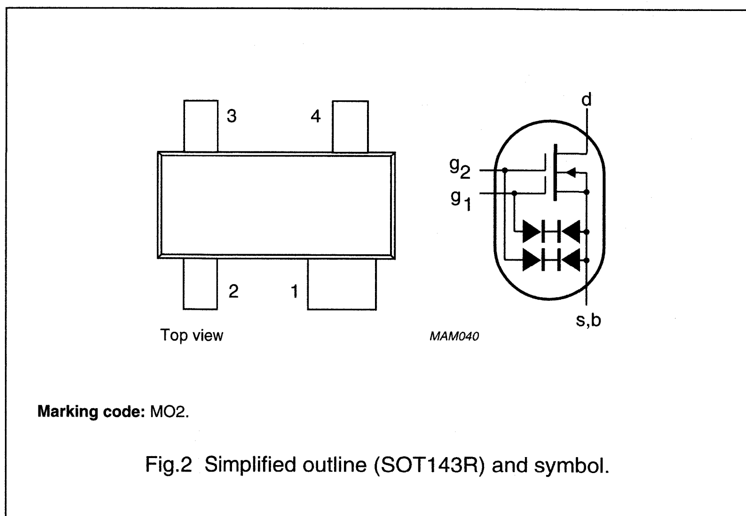
QUICK REFERENCE DATA

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
V_{DS}	drain-source voltage	–	12	V
I_D	drain current	–	30	mA
P_{tot}	total power dissipation	–	200	mW
T_j	junction temperature	–	150	°C
$\|Y_{fs}\|$	transfer admittance	28	35	mS
C_{ig1-s}	input capacitance at gate 1	2.35	2.75	pF
C_{rs}	feedback capacitance	25	–	fF
F	noise figure at 800 MHz	1.7	–	dB



Marking code: MO1.

Fig.1 Simplified outline (SOT143) and symbol.



Marking code: MO2.

Fig.2 Simplified outline (SOT143R) and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	12	V
$V_{D\text{-}G2}$	drain-gate 2 voltage		–	6	V
I_D	DC drain current		–	30	mA
$\pm I_{G1\text{-}S}$	gate 1-source current		–	10	mA
$\pm I_{G2\text{-}S}$	gate 2-source current		–	10	mA
P_{tot}	total power dissipation				
	BF901	up to T_{amb} = 50 °C (note 1)	–	200	mW
	BF901R	up to T_{amb} = 40 °C (note 1)	–	200	mW
T_{stg}	storage temperature		–65	150	°C
T_j	junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient (note 1)	
	BF901	500 K/W
	BF901R	550 K/W

Note

1. Device mounted on an FR4 printboard.

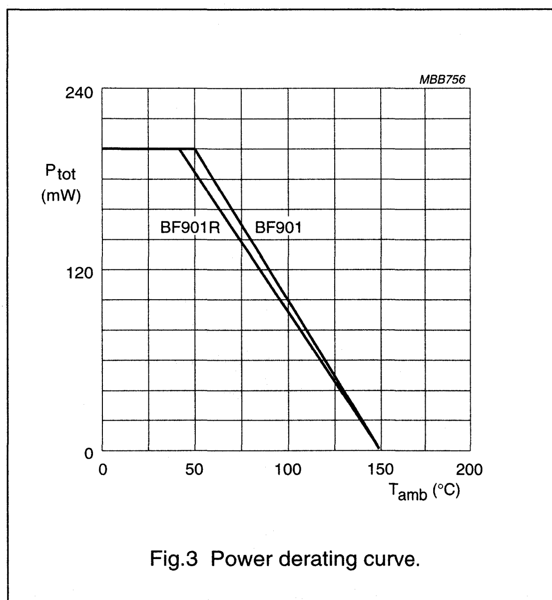


Fig.3 Power derating curve.

STATIC CHARACTERISTICS

$T_j = 25\ °C$.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$\pm I_{G1\text{-}SS}$	gate 1 cut-off current	$\pm V_{G1\text{-}S} = 5\ V$; $V_{G2\text{-}S} = V_{DS} = 0$	–	50	nA
$\pm I_{G2\text{-}SS}$	gate 2 cut-off current	$\pm V_{G2\text{-}S} = 5\ V$; $V_{G1\text{-}S} = V_{DS} = 0$	–	50	nA
$\pm V_{(BR)G1\text{-}SS}$	gate 1-source breakdown voltage	$\pm I_{G1\text{-}SS} = 10\ mA$; $V_{G2\text{-}S} = V_{DS} = 0$	6	20	V
$\pm V_{(BR)G2\text{-}SS}$	gate 2-source breakdown voltage	$\pm I_{G2\text{-}SS} = 10\ mA$; $V_{G1\text{-}S} = V_{DS} = 0$	6	20	V
$V_{G1\text{-}S(th)}$	gate 1-source threshold voltage	$I_D = 20\ \mu A$; $V_{DS} = 8\ V$; $V_{G2\text{-}S} = 4\ V$	0	0.7	V
$V_{G2\text{-}S(th)}$	gate 2-source threshold voltage	$I_D = 20\ \mu A$; $V_{DS} = 8\ V$; $V_{G1\text{-}S} = 0$	0.3	1	V
I_{DSX}	drain-source current	$V_{DS} = 4\ V$; $V_{G1\text{-}S} = 1.1\ V$; $V_{G2\text{-}S} = 3.4\ V$	2	18	mA

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): $I_D = 14\ mA$; $V_{DS} = 5\ V$; $V_{G2\text{-}S} = 4\ V$; $T_{amb} = 25\ °C$.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\|Y_{fs}\|$	transfer admittance	pulsed; $T_j = 25\ °C$	25	28	35	mS
$C_{ig1\text{-}s}$	input capacitance at gate 1	f = 1 MHz	–	2.35	2.75	pF
$C_{ig2\text{-}s}$	input capacitance at gate 2	f = 1 MHz	–	1.2	–	pF
C_{os}	output capacitance	f = 1 MHz	–	1.4	–	pF
C_{rs}	feedback capacitance	f = 1 MHz	–	25	–	fF
F	noise figure	f = 200 MHz; $G_s = 2\ mS$; $B_s = B_{sopt.}$	–	0.7	–	dB
		f = 800 MHz; $G_s = 3.3\ mS$; $B_s = B_{sopt.}$	–	1.7	–	dB

N-channel dual gate MOS-FETs BF904; BF904R

FEATURES

- Specially designed for use at 5 V supply voltage
- Short channel transistor with high transfer admittance to input capacitance ratio
- Low noise gain controlled amplifier up to 1 GHz
- Superior cross-modulation performance during AGC.

APPLICATIONS

- VHF and UHF applications with 3 to 7 V supply voltage such as television tuners and professional communications equipment.

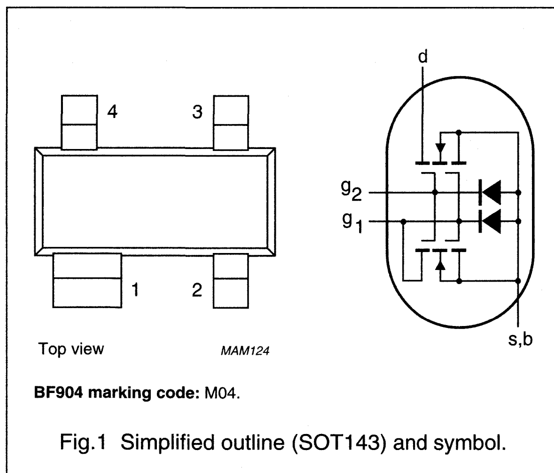
DESCRIPTION

Enhancement type field-effect transistor in a plastic microminiature SOT143 and SOT143R package. The transistor consists of an amplifier MOS-FET with source and substrate interconnected and an internal bias circuit to ensure good cross-modulation performance during AGC.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

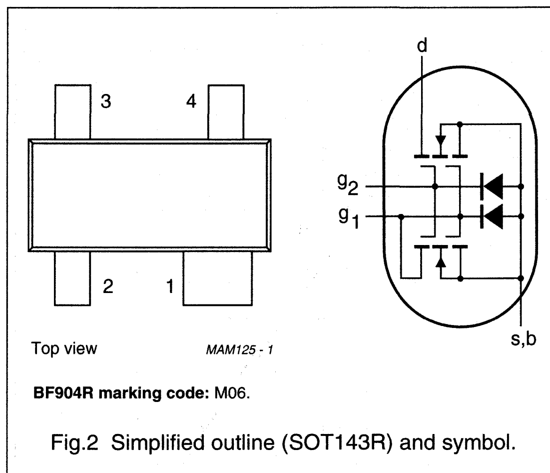
PINNING

PIN	SYMBOL	DESCRIPTION
1	s, b	source
2	d	drain
3	g_2	gate 2
4	g_1	gate 1



BF904 marking code: M04.

Fig.1 Simplified outline (SOT143) and symbol.



BF904R marking code: M06.

Fig.2 Simplified outline (SOT143R) and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DS}	drain-source voltage		–	–	7	V
I_D	drain current		–	–	30	mA
P_{tot}	total power dissipation		–	–	200	mW
T_j	operating junction temperature		–	–	150	°C
$\|y_{fs}\|$	forward transfer admittance		22	25	30	mS
C_{ig1-s}	input capacitance at gate 1		–	2.2	2.6	pF
C_{rs}	reverse transfer capacitance	f = 1 MHz	–	25	35	fF
F	noise figure	f = 800 MHz	–	2	–	dB

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	7	V
I_D	drain current		–	30	mA
I_{G1}	gate 1 current		–	±10	mA
I_{G2}	gate 2 current		–	±10	mA
P_{tot}	total power dissipation	see Fig.3			
	BF904	up to T_{amb} = 50 °C; note 1	–	200	mW
	BF904R	up to T_{amb} = 40 °C; note 1	–	200	mW
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–	150	°C

Note

1. Device mounted on a printed-circuit board.

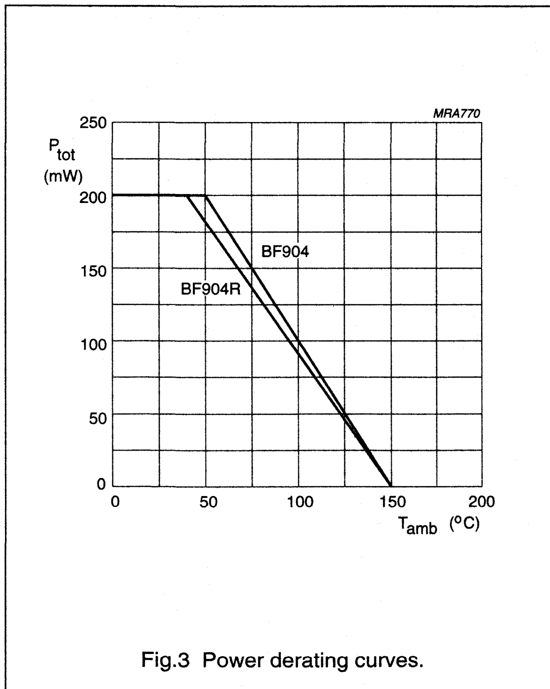


Fig.3 Power derating curves.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	note 1		
	BF904		500	K/W
	BF904R		550	K/W
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	note 2		
	BF904	T_s = 92 °C	290	K/W
	BF904R	T_s = 78 °C	360	K/W

Notes

1. Device mounted on a printed-circuit board.
2. T_s is the temperature at the soldering point of the source lead.

STATIC CHARACTERISTICS

T_j = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{(BR)G1\text{-}SS}$	gate 1-source breakdown voltage	$V_{G2\text{-}S} = V_{DS} = 0$; $I_{G1\text{-}S}$ = 10 mA	6	15	V
$V_{(BR)G2\text{-}SS}$	gate 2-source breakdown voltage	$V_{G1\text{-}S} = V_{DS} = 0$; $I_{G2\text{-}S}$ = 10 mA	6	15	V
$V_{(F)S\text{-}G1}$	forward source-gate 1 voltage	$V_{G2\text{-}S} = V_{DS} = 0$; $I_{S\text{-}G1}$ = 10 mA	0.5	1.5	V
$V_{(F)S\text{-}G2}$	forward source-gate 2 voltage	$V_{G1\text{-}S} = V_{DS} = 0$; $I_{S\text{-}G2}$ = 10 mA	0.5	1.5	V
$V_{G1\text{-}S(th)}$	gate 1-source threshold voltage	$V_{G2\text{-}S}$ = 4 V; V_{DS} = 5 V; I_D = 20 μA	0.3	1	V
$V_{G2\text{-}S(th)}$	gate 2-source threshold voltage	$V_{G1\text{-}S} = V_{DS}$ = 5 V; I_D = 20 μA	0.3	1.2	V
I_{DSX}	drain-source current	$V_{G2\text{-}S}$ = 4 V; V_{DS} = 5 V; R_{G1} = 120 kΩ; note 1	8	13	mA
$I_{G1\text{-}SS}$	gate 1 cut-off current	$V_{G2\text{-}S} = V_{DS} = 0$; $V_{G1\text{-}S}$ = 5 V	–	50	nA
$I_{G2\text{-}SS}$	gate 2 cut-off current	$V_{G1\text{-}S} = V_{DS} = 0$; $V_{G2\text{-}S}$ = 5 V	–	50	nA

Note

1. R_G connects gate 1 to V_{GG} = 5 V; see Fig.20.

DYNAMIC CHARACTERISTICS

Common source; T_{amb} = 25 °C; V_{DS} = 5 V; $V_{G2\text{-}S}$ = 4 V; I_D = 10 mA; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\|y_{fs}\|$	forward transfer admittance	pulsed; T_j = 25 °C	22	25	30	mS
$C_{ig1\text{-}s}$	input capacitance at gate 1	f = 1 MHz	–	2.2	2.6	pF
$C_{ig2\text{-}s}$	input capacitance at gate 2	f = 1 MHz	1	1.5	2	pF
C_{os}	drain-source capacitance	f = 1 MHz	1	1.3	1.6	pF
C_{rs}	reverse transfer capacitance	f = 1 MHz	–	25	35	fF
F	noise figure	f = 200 MHz; G_S = 2 mS; $B_S = B_{Sopt}$	–	1	1.5	dB
		f = 800 MHz; $G_S = G_{Sopt}$; $B_S = B_{Sopt}$	–	2	2.8	dB

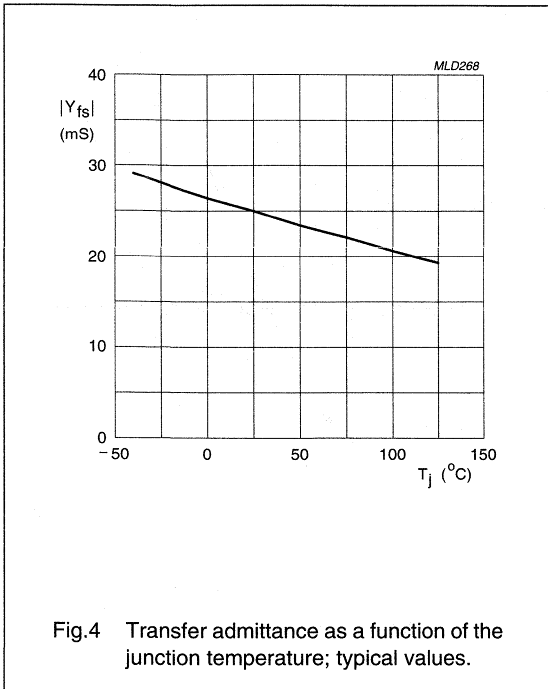
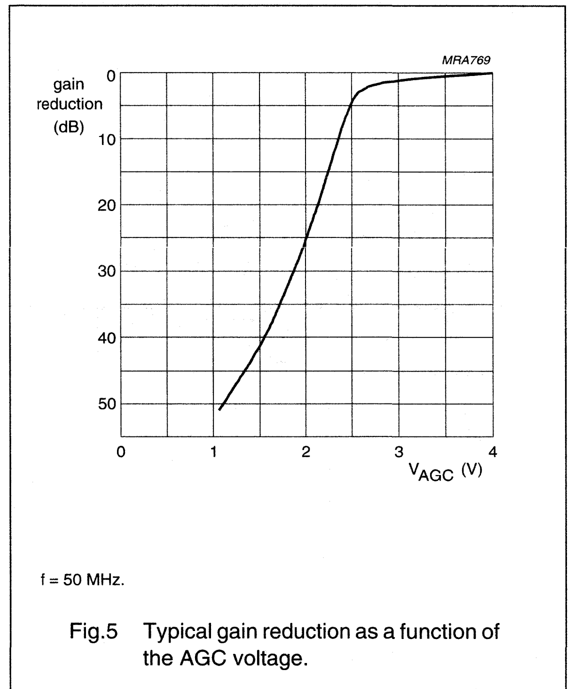
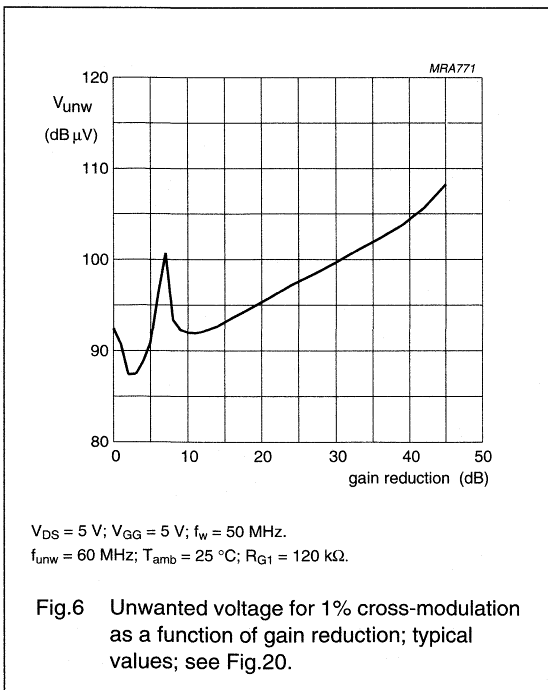


Fig.4 Transfer admittance as a function of the junction temperature; typical values.



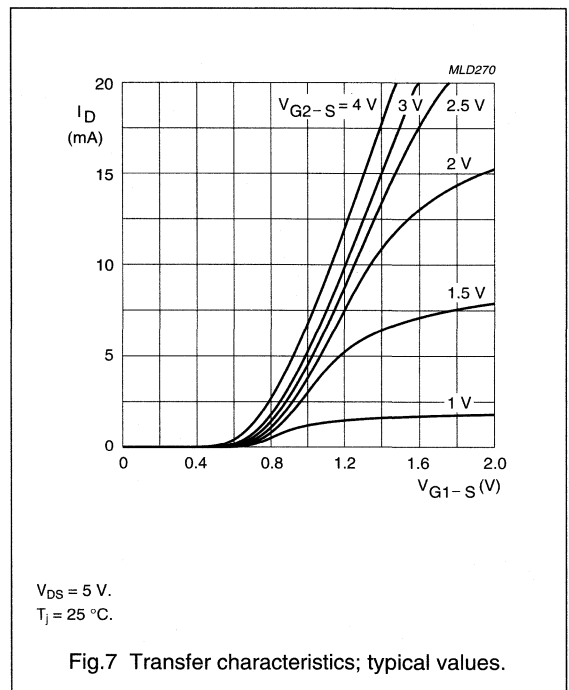
f = 50 MHz.

Fig.5 Typical gain reduction as a function of the AGC voltage.



V_{DS} = 5 V; V_{GG} = 5 V; f_w = 50 MHz.
f_{unw} = 60 MHz; T_{amb} = 25 °C; R_{G1} = 120 kΩ.

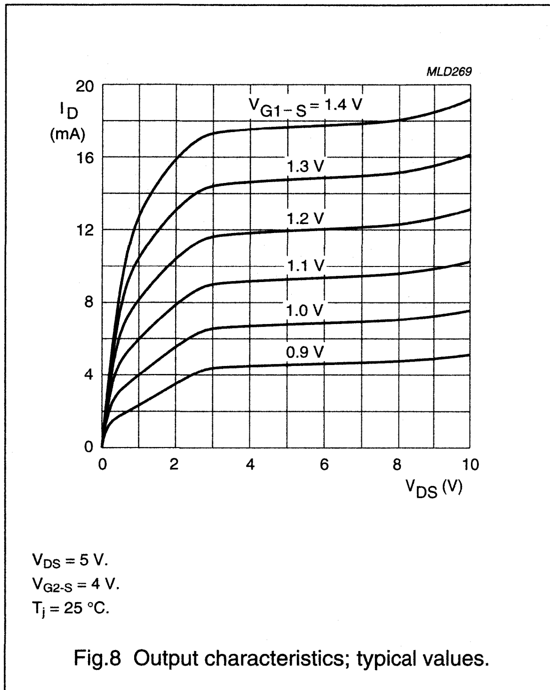
Fig.6 Unwanted voltage for 1% cross-modulation as a function of gain reduction; typical values; see Fig.20.



V_{DS} = 5 V.
T_j = 25 °C.

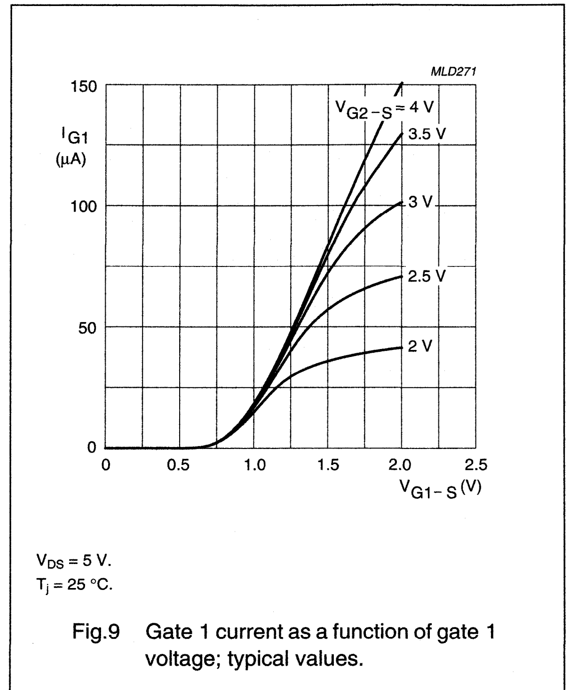
Fig.7 Transfer characteristics; typical values.

N-channel dual gate MOS-FETs BF904; BF904R



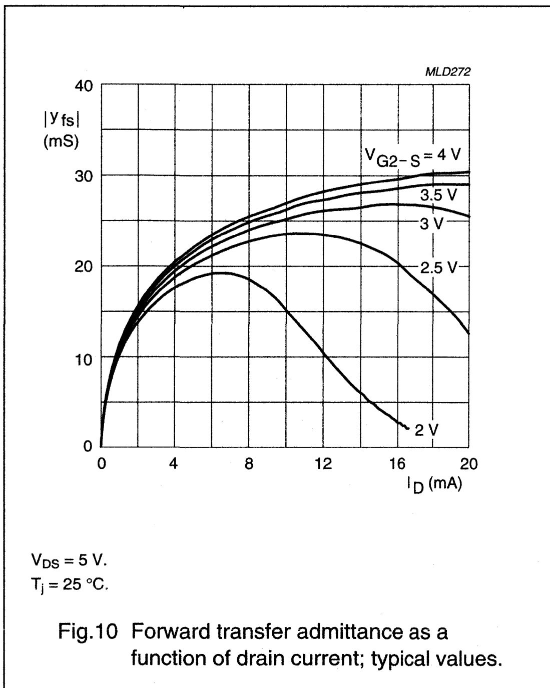
V_{DS} = 5 V.
V_{G2-S} = 4 V.
T_j = 25 °C.

Fig.8 Output characteristics; typical values.



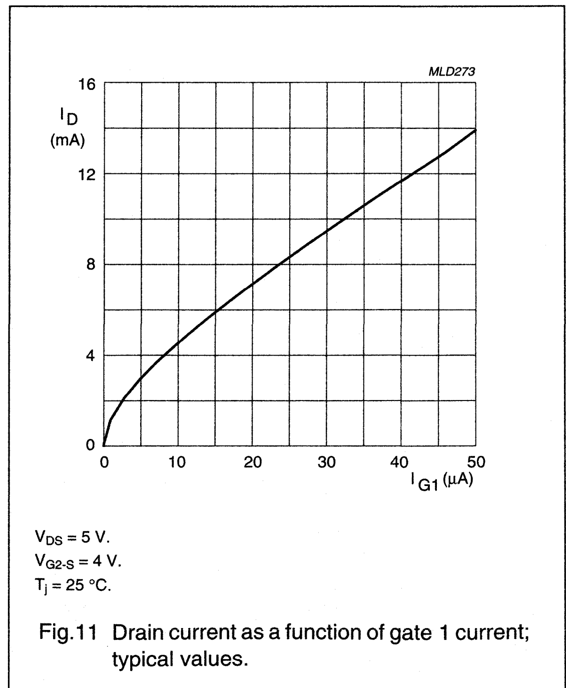
V_{DS} = 5 V.
T_j = 25 °C.

Fig.9 Gate 1 current as a function of gate 1 voltage; typical values.



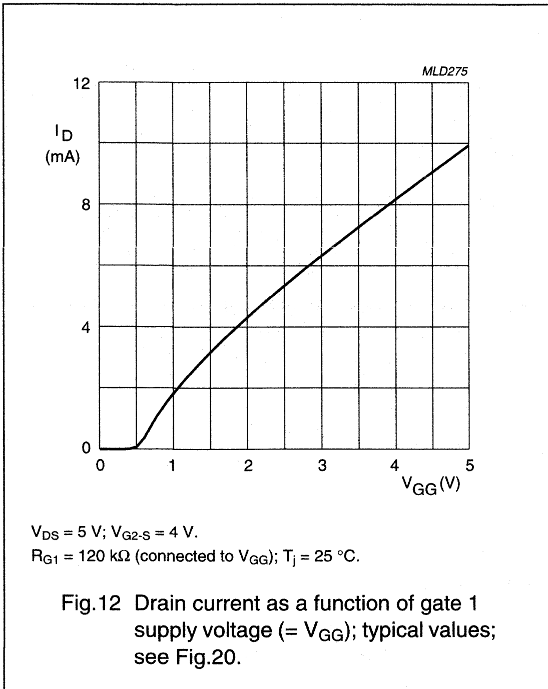
V_{DS} = 5 V.
T_j = 25 °C.

Fig.10 Forward transfer admittance as a function of drain current; typical values.



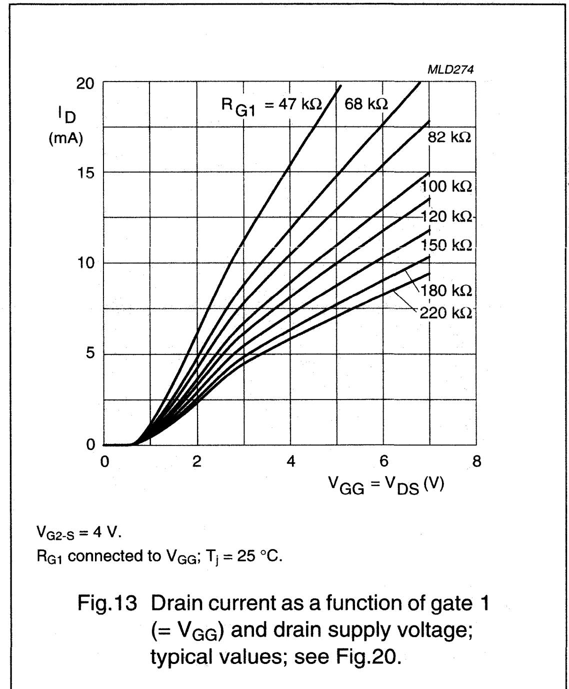
V_{DS} = 5 V.
V_{G2-S} = 4 V.
T_j = 25 °C.

Fig.11 Drain current as a function of gate 1 current; typical values.



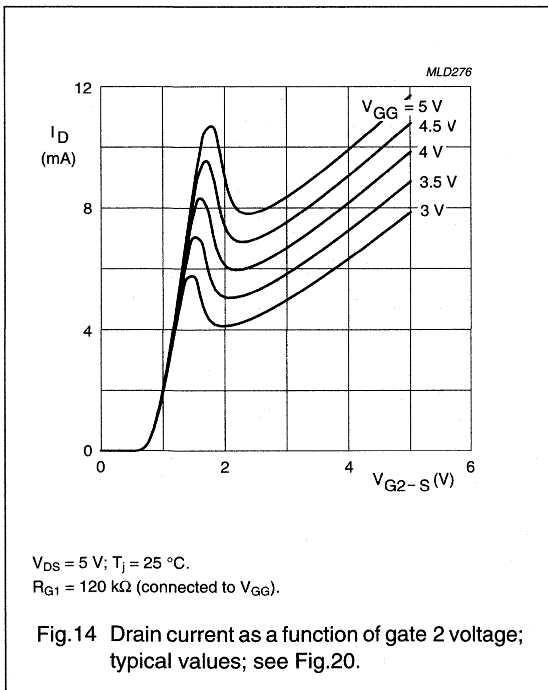
V_{DS} = 5 V; V_{G2-S} = 4 V.
R_{G1} = 120 kΩ (connected to V_{GG}); T_j = 25 °C.

Fig.12 Drain current as a function of gate 1 supply voltage (= V_{GG}); typical values; see Fig.20.



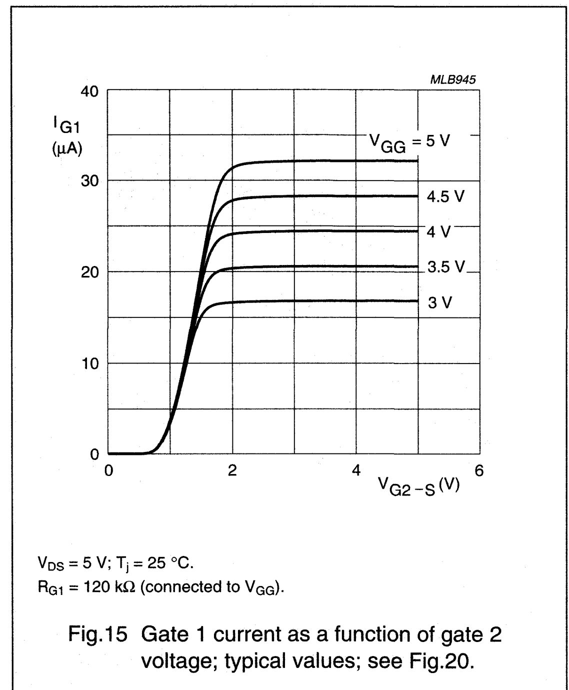
V_{G2-S} = 4 V.
R_{G1} connected to V_{GG}; T_j = 25 °C.

Fig.13 Drain current as a function of gate 1 (= V_{GG}) and drain supply voltage; typical values; see Fig.20.



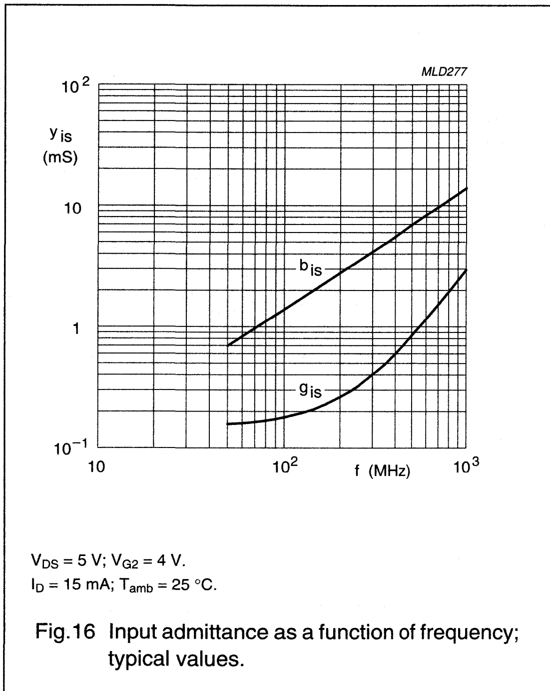
V_{DS} = 5 V; T_j = 25 °C.
R_{G1} = 120 kΩ (connected to V_{GG}).

Fig.14 Drain current as a function of gate 2 voltage; typical values; see Fig.20.



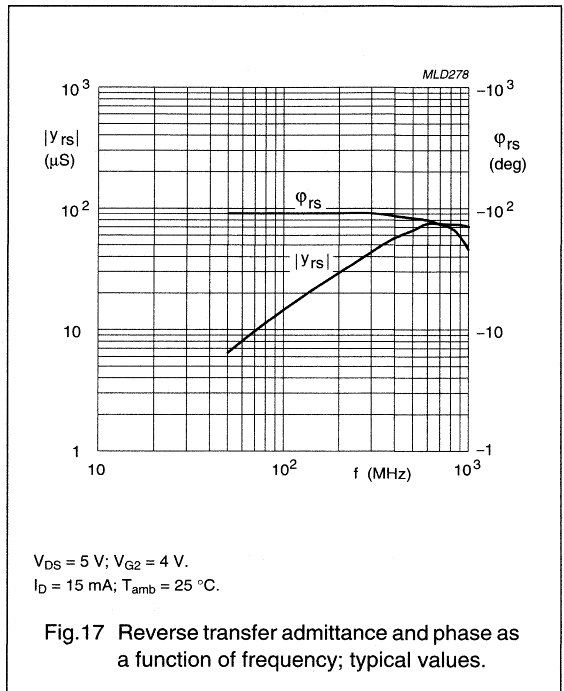
V_{DS} = 5 V; T_j = 25 °C.
R_{G1} = 120 kΩ (connected to V_{GG}).

Fig.15 Gate 1 current as a function of gate 2 voltage; typical values; see Fig.20.



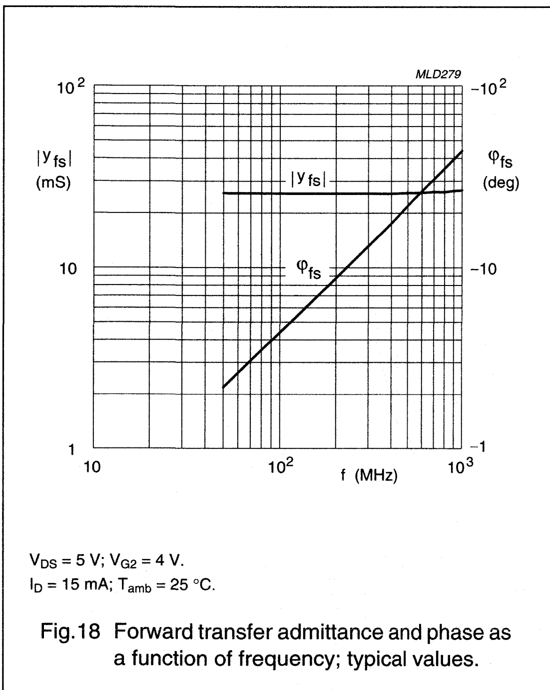
V_{DS} = 5 V; V_{G2} = 4 V.
I_D = 15 mA; T_{amb} = 25 °C.

Fig.16 Input admittance as a function of frequency; typical values.



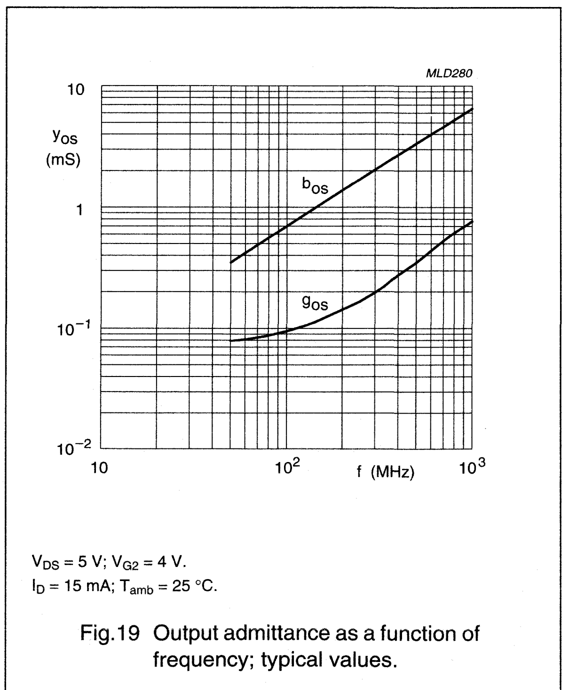
V_{DS} = 5 V; V_{G2} = 4 V.
I_D = 15 mA; T_{amb} = 25 °C.

Fig.17 Reverse transfer admittance and phase as a function of frequency; typical values.



V_{DS} = 5 V; V_{G2} = 4 V.
I_D = 15 mA; T_{amb} = 25 °C.

Fig.18 Forward transfer admittance and phase as a function of frequency; typical values.



V_{DS} = 5 V; V_{G2} = 4 V.
I_D = 15 mA; T_{amb} = 25 °C.

Fig.19 Output admittance as a function of frequency; typical values.

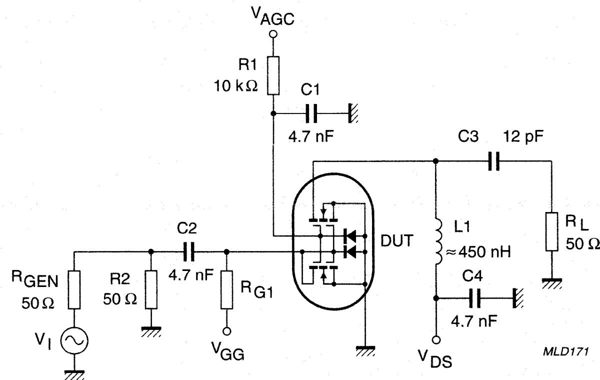


Fig.20 Cross-modulation test set-up.

Table 1 Scattering parameters: V_{DS} =5 V; V_{G2-S} = 4 V; I_D = 10 mA

f (MHz)	s_{11}		s_{21}		s_{12}		s_{22}	
	MAGNITUDE (ratio)	**ANGLE (deg)**	**MAGNITUDE (ratio)**	**ANGLE (deg)**	**MAGNITUDE (ratio)**	**ANGLE (deg)**	**MAGNITUDE (ratio)**	**ANGLE (deg)**
40	0.989	−3.4	2.420	175.7	0.000	79.9	0.993	−1.6
100	0.985	−8.3	2.414	169.1	0.001	78.3	0.992	−3.9
200	0.976	−16.4	2.368	158.8	0.003	80.3	0.987	−7.8
300	0.958	−24.1	2.301	148.5	0.004	73.7	0.980	−11.4
400	0.942	−32.0	2.251	138.8	0.005	70.7	0.974	−15.2
500	0.918	−39.3	2.170	129.5	0.005	67.2	0.966	−18.7
600	0.899	−46.0	2.080	120.7	0.005	67.8	0.958	−22.2
700	0.876	−52.6	2.001	112.1	0.005	68.6	0.951	−25.5
800	0.852	−58.8	1.924	103.2	0.005	72.9	0.944	−28.9
900	0.823	−64.9	1.829	94.7	0.005	78.7	0.937	−32.1
1000	0.800	−70.9	1.747	86.5	0.005	88.3	0.933	−35.2
1200	0.750	−82.4	1.621	70.7	0.005	120.5	0.928	−41.7
1400	0.719	−92.7	1.535	54.6	0.008	139.8	0.930	−48.4
1600	0.682	−102.5	1.424	39.4	0.010	137.8	0.924	−54.9
1800	0.642	−109.8	1.349	22.5	0.013	156.8	0.928	−62.9
2000	0.602	−116.5	1.283	1.1	0.018	175.1	0.928	−73.1
2200	0.547	−124.9	1.130	−15.1	0.014	172.6	0.887	−81.0
2400	0.596	−128.7	1.018	−49.1	0.040	−163.9	0.837	−95.8
2600	0.682	−132.6	0.979	−79.4	0.077	−164.0	0.778	−109.6
2800	0.771	−142.5	0.804	−116.2	0.120	178.8	0.629	−119.5
3000	0.793	−157.5	0.541	−153.5	0.149	158.3	0.479	−119.9

Table 2 Noise data: V_{DS} = 5 V; V_{G2-S} = 4 V; I_D = 10 mA

f (MHz)	F_{min} (dB)	Γ_{opt}		r_n
		(ratio)	**(deg)**	
800	2.00	o.686	49.6	50.40

N-channel dual-gate MOS-FET BF904WR

FEATURES

- Specially designed for use at 5 V supply voltage
- Short channel transistor with high forward transfer admittance to input capacitance ratio
- Low noise gain controlled amplifier up to 1 GHz
- Superior cross-modulation performance during AGC.

APPLICATIONS

- VHF and UHF applications with 3 to 7 V supply voltage such as television tuners and professional communications equipment.

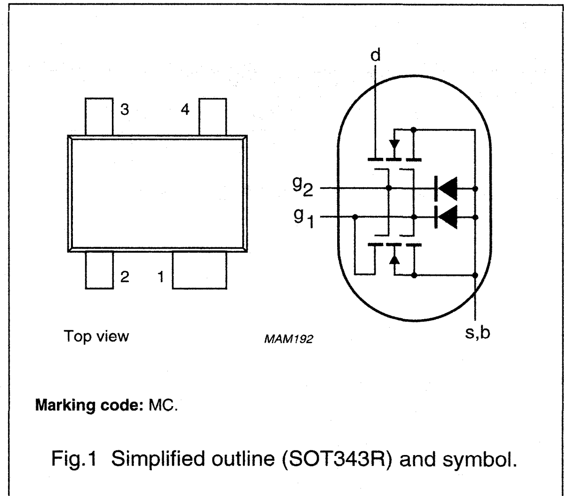
DESCRIPTION

Enhancement type field-effect transistor in a plastic microminiature SOT343R package. The transistor consists of an amplifier MOS-FET with source and substrate interconnected and an internal bias circuit to ensure good cross-modulation performance during AGC.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING

PIN	SYMBOL	DESCRIPTION
1	s, b	source
2	d	drain
3	g_2	gate 2
4	g_1	gate 1



Marking code: MC.

Fig.1 Simplified outline (SOT343R) and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DS}	drain-source voltage		–	–	7	V
I_D	drain current		–	–	30	mA
P_{tot}	total power dissipation		–	–	280	mW
T_j	operating junction temperature		–	–	150	°C
$\lvert y_{fs} \rvert$	forward transfer admittance		22	25	30	mS
C_{ig1-s}	input capacitance at gate 1		–	2.2	2.6	pF
C_{rs}	reverse transfer capacitance	f = 1 MHz	–	25	35	fF
F	noise figure	f = 800 MHz	–	2	–	dB

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	7	V
I_D	drain current		–	30	mA
I_{G1}	gate 1 current		–	±10	mA
I_{G2}	gate 2 current		–	±10	mA
P_{tot}	total power dissipation	up to T_{amb} = 50 °C; see Fig.2; note 1	–	280	mW
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–	+150	°C

Note

1. Device mounted on a printed-circuit board.

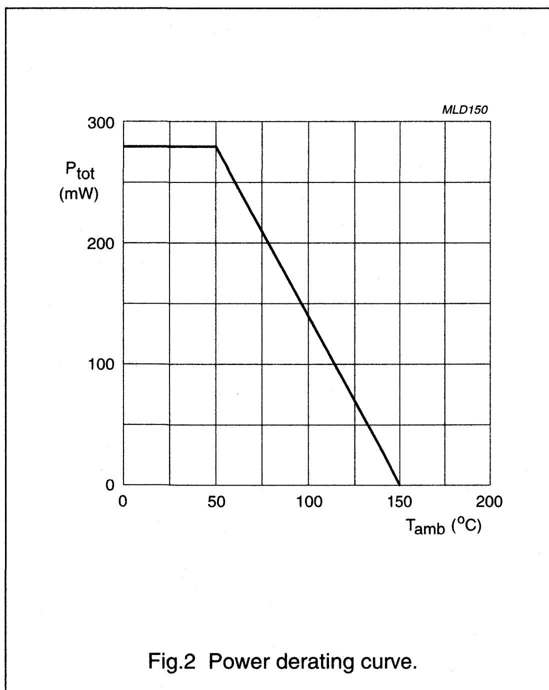


Fig.2 Power derating curve.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	note 1	350	K/W
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	T_s = 91 °C; note 2	210	K/W

Notes

1. Device mounted on a printed-circuit board.
2. T_s is the temperature at the soldering point of the source lead.

STATIC CHARACTERISTICS

T_j = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{(BR)G1\text{-}SS}$	gate 1-source breakdown voltage	$V_{G2\text{-}S} = V_{DS} = 0$; $I_{G1\text{-}S}$ = 10 mA	6	15	V
$V_{(BR)G2\text{-}SS}$	gate 2-source breakdown voltage	$V_{G1\text{-}S} = V_{DS} = 0$; $I_{G2\text{-}S}$ = 10 mA	6	15	V
$V_{(F)S\text{-}G1}$	forward source-gate 1 voltage	$V_{G2\text{-}S} = V_{DS} = 0$; $I_{S\text{-}G1}$ = 10 mA	0.5	1.5	V
$V_{(F)S\text{-}G2}$	forward source-gate 2 voltage	$V_{G1\text{-}S} = V_{DS} = 0$; $I_{S\text{-}G2}$ = 10 mA	0.5	1.5	V
$V_{G1\text{-}S(th)}$	gate 1-source threshold voltage	$V_{G2\text{-}S}$ = 4V; V_{DS} = 5 V; I_D = 20 μA	0.3	1	V
$V_{G2\text{-}S(th)}$	gate 2-source threshold voltage	$V_{G1\text{-}S} = V_{DS}$ = 5 V; I_D = 20 μA	0.3	1.2	V
I_{DSX}	drain-source current	$V_{G2\text{-}S}$ = 4 V; V_{DS} = 5 V; R_{G1} = 120 kΩ; note 1	8	13	mA
$I_{G1\text{-}SS}$	gate 1 cut-off current	$V_{G2\text{-}S} = V_{DS} = 0$; $V_{G1\text{-}S}$ = 5 V	–	50	nA
$I_{G2\text{-}SS}$	gate 2 cut-off current	$V_{G1\text{-}S} = V_{DS} = 0$; $V_{G2\text{-}S}$ = 5 V	–	50	nA

Note

1. R_G connects gate 1 to V_{GG} = 5 V.

DYNAMIC CHARACTERISTICS

Common source; T_{amb} = 25 °C; V_{DS} = 5 V; $V_{G2\text{-}S}$ = 4 V; I_D = 10 mA; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\lvert y_{fs} \rvert$	forward transfer admittance	pulsed; T_j = 25 °C	22	25	30	mS
$C_{ig1\text{-}s}$	input capacitance at gate 1	f = 1 MHz	–	2.2	2.6	pF
$C_{ig2\text{-}s}$	input capacitance at gate 2	f = 1 MHz	1	1.5	2	pF
C_{os}	drain-source capacitance	f = 1 MHz	1	1.3	1.6	pF
C_{rs}	reverse transfer capacitance	f = 1 MHz	–	25	35	fF
F	noise figure	f = 200 MHz; G_S = 2 mS; $B_S = B_{Sopt}$	–	1	1.5	dB
		f = 800 MHz; $G_S = G_{Sopt}$; $B_S = B_{Sopt}$	–	2	2.8	dB

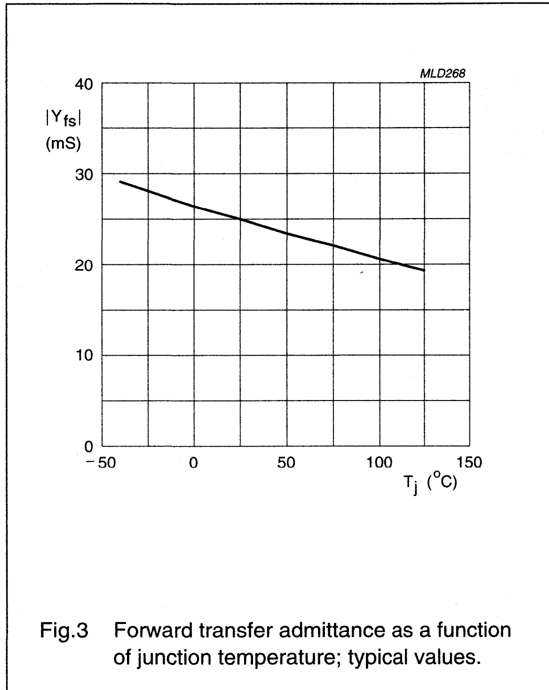
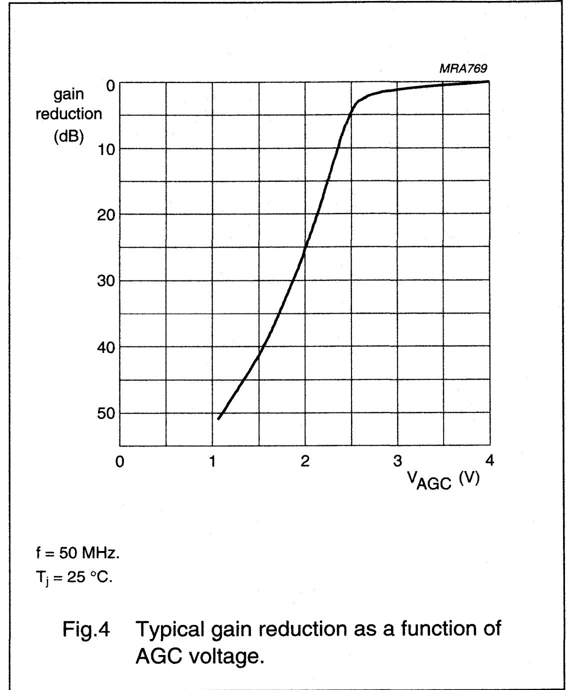
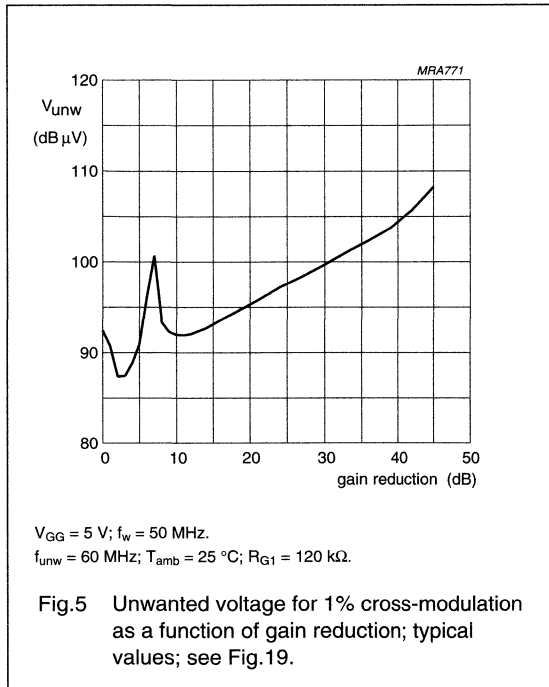


Fig.3 Forward transfer admittance as a function of junction temperature; typical values.



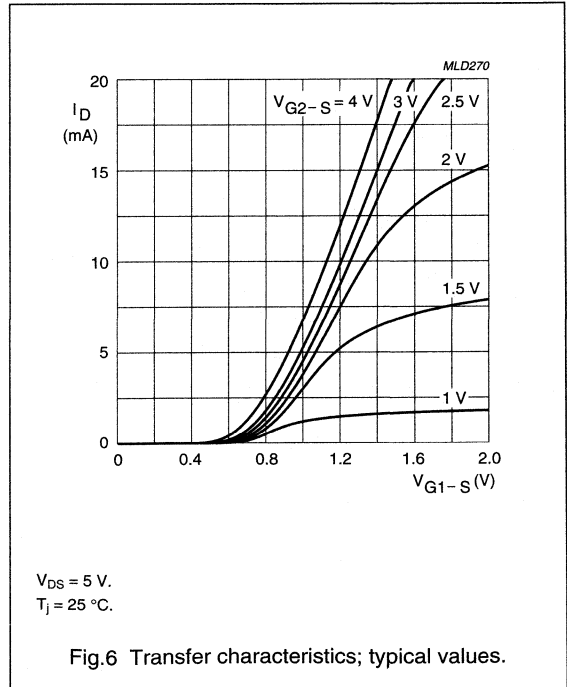
f = 50 MHz.
T_j = 25 °C.

Fig.4 Typical gain reduction as a function of AGC voltage.



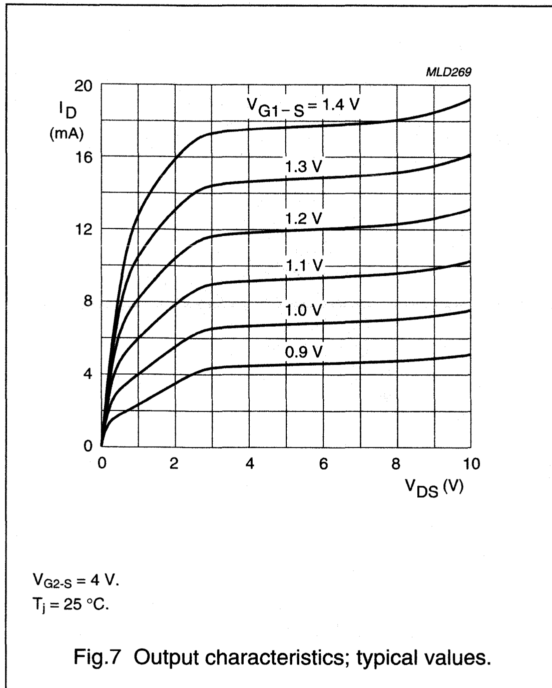
V_{GG} = 5 V; f_w = 50 MHz.
f_{unw} = 60 MHz; T_{amb} = 25 °C; R_{G1} = 120 kΩ.

Fig.5 Unwanted voltage for 1% cross-modulation as a function of gain reduction; typical values; see Fig.19.



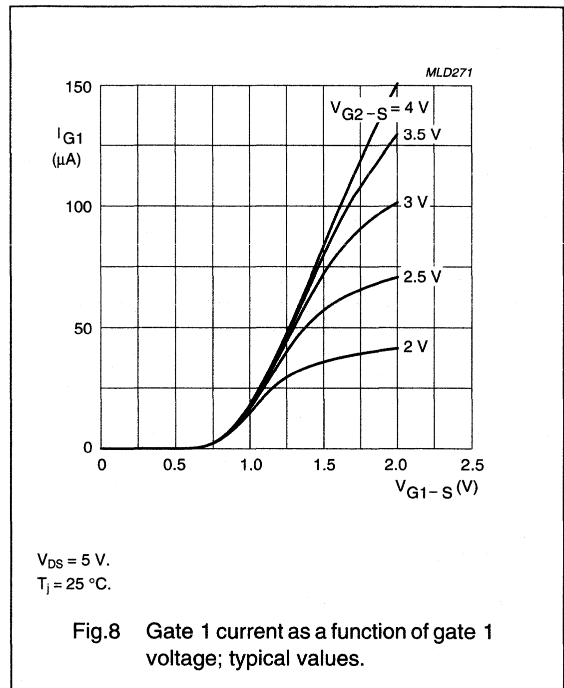
V_{DS} = 5 V.
T_j = 25 °C.

Fig.6 Transfer characteristics; typical values.



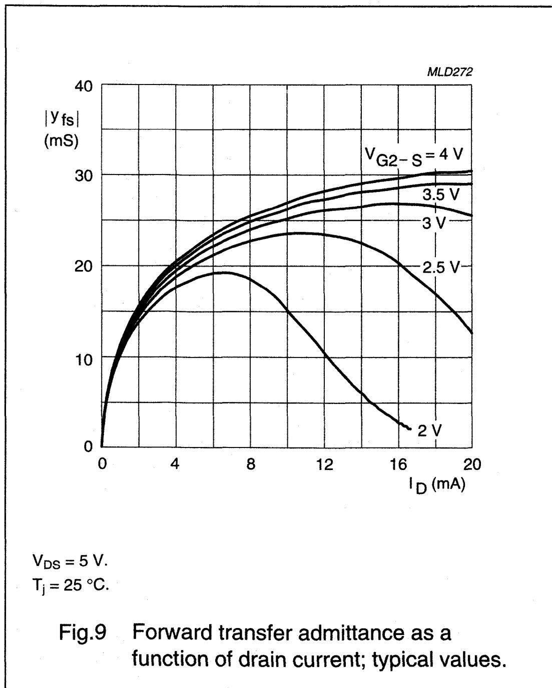
V_{G2-S} = 4 V.
T_j = 25 °C.

Fig.7 Output characteristics; typical values.



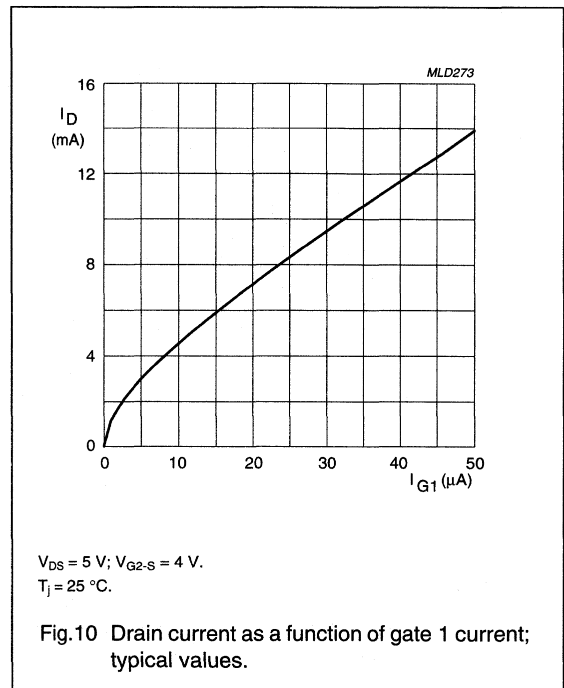
V_{DS} = 5 V.
T_j = 25 °C.

Fig.8 Gate 1 current as a function of gate 1 voltage; typical values.



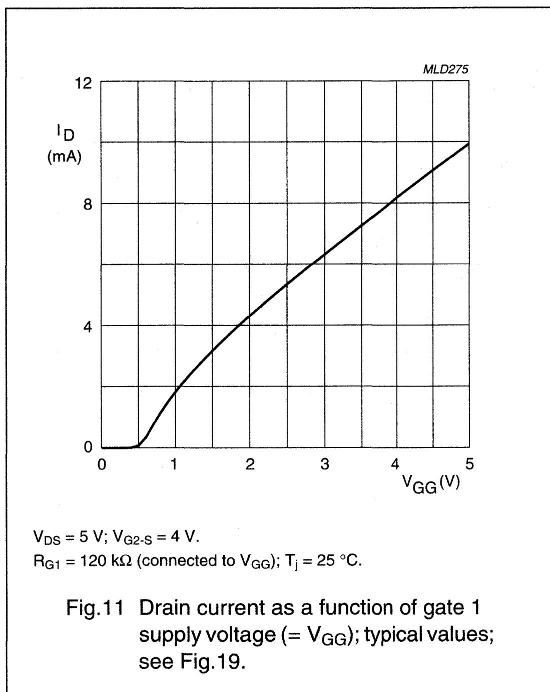
V_{DS} = 5 V.
T_j = 25 °C.

Fig.9 Forward transfer admittance as a function of drain current; typical values.



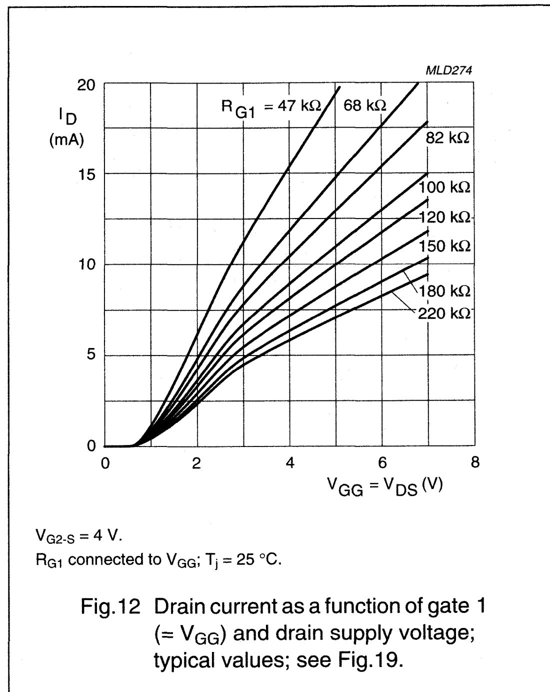
V_{DS} = 5 V; V_{G2-S} = 4 V.
T_j = 25 °C.

Fig.10 Drain current as a function of gate 1 current; typical values.



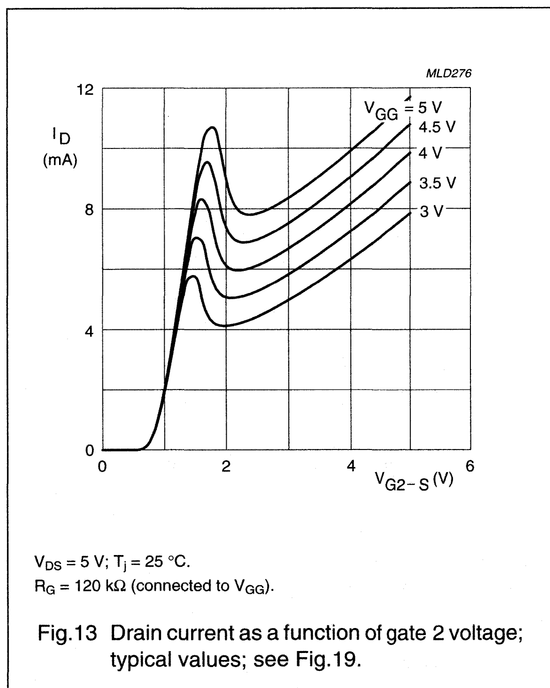
V_{DS} = 5 V; V_{G2-S} = 4 V.
R_{G1} = 120 kΩ (connected to V_{GG}); T_j = 25 °C.

Fig.11 Drain current as a function of gate 1 supply voltage (= V_{GG}); typical values; see Fig.19.



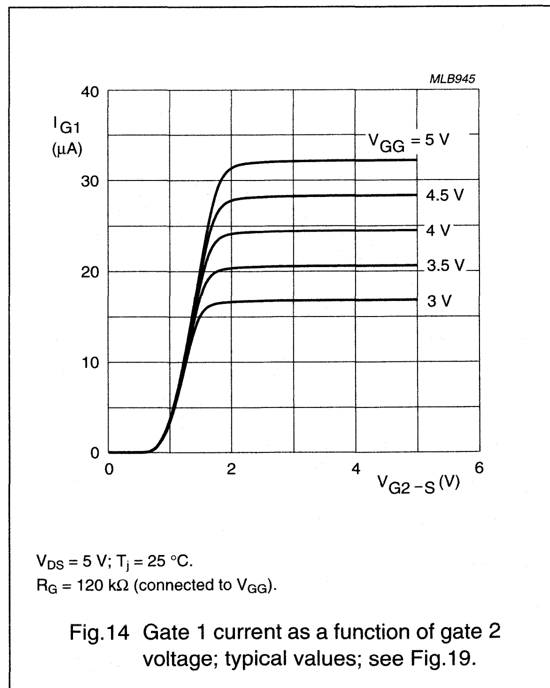
V_{G2-S} = 4 V.
R_{G1} connected to V_{GG}; T_j = 25 °C.

Fig.12 Drain current as a function of gate 1 (= V_{GG}) and drain supply voltage; typical values; see Fig.19.



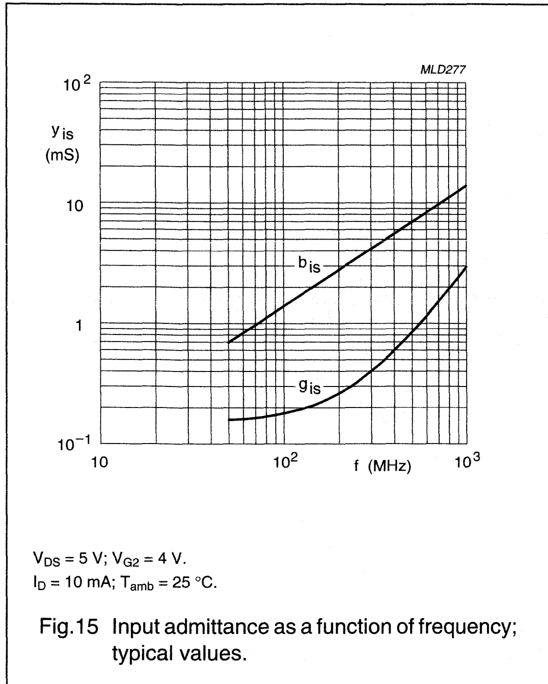
V_{DS} = 5 V; T_j = 25 °C.
R_G = 120 kΩ (connected to V_{GG}).

Fig.13 Drain current as a function of gate 2 voltage; typical values; see Fig.19.



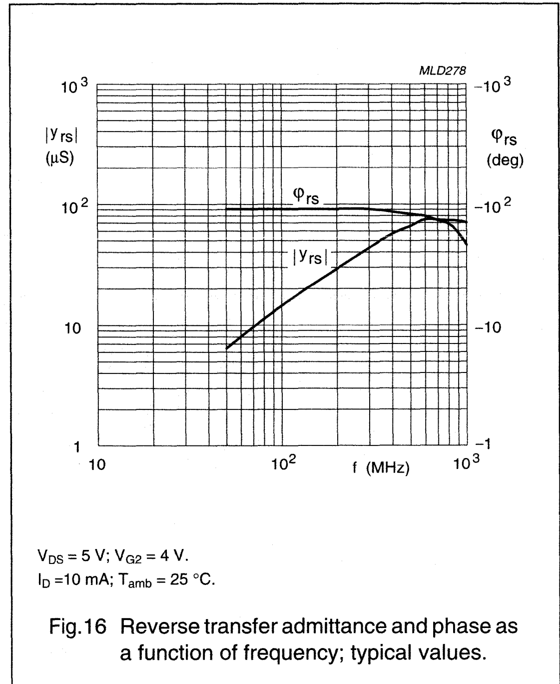
V_{DS} = 5 V; T_j = 25 °C.
R_G = 120 kΩ (connected to V_{GG}).

Fig.14 Gate 1 current as a function of gate 2 voltage; typical values; see Fig.19.



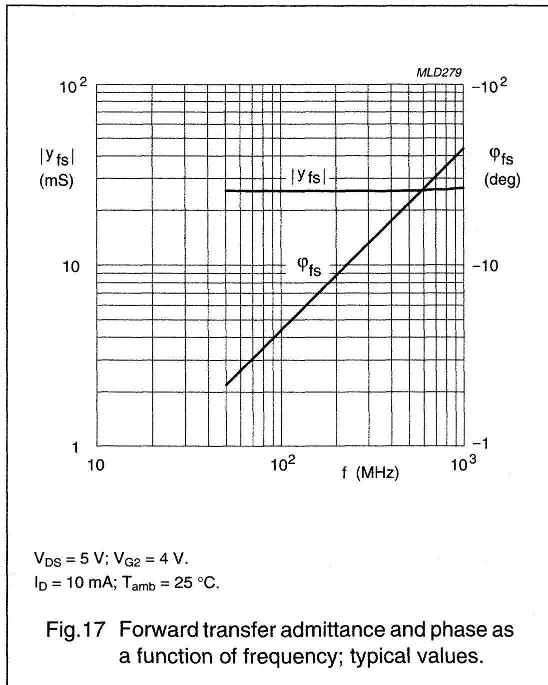
V_{DS} = 5 V; V_{G2} = 4 V.
I_D = 10 mA; T_{amb} = 25 °C.

Fig.15 Input admittance as a function of frequency; typical values.



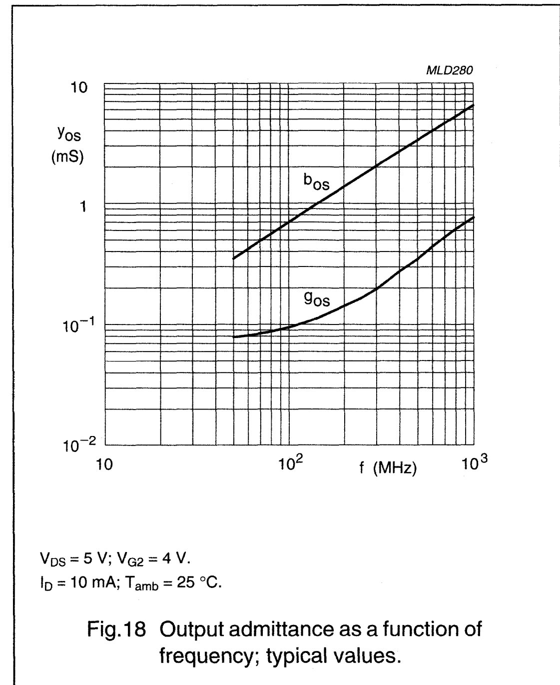
V_{DS} = 5 V; V_{G2} = 4 V.
I_D =10 mA; T_{amb} = 25 °C.

Fig.16 Reverse transfer admittance and phase as a function of frequency; typical values.



V_{DS} = 5 V; V_{G2} = 4 V.
I_D = 10 mA; T_{amb} = 25 °C.

Fig.17 Forward transfer admittance and phase as a function of frequency; typical values.



V_{DS} = 5 V; V_{G2} = 4 V.
I_D = 10 mA; T_{amb} = 25 °C.

Fig.18 Output admittance as a function of frequency; typical values.

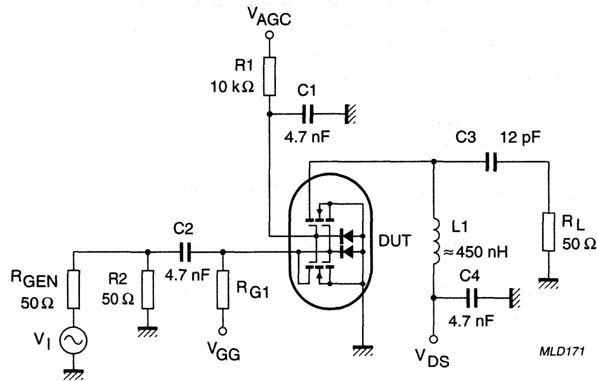


Fig.19 Cross-modulation test set-up.

Table 1 Scattering parameters: V_{DS} =5 V; V_{G2-S} = 4 V; I_D = 10 mA

f (MHz)	s_{11}		s_{21}		s_{12}		s_{22}	
	MAGNITUDE (ratio)	**ANGLE (deg)**	**MAGNITUDE (ratio)**	**ANGLE (deg)**	**MAGNITUDE (ratio)**	**ANGLE (deg)**	**MAGNITUDE (ratio)**	**ANGLE (deg)**
40	0.989	−3.4	2.420	175.7	0.000	79.9	0.993	−1.6
100	0.985	−8.3	2.414	169.1	0.001	78.3	0.992	−3.9
200	0.976	−16.4	2.368	158.8	0.003	80.3	0.987	−7.8
300	0.958	−24.1	2.301	148.5	0.004	73.7	0.980	−11.4
400	0.942	−32.0	2.251	138.8	0.005	70.7	0.974	−15.2
500	0.918	−39.3	2.170	129.5	0.005	67.2	0.966	−18.7
600	0.899	−46.0	2.080	120.7	0.005	67.8	0.958	−22.2
700	0.876	−52.6	2.001	112.1	0.005	68.6	0.951	−25.5
800	0.852	−58.8	1.924	103.2	0.005	72.9	0.944	−28.9
900	0.823	−64.9	1.829	94.7	0.005	78.7	0.937	−32.1
1000	0.800	−70.9	1.747	86.5	0.005	88.3	0.933	−35.2
1200	0.750	−82.4	1.621	70.7	0.005	120.5	0.928	−41.7
1400	0.719	−92.7	1.535	54.6	0.008	139.8	0.930	−48.4
1600	0.682	−102.5	1.424	39.4	0.010	137.8	0.924	−54.9
1800	0.642	−109.8	1.349	22.5	0.013	156.8	0.928	−62.9
2000	0.602	−116.5	1.283	1.1	0.018	175.1	0.928	−73.1
2200	0.547	−124.9	1.130	−15.1	0.014	172.6	0.887	−81.0
2400	0.596	−128.7	1.018	−49.1	0.040	−163.9	0.837	−95.8
2600	0.682	−132.6	0.979	−79.4	0.077	−164.0	0.778	−109.6
2800	0.771	−142.5	0.804	−116.2	0.120	178.8	0.629	−119.5
3000	0.793	−157.5	0.541	−153.5	0.149	158.3	0.479	−119.9

Table 2 Noise data: V_{DS} = 5 V; V_{G2-S} = 4 V; I_D = 10 mA

f (MHz)	F_{min} (dB)	Γ_{opt}		r_n
		(ratio)	**(deg)**	
800	2.00	.686	49.6	50.40

FEATURES

- High forward transfer admittance
- Short channel transistor with high forward transfer admittance to input capacitance ratio
- Low noise gain controlled amplifier up to 1 GHz.

APPLICATIONS

- VHF and UHF applications with 12 V supply voltage, such as television tuners and professional communications equipment.

DESCRIPTION

Depletion type field-effect transistor in a plastic microminiature SOT143 or SOT143R package. The transistors are protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING

PIN	SYMBOL	DESCRIPTION
1	s, b	source
2	d	drain
3	g_2	gate 2
4	g_1	gate 1

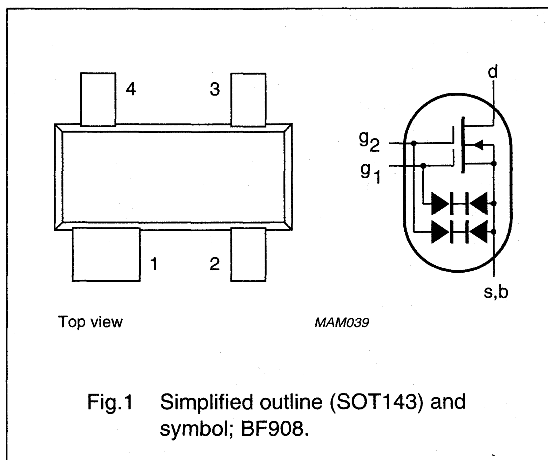


Fig.1 Simplified outline (SOT143) and symbol; BF908.

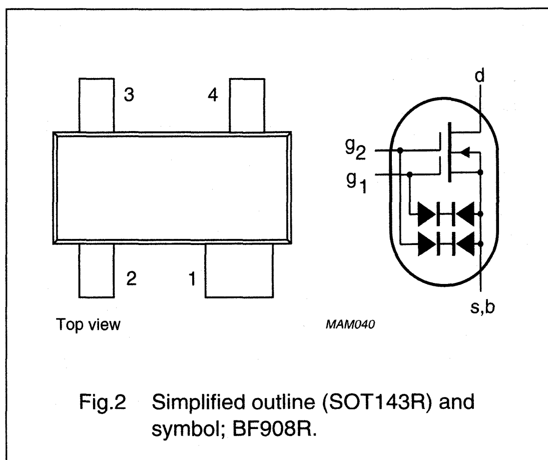


Fig.2 Simplified outline (SOT143R) and symbol; BF908R.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DS}	drain-source voltage		–	–	12	V
I_D	drain current		–	–	40	mA
P_{tot}	total power dissipation		–	–	200	mW
T_j	operating junction temperature		–	–	150	°C
$\|y_{fs}\|$	forward transfer admittance		36	43	50	mS
C_{ig1-s}	input capacitance at gate 1		2.4	3.1	4	pF
C_{rs}	reverse transfer capacitance	f = 1 MHz	20	30	45	pF
F	noise figure	f = 800 MHz	–	1.5	2.5	dB

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	12	V
I_D	drain current		–	40	mA
$\pm I_{G1}$	gate 1 current		–	10	mA
$\pm I_{G2}$	gate 2 current		–	10	mA
P_{tot}	total power dissipation	see Fig.3; note 1			
	BF908	up to T_{amb} = 50 °C	–	200	mW
	BF908R	up to T_{amb} = 40 °C	–	200	mW
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–	150	°C

Note

1. Device mounted on a printed-circuit board.

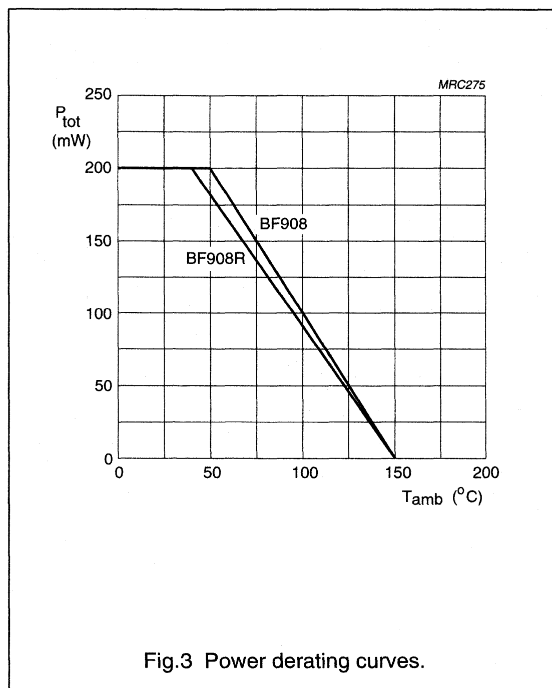


Fig.3 Power derating curves.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	note 1		
	BF908		500	K/W
	BF908R		550	K/W

Note

1. Device mounted on a printed-circuit board.

STATIC CHARACTERISTICS

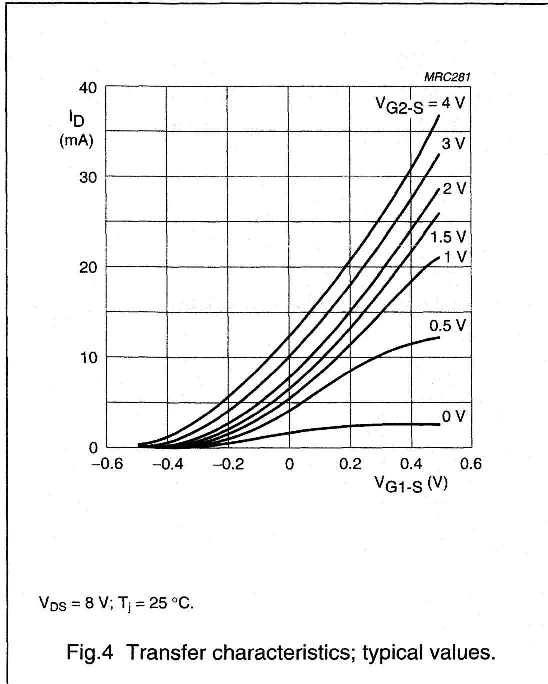
T_j = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\pm V_{(BR)G1\text{-}SS}$	gate 1-source breakdown voltage	$V_{G2\text{-}S} = V_{DS} = 0$; $I_{G1\text{-}S} = 10$ mA	8	–	20	V
$\pm V_{(BR)G2\text{-}SS}$	gate 2-source breakdown voltage	$V_{G1\text{-}S} = V_{DS} = 0$; $I_{G2\text{-}S} = 10$ mA	8	–	20	V
$-V_{(P)G1\text{-}S}$	gate 1-source cut-off voltage	$V_{G2\text{-}S} = 4$ V; $V_{DS} = 8$ V; $I_D = 20$ μA	–	–	2	V
$-V_{(P)G2\text{-}S}$	gate 2-source cut-off voltage	$V_{G1\text{-}S} = 4$ V; $V_{DS} = 8$ V; $I_D = 20$ μA	–	–	1.5	V
I_{DSS}	drain-source current	$V_{G2\text{-}S} = 4$ V; $V_{DS} = 8$ V; $V_{G1\text{-}S} = 0$	3	15	27	mA
$\pm I_{G1\text{-}SS}$	gate 1 cut-off current	$V_{G2\text{-}S} = V_{DS} = 0$; $V_{G1\text{-}S} = 5$ V	–	–	50	nA
$\pm I_{G2\text{-}SS}$	gate 2 cut-off current	$V_{G1\text{-}S} = V_{DS} = 0$; $V_{G2\text{-}S} = 5$ V	–	–	50	nA

DYNAMIC CHARACTERISTICS

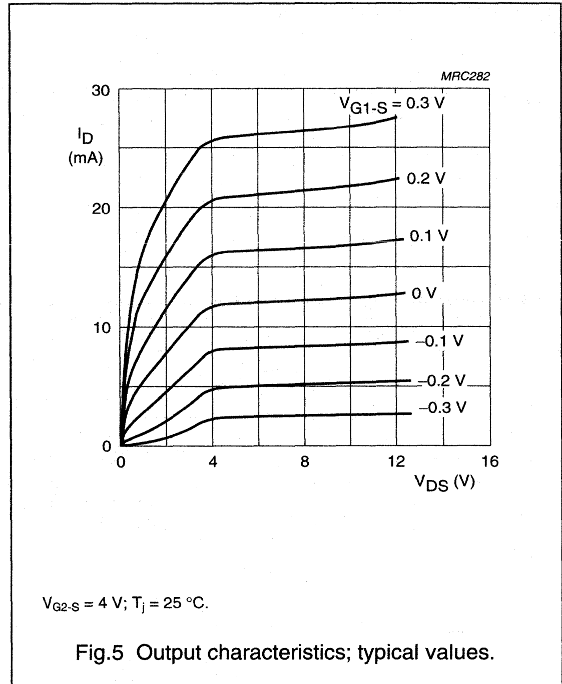
Common source; T_{amb} = 25 °C; V_{DS} = 8 V; $V_{G2\text{-}S}$ = 4 V; I_D = 15 mA; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\lvert y_{fs} \rvert$	forward transfer admittance	pulsed; T_j = 25 °C; f = 1 MHz	36	43	50	mS
$C_{ig1\text{-}s}$	input capacitance at gate 1	f = 1 MHz	2.4	3.1	4	pF
$C_{ig2\text{-}s}$	input capacitance at gate 2	f = 1 MHz	1.2	1.8	2.5	pF
C_{os}	output capacitance	f = 1 MHz	1.2	1.7	2.2	pF
C_{rs}	reverse transfer capacitance	f = 1 MHz	20	30	45	fF
F	noise figure	f = 200 MHz; G_S = 2 mS; $B_S = B_{Sopt}$	–	0.6	1.2	dB
		f = 800 MHz; $G_S = G_{Sopt}$; $B_S = B_{Sopt}$	–	1.5	2.5	dB



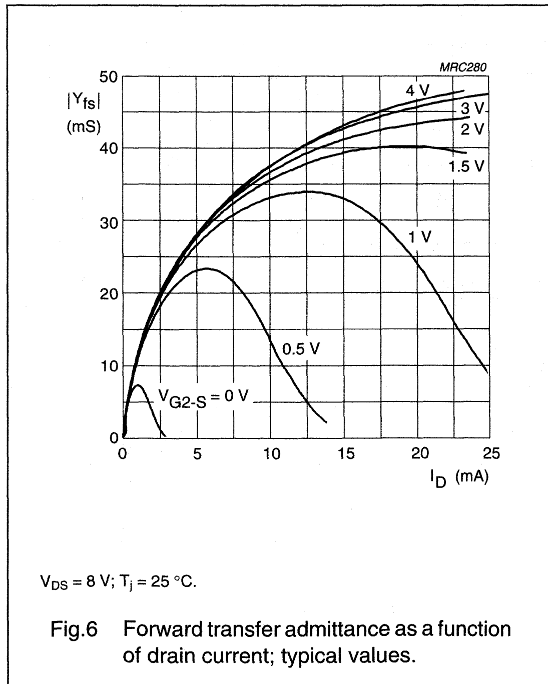
V_{DS} = 8 V; T_j = 25 °C.

Fig.4 Transfer characteristics; typical values.



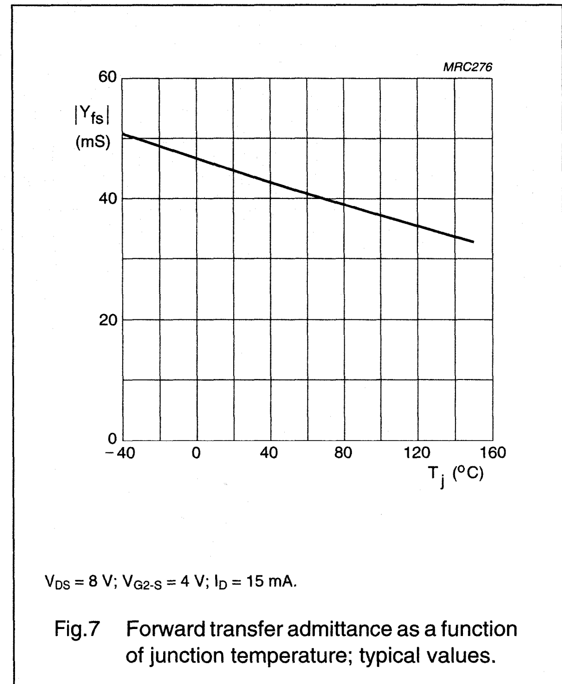
V_{G2-S} = 4 V; T_j = 25 °C.

Fig.5 Output characteristics; typical values.



V_{DS} = 8 V; T_j = 25 °C.

Fig.6 Forward transfer admittance as a function of drain current; typical values.



V_{DS} = 8 V; V_{G2-S} = 4 V; I_D = 15 mA.

Fig.7 Forward transfer admittance as a function of junction temperature; typical values.

Table 1 Scattering parameters

f (MHz)	s_{11} MAGNITUDE (ratio)	s_{11} ANGLE (deg)	s_{21} MAGNITUDE (ratio)	s_{21} ANGLE (deg)	s_{12} MAGNITUDE (ratio)	s_{12} ANGLE (deg)	s_{22} MAGNITUDE (ratio)	s_{22} ANGLE (deg)
V_{DS} = 8 V; V_{G2-S} = 4 V; I_D = 10 mA; T_{amb} = 25 °C.								
50	0.998	−5.1	3.537	173.5	0.001	98.2	0.996	−2.4
100	0.994	−10.4	3.502	167.7	0.001	88.8	0.994	−4.9
200	0.979	−20.8	3.450	154.9	0.003	74.6	0.987	−9.5
300	0.962	−30.3	3.318	143.7	0.004	69.5	0.983	−13.9
400	0.939	−40.1	3.234	131.9	0.005	65.6	0.980	−18.5
500	0.914	−49.1	3.093	120.7	0.006	64.4	0.974	−22.8
600	0.892	−57.1	2.912	111.1	0.005	63.1	0.969	−27.0
700	0.865	−64.4	2.774	101.0	0.005	65.2	0.966	−31.2
800	0.837	−71.6	2.616	91.4	0.004	70.8	0.965	−35.4
900	0.811	−78.1	2.479	81.9	0.004	87.4	0.965	−39.4
1000	0.785	−84.5	3.329	72.5	0.003	108.0	0.966	−43.7
V_{DS} = 8 V; V_{G2-S} = 4 V; I_D = 15 mA; T_{amb} = 25 °C.								
50	0.998	−5.3	3.983	173.4	0.001	95.5	0.994	−2.4
100	0.994	−10.9	3.943	167.5	0.001	93.6	0.991	−5.0
200	0.976	−21.6	3.878	154.7	0.003	74.3	0.984	−9.7
300	0.957	−31.7	3.722	143.3	0.004	70.0	0.979	−14.2
400	0.934	−41.7	3.614	131.6	0.005	63.5	0.975	−18.8
500	0.907	−51.1	3.446	120.4	0.006	62.2	0.969	−23.2
600	0.885	−59.1	3.240	110.9	0.005	59.6	0.964	−27.4
700	0.851	−66.8	3.072	100.9	0.005	64.8	0.961	−31.6
800	0.826	−73.9	2.891	91.3	0.004	67.8	0.959	−35.9
900	0.797	−80.7	2.733	81.9	0.004	85.0	0.958	−40.0
1000	0.773	−87.0	2.569	72.8	0.004	102.9	0.958	−44.2

Table 2 Noise data

f (MHz)	F_{min} (dB)	Γ_{opt} (ratio)	Γ_{opt} (deg)	r_n
V_{DS} = 8 V; V_{G2-S} = 4 V; I_D = 10 mA; T_{amb} = 25 °C.				
800	1.50	0.720	56.7	0.580
V_{DS} = 8 V; V_{G2-S} = 4 V; I_D = 15 mA; T_{amb} = 25 °C.				
800	1.50	0.700	59.2	0.520

N-channel dual-gate MOS-FET BF908WR

FEATURES

- High forward transfer admittance
- Short channel transistor with high forward transfer admittance to input capacitance ratio
- Low noise gain controlled amplifier up to 1 GHz.

APPLICATIONS

- VHF and UHF applications with 12 V supply voltage, such as television tuners and professional communications equipment.

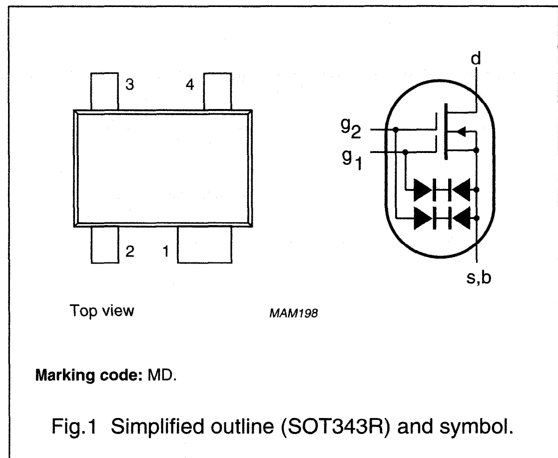
DESCRIPTION

Depletion type field effect transistor in a plastic microminiature SOT343R package. The transistor is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING

PIN	SYMBOL	DESCRIPTION
1	s, b	source
2	d	drain
3	g_2	gate 2
4	g_1	gate 1



Marking code: MD.

Fig.1 Simplified outline (SOT343R) and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DS}	drain-source voltage		–	–	12	V
I_D	drain current		–	–	40	mA
P_{tot}	total power dissipation		–	–	300	mW
T_j	operating junction temperature		–	–	150	°C
$\lvert y_{fs} \rvert$	forward transfer admittance		36	43	50	mS
C_{ig1-s}	input capacitance at gate 1		2.4	3.1	4	pF
C_{rs}	reverse transfer capacitance	f = 1 MHz	20	30	45	fF
F	noise figure	f = 800 MHz	–	1.5	2.5	dB

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	12	V
I_D	drain current		–	40	mA
I_{G1}	gate 1 current		–	±10	mA
I_{G2}	gate 2 current		–	±10	mA
P_{tot}	total power dissipation	up to T_{amb} = 45 °C; see Fig.2; note 1	–	300	mW
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–	+150	°C

Note

1. Device mounted on a printed-circuit board.

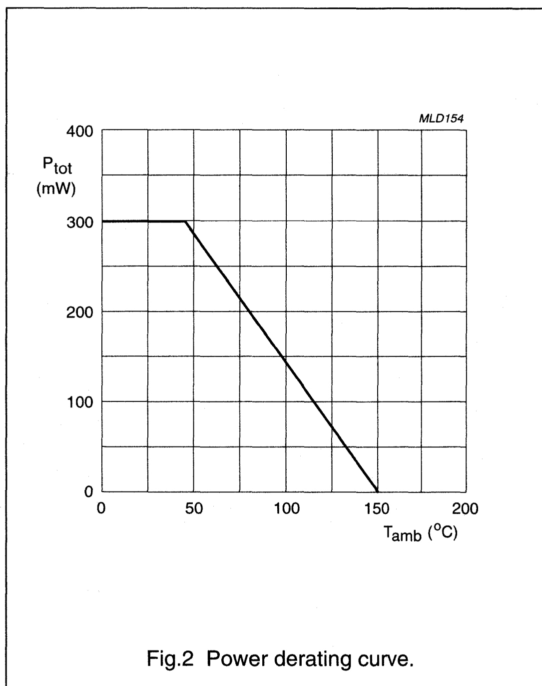


Fig.2 Power derating curve.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	note 1	350	K/W
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	T_s = 87 °C; note 2	210	K/W

Notes

1. Device mounted on a printed-circuit board.
2. T_s is the temperature at the soldering point of the source lead.

STATIC CHARACTERISTICS

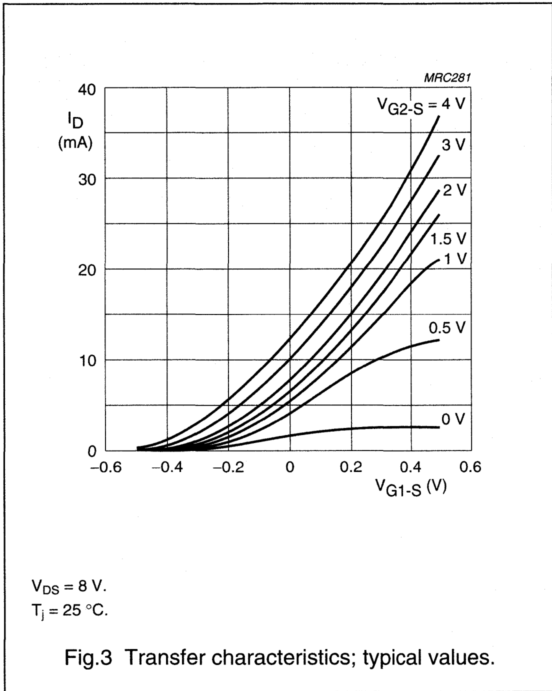
T_j = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)G1\text{-}SS}$	gate 1-source breakdown voltage	$V_{G2\text{-}S} = V_{DS} = 0$; $I_{G1\text{-}S}$ = 10 mA	8	–	20	V
$V_{(BR)G2\text{-}SS}$	gate 2-source breakdown voltage	$V_{G1\text{-}S} = V_{DS} = 0$; $I_{G2\text{-}S}$ = 10 mA	8	–	20	V
$V_{(P)G1\text{-}S}$	gate 1-source cut-off voltage	$V_{G2\text{-}S}$ = 4 V; V_{DS} = 8 V; I_D = 20 μA	–	–	−2	V
$V_{(P)G2\text{-}S}$	gate 2-source cut-off voltage	$V_{G1\text{-}S}$ = 4 V; V_{DS} = 8 V; I_D = 20 μA	–	–	−1.5	V
I_{DSS}	drain-source current	$V_{G2\text{-}S}$ = 4 V; V_{DS} = 8 V; $V_{G1\text{-}S}$ = 0	3	15	27	mA
$I_{G1\text{-}SS}$	gate 1 cut-off current	$V_{G2\text{-}S} = V_{DS} = 0$; $V_{G1\text{-}S}$ = 5 V	–	–	50	nA
$I_{G2\text{-}SS}$	gate 2 cut-off current	$V_{G1\text{-}S} = V_{DS} = 0$; $V_{G2\text{-}S}$ = 5 V	–	–	50	nA

DYNAMIC CHARACTERISTICS

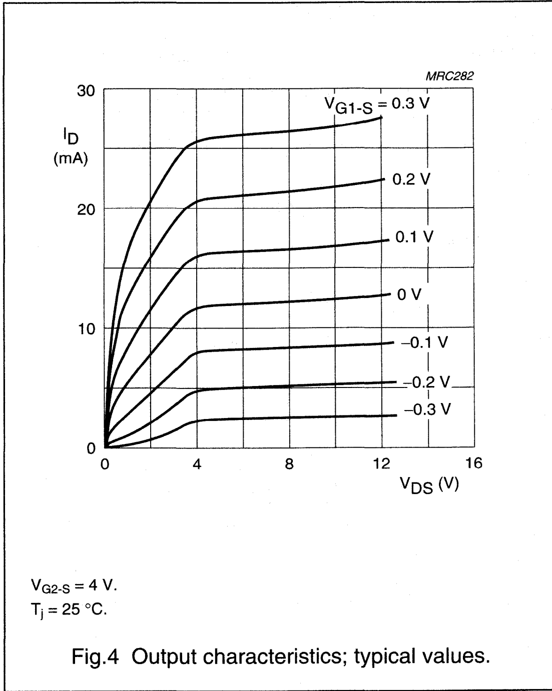
Common source; T_{amb} = 25 °C; V_{DS} = 8 V; $V_{G2\text{-}S}$ = 4 V; I_D = 15 mA; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\lvert y_{fs} \rvert$	forward transfer admittance	pulsed; T_j = 25 °C	36	43	50	mS
$C_{ig1\text{-}s}$	input capacitance at gate 1	f = 1 MHz	2.4	3.1	4	pF
$C_{ig2\text{-}s}$	input capacitance at gate 2	f = 1 MHz	1.2	1.8	2.5	pF
C_{os}	drain-source capacitance	f = 1 MHz	1.2	1.7	2.2	pF
C_{rs}	reverse transfer capacitance	f = 1 MHz	20	30	45	fF
F	noise figure	f = 200 MHz; G_S = 2 mS; $B_S = B_{Sopt}$	–	0.6	1.2	dB
		f = 800 MHz; $G_S = G_{Sopt}$; $B_S = B_{Sopt}$	–	1.5	2.5	dB



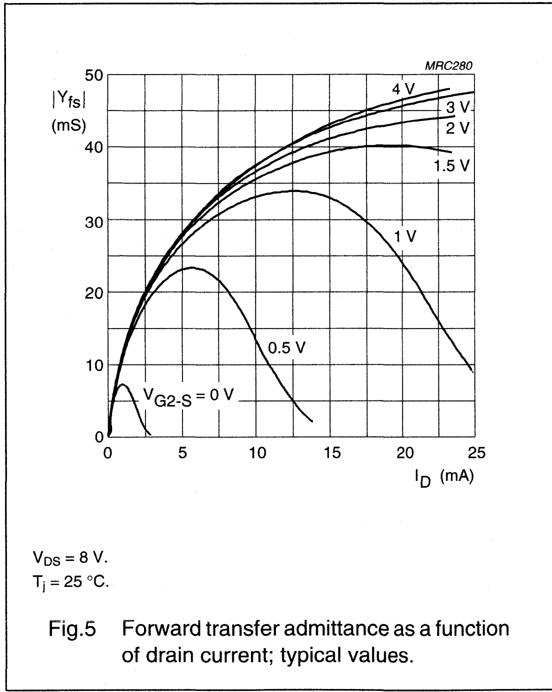
V_{DS} = 8 V.
T_j = 25 °C.

Fig.3 Transfer characteristics; typical values.



V_{G2-S} = 4 V.
T_j = 25 °C.

Fig.4 Output characteristics; typical values.



V_{DS} = 8 V.
T_j = 25 °C.

Fig.5 Forward transfer admittance as a function of drain current; typical values.

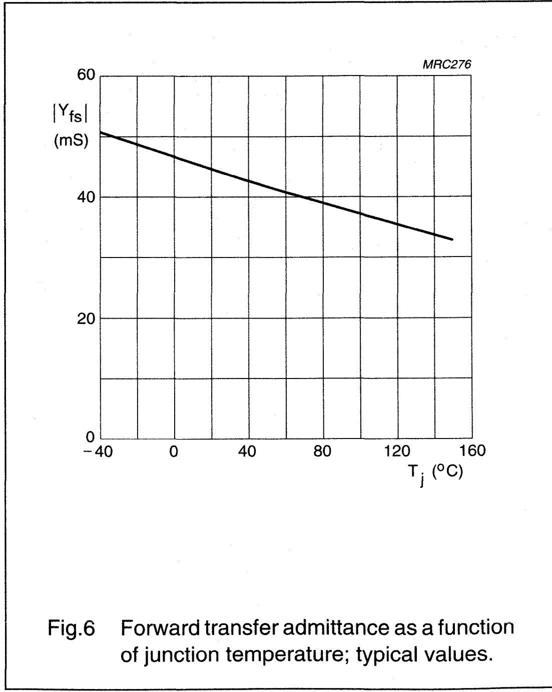


Fig.6 Forward transfer admittance as a function of junction temperature; typical values.

N-channel dual gate MOS-FETs BF909; BF909R

FEATURES

- Specially designed for use at 5 V supply voltage
- High forward transfer admittance
- Short channel transistor with high forward transfer admittance to input capacitance ratio
- Low noise gain controlled amplifier up to 1 GHz
- Superior cross-modulation performance during AGC.

APPLICATIONS

- VHF and UHF applications with 3 to 7 V supply voltage such as television tuners and professional communications equipment.

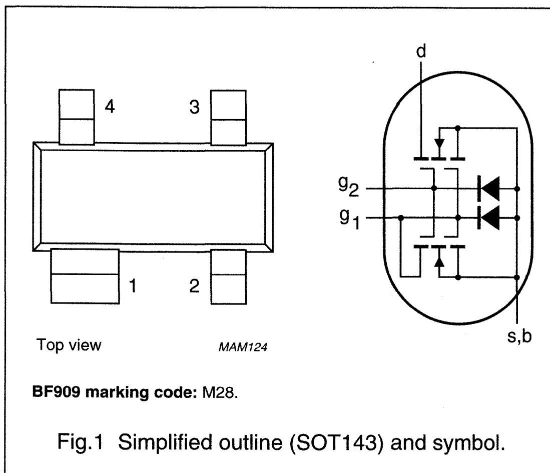
DESCRIPTION

Enhancement type field-effect transistor in a plastic microminiature SOT143 or SOT143R package. The transistor consists of an amplifier MOS-FET with source and substrate interconnected and an internal bias circuit to ensure good cross-modulation performance during AGC.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

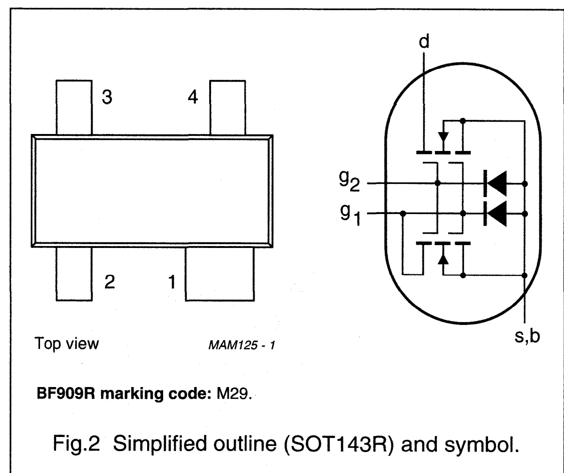
PINNING

PIN	SYMBOL	DESCRIPTION
1	s, b	source
2	d	drain
3	g_2	gate 2
4	g_1	gate 1



BF909 marking code: M28.

Fig.1 Simplified outline (SOT143) and symbol.



BF909R marking code: M29.

Fig.2 Simplified outline (SOT143R) and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DS}	drain-source voltage		–	–	7	V
I_D	drain current		–	–	40	mA
P_{tot}	total power dissipation		–	–	200	mW
T_j	operating junction temperature		–	–	150	°C
$\|y_{fs}\|$	forward transfer admittance		36	43	50	mS
C_{ig1-s}	input capacitance at gate 1		–	3.6	4.3	pF
C_{rs}	reverse transfer capacitance	f = 1 MHz	–	35	50	fF
F	noise figure	f = 800 MHz	–	2	2.8	dB

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	7	V
I_D	drain current		–	40	mA
I_{G1}	gate 1 current		–	±10	mA
I_{G2}	gate 2 current		–	±10	mA
P_{tot}	total power dissipation	see Fig.3			
	BF909	up to T_{amb} = 50 °C; note 1	–	200	mW
	BF909R	up to T_{amb} = 40 °C; note 1	–	200	mW
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–	150	°C

Note

1. Device mounted on a printed-circuit board.

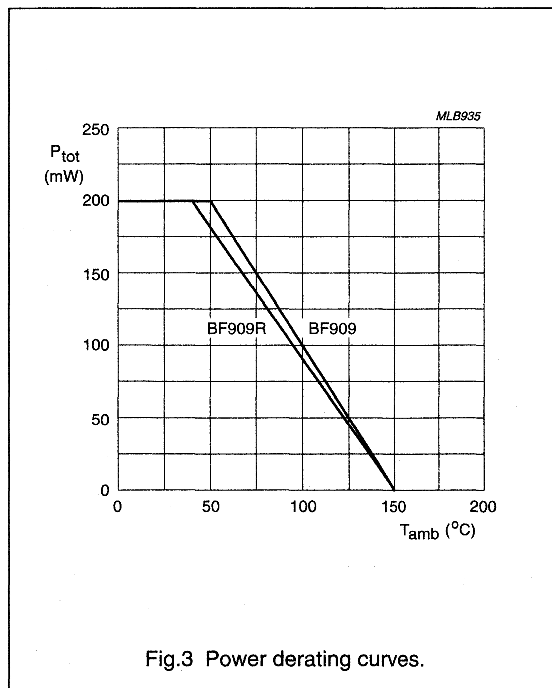


Fig.3 Power derating curves.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	note 1		
	BF909		500	K/W
	BF909R		550	K/W
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	note 2		
	BF909	T_s = 92 °C	290	K/W
	BF909R	T_s = 78 °C	360	K/W

Notes

1. Device mounted on a printed-circuit board.
2. T_s is the temperature at the soldering point of the source lead.

STATIC CHARACTERISTICS

T_j = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{(BR)G1\text{-}SS}$	gate 1-source breakdown voltage	$V_{G2\text{-}S} = V_{DS} = 0$; $I_{G1\text{-}S}$ = 10 mA	6	15	V
$V_{(BR)G2\text{-}SS}$	gate 2-source breakdown voltage	$V_{G1\text{-}S} = V_{DS} = 0$; $I_{G2\text{-}S}$ = 10 mA	6	15	V
$V_{(F)S\text{-}G1}$	forward source-gate 1 voltage	$V_{G2\text{-}S} = V_{DS} = 0$; $I_{S\text{-}G1}$ = 10 mA	0.5	1.5	V
$V_{(F)S\text{-}G2}$	forward source-gate 2 voltage	$V_{G1\text{-}S} = V_{DS} = 0$; $I_{S\text{-}G2}$ = 10 mA	0.5	1.5	V
$V_{G1\text{-}S(th)}$	gate 1-source threshold voltage	$V_{G2\text{-}S}$ = 4 V; V_{DS} = 5 V; I_D = 20 µA	0.3	1	V
$V_{G2\text{-}S(th)}$	gate 2-source threshold voltage	$V_{G1\text{-}S} = V_{DS}$ = 5 V; I_D = 20 µA	0.3	1.2	V
I_{DSX}	drain-source current	$V_{G2\text{-}S}$ = 4 V; V_{DS} = 5 V; R_{G1} = 120 kΩ; note 1	12	20	mA
$I_{G1\text{-}SS}$	gate 1 cut-off current	$V_{G1\text{-}S}$ = 5 V; $V_{G2\text{-}S} = V_{DS} = 0$	–	50	nA
$I_{G2\text{-}SS}$	gate 2 cut-off current	$V_{G2\text{-}S}$ = 5 V; $V_{G1\text{-}S} = V_{DS} = 0$	–	50	nA

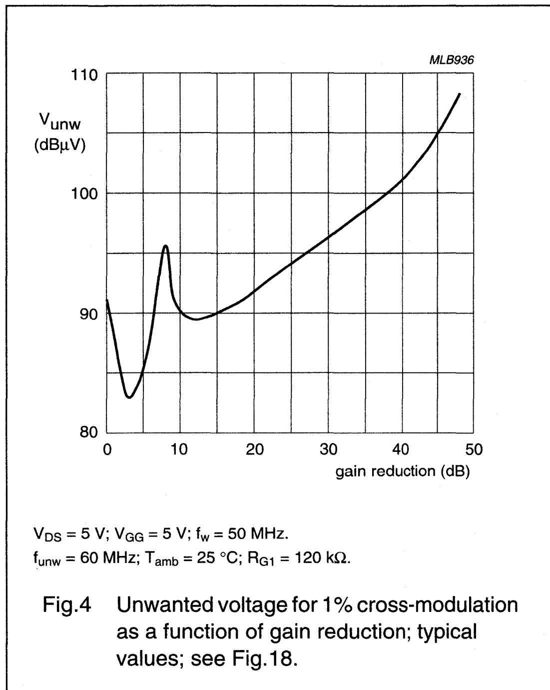
Note

1. R_{G1} connects gate 1 to V_{GG} = 5 V; see Fig.18.

DYNAMIC CHARACTERISTICS

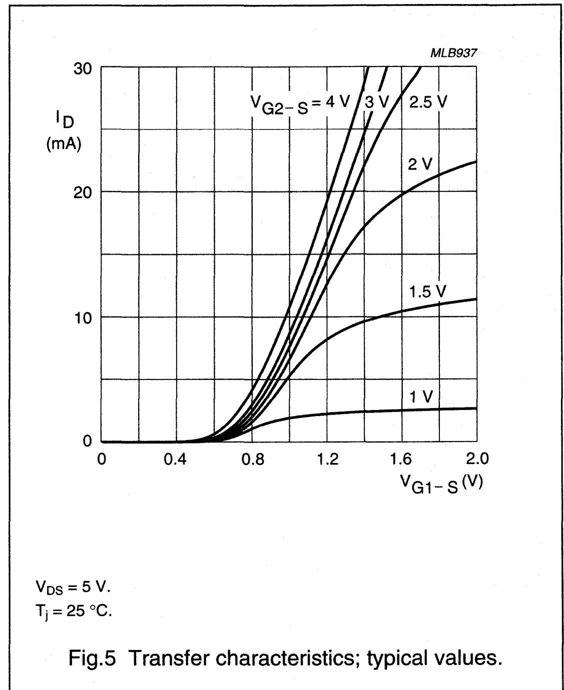
Common source; T_{amb} = 25 °C; V_{DS} = 5 V; $V_{G2\text{-}S}$ = 4 V; I_D = 15 mA; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\|y_{fs}\|$	forward transfer admittance	pulsed; T_j = 25 °C	36	43	50	mS
$C_{ig1\text{-}s}$	input capacitance at gate 1	f = 1 MHz	–	3.6	4.3	pF
$C_{ig2\text{-}s}$	input capacitance at gate 2	f = 1 MHz	–	2.3	3	pF
C_{os}	drain-source capacitance	f = 1 MHz	–	2.3	3	pF
C_{rs}	reverse transfer capacitance	f = 1 MHz	–	35	50	fF
F	noise figure	f = 800 MHz; $G_S = G_{Sopt}$; $B_S = B_{Sopt}$	–	2	2.8	dB



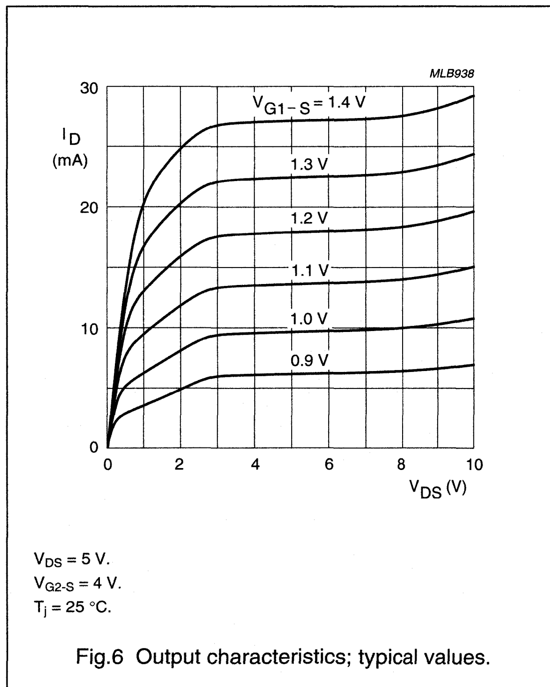
V_{DS} = 5 V; V_{GG} = 5 V; f_w = 50 MHz.
f_{unw} = 60 MHz; T_{amb} = 25 °C; R_{G1} = 120 kΩ.

Fig.4 Unwanted voltage for 1% cross-modulation as a function of gain reduction; typical values; see Fig.18.



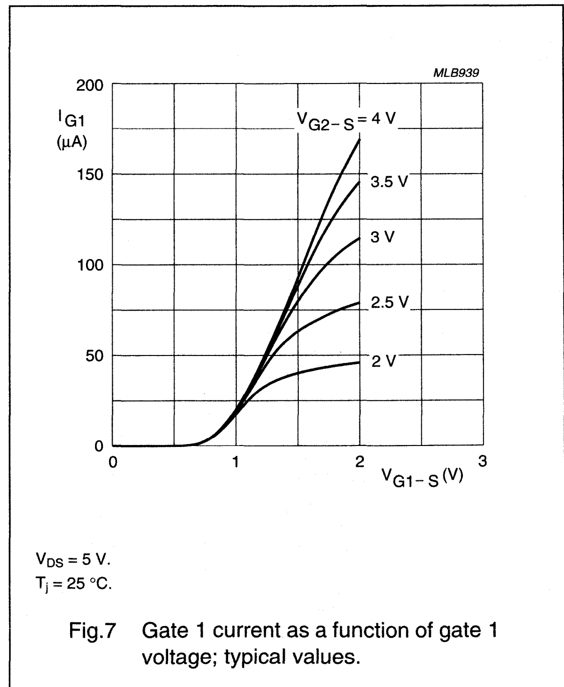
V_{DS} = 5 V.
T_j = 25 °C.

Fig.5 Transfer characteristics; typical values.



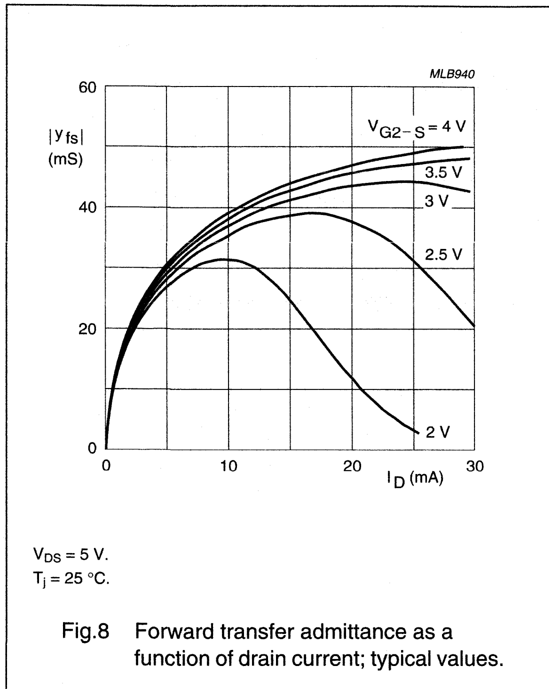
V_{DS} = 5 V.
V_{G2-S} = 4 V.
T_j = 25 °C.

Fig.6 Output characteristics; typical values.



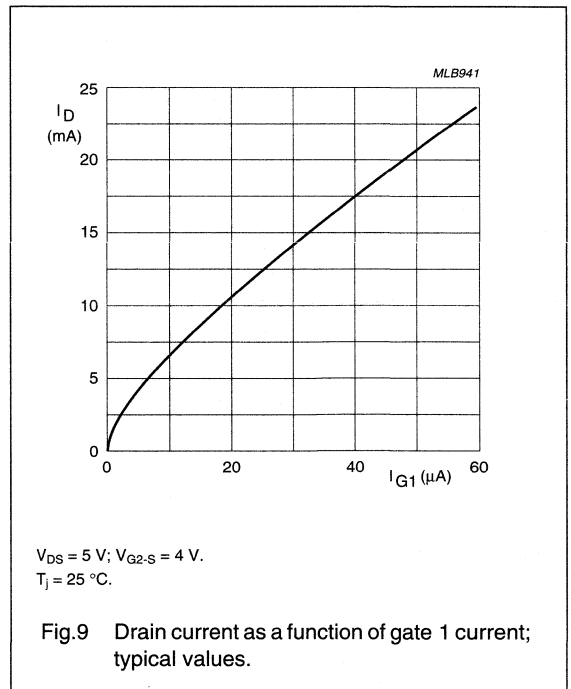
V_{DS} = 5 V.
T_j = 25 °C.

Fig.7 Gate 1 current as a function of gate 1 voltage; typical values.



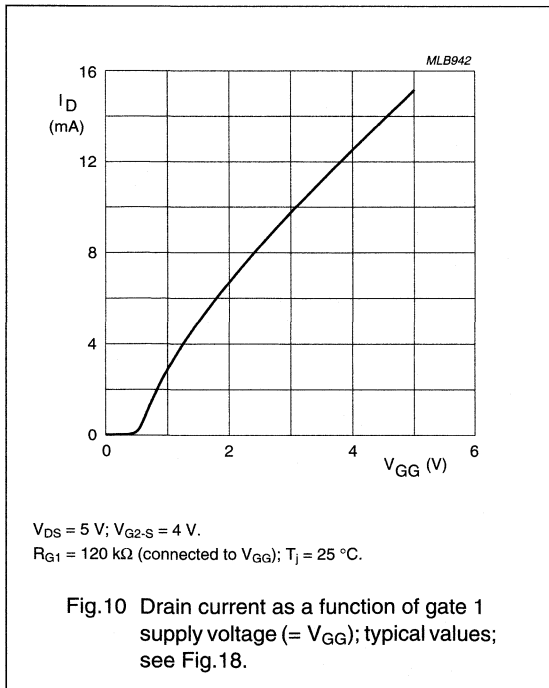
V_{DS} = 5 V.
T_j = 25 °C.

Fig.8 Forward transfer admittance as a function of drain current; typical values.



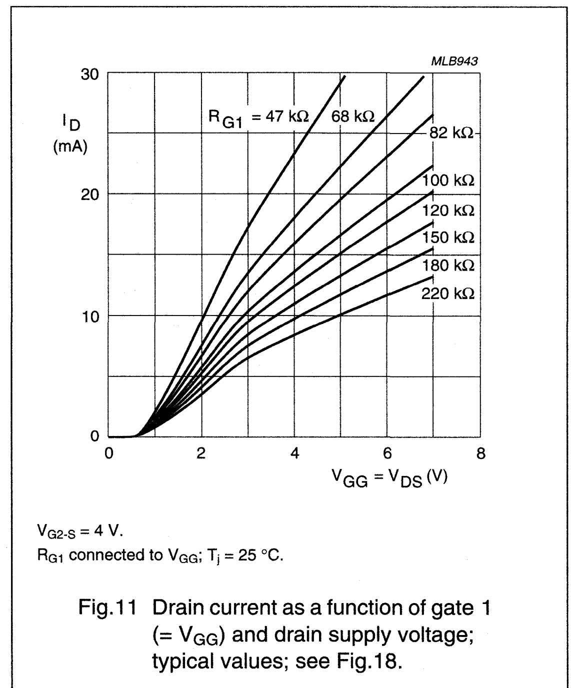
V_{DS} = 5 V; V_{G2-S} = 4 V.
T_j = 25 °C.

Fig.9 Drain current as a function of gate 1 current; typical values.



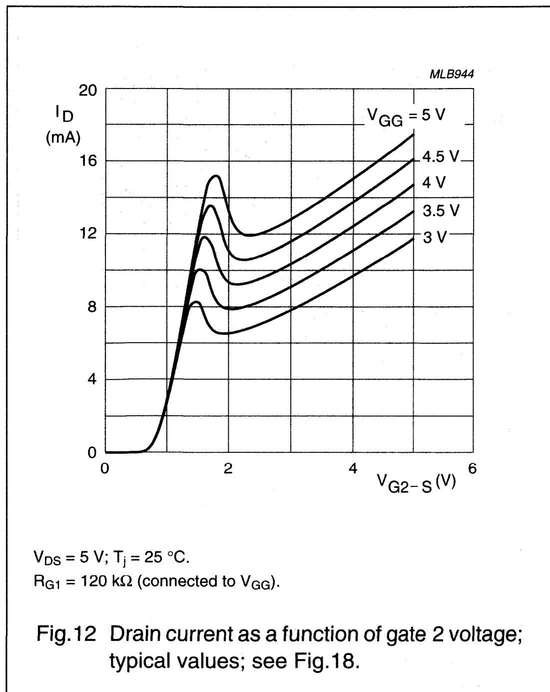
V_{DS} = 5 V; V_{G2-S} = 4 V.
R_{G1} = 120 kΩ (connected to V_{GG}); T_j = 25 °C.

Fig.10 Drain current as a function of gate 1 supply voltage (= V_{GG}); typical values; see Fig.18.



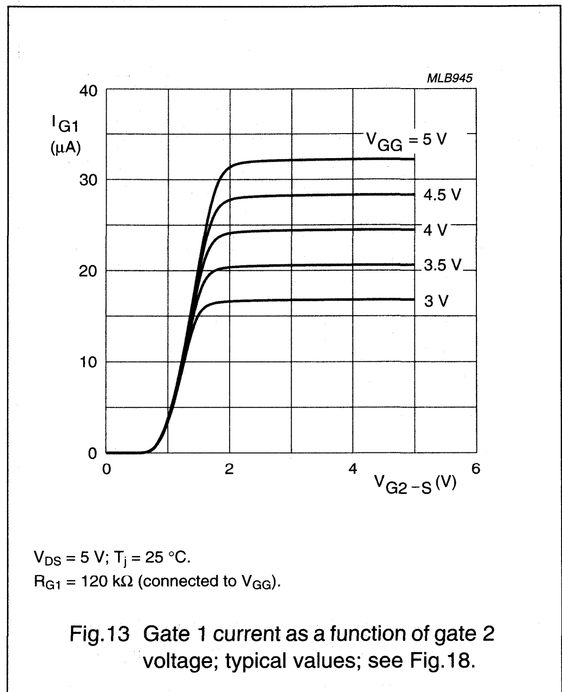
V_{G2-S} = 4 V.
R_{G1} connected to V_{GG}; T_j = 25 °C.

Fig.11 Drain current as a function of gate 1 (= V_{GG}) and drain supply voltage; typical values; see Fig.18.



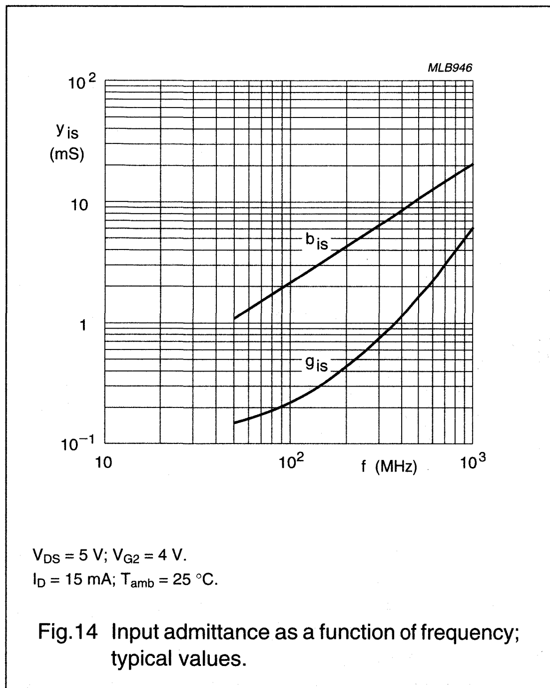
V_{DS} = 5 V; T_j = 25 °C.
R_{G1} = 120 kΩ (connected to V_{GG}).

Fig.12 Drain current as a function of gate 2 voltage; typical values; see Fig.18.



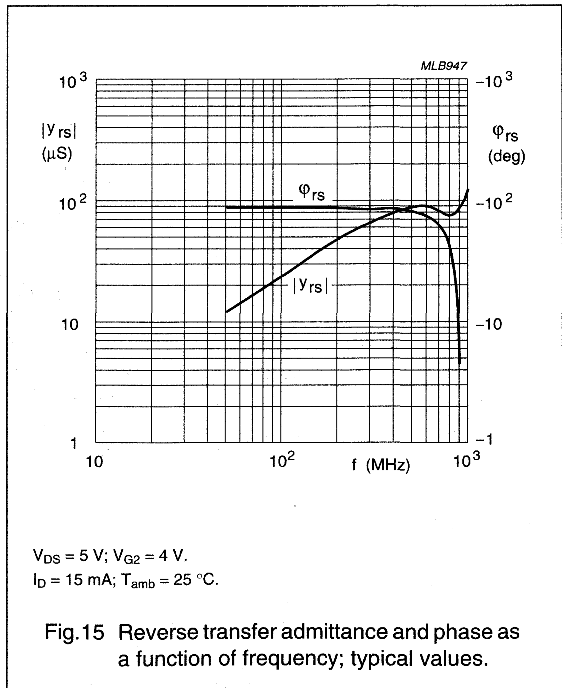
V_{DS} = 5 V; T_j = 25 °C.
R_{G1} = 120 kΩ (connected to V_{GG}).

Fig.13 Gate 1 current as a function of gate 2 voltage; typical values; see Fig.18.



V_{DS} = 5 V; V_{G2} = 4 V.
I_D = 15 mA; T_{amb} = 25 °C.

Fig.14 Input admittance as a function of frequency; typical values.



V_{DS} = 5 V; V_{G2} = 4 V.
I_D = 15 mA; T_{amb} = 25 °C.

Fig.15 Reverse transfer admittance and phase as a function of frequency; typical values.

N-channel dual gate MOS-FETs BF909; BF909R

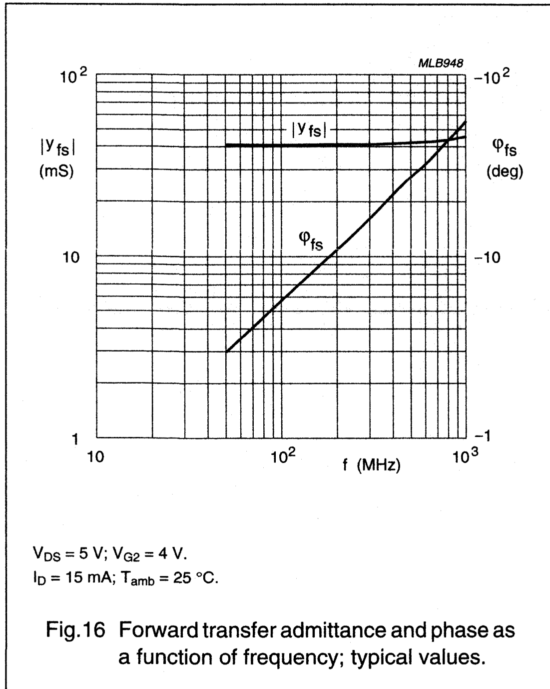


Fig.16 Forward transfer admittance and phase as a function of frequency; typical values.

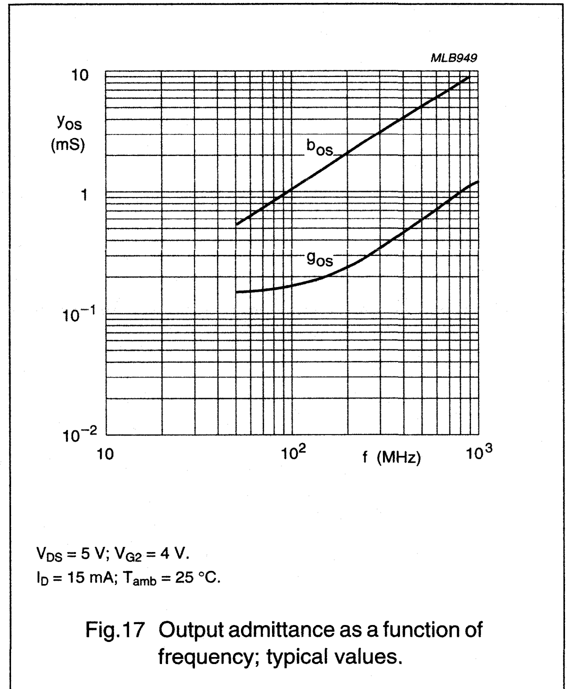


Fig.17 Output admittance as a function of frequency; typical values.

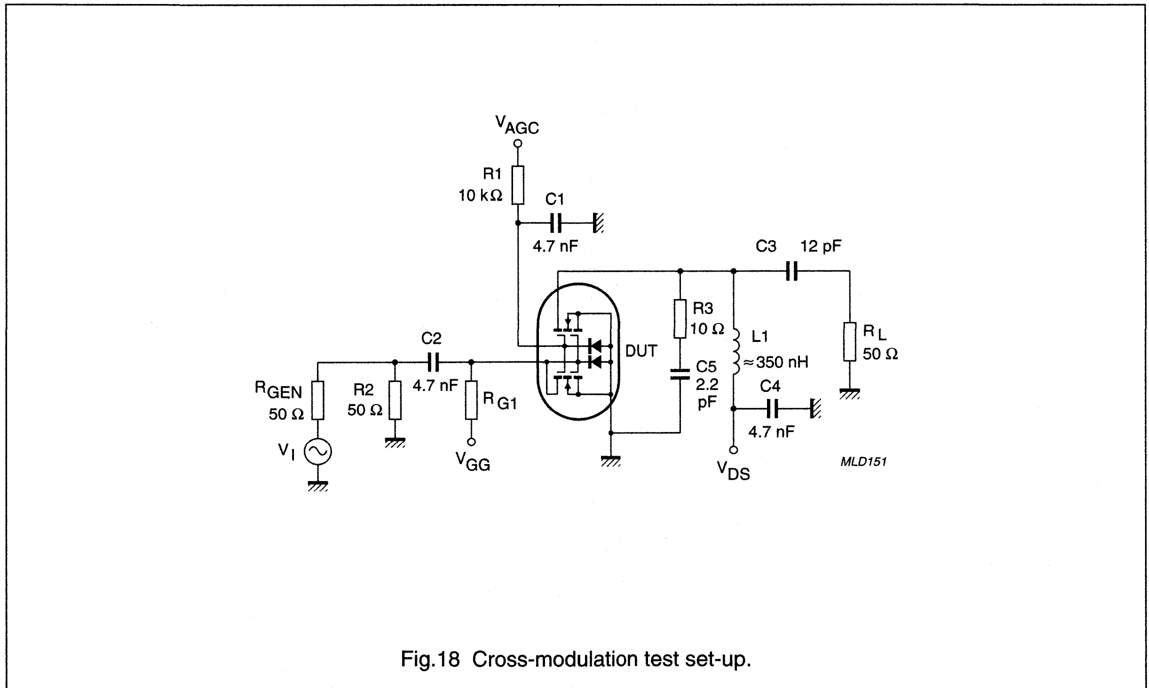


Fig.18 Cross-modulation test set-up.

Table 1 Scattering parameters: T_{amb} = 25 °C; V_{DS} = 5 V; V_{G2-S} = 4 V; I_D = 15 mA

f (MHz)	s_{11}		s_{21}		s_{12}		s_{22}	
	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)
50	0.985	−6.4	4.064	172.3	0.001	86.9	0.985	−3.2
100	0.978	−12.6	3.997	164.9	0.002	82.7	0.982	−6.4
200	0.957	−25.0	3.886	150.8	0.005	74.3	0.973	−12.6
300	0.931	−36.5	3.682	137.3	0.006	68.9	0.960	−18.6
400	0.899	−47.6	3.484	123.8	0.007	59.6	0.947	−24.2
500	0.868	−57.4	3.260	111.7	0.007	57.9	0.936	−29.6
600	0.848	−66.6	3.053	101.0	0.006	58.5	0.927	−34.8
700	0.816	−74.6	2.829	90.3	0.005	65.5	0.919	−39.8
800	0.792	−82.2	2.652	79.9	0.005	83.3	0.913	−44.6
900	0.772	−89.3	2.470	69.5	0.005	114.9	0.910	−49.5
1000	0.754	−95.6	2.328	59.5	0.006	138.7	0.909	−54.6

Table 2 Noise data: T_{amb} = 25 °C; V_{DS} = 5 V; V_{G2-S} = 4 V; I_D = 15 mA

f (MHz)	F_{min} (dB)	Γ_{opt}		r_n
		(ratio)	(deg)	
800	2.00	0.603	67.71	0.581

N-channel dual-gate MOS-FET BF909WR

FEATURES

- Specially designed for use at 5 V supply voltage
- Short channel transistor with high forward transfer admittance to input capacitance ratio
- Low noise gain controlled amplifier up to 1 GHz
- Superior cross-modulation performance during AGC.

APPLICATIONS

- VHF and UHF applications with 3 to 7 V supply voltage such as television tuners and professional communications equipment.

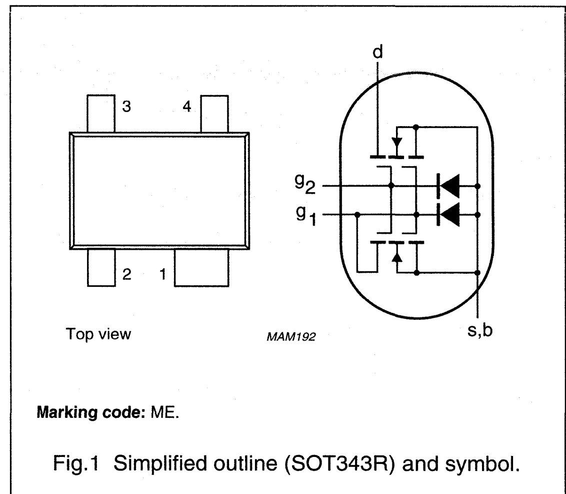
DESCRIPTION

Enhancement type field-effect transistor in a plastic microminiature SOT343R package. The transistor consists of an amplifier MOS-FET with source and substrate interconnected and an internal bias circuit to ensure good cross-modulation performance during AGC.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING

PIN	SYMBOL	DESCRIPTION
1	s, b	source
2	d	drain
3	g_2	gate 2
4	g_1	gate 1



Marking code: ME.

Fig.1 Simplified outline (SOT343R) and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DS}	drain-source voltage		–	–	7	V
I_D	drain current		–	–	40	mA
P_{tot}	total power dissipation		–	–	280	mW
T_j	operating junction temperature		–	–	150	°C
$\|y_{fs}\|$	forward transfer admittance		36	43	50	mS
C_{ig1-s}	input capacitance at gate 1		–	3.6	4.3	pF
C_{rs}	reverse transfer capacitance	f = 1 MHz	–	30	50	fF
F	noise figure	f = 800 MHz	–	2	2.8	dB

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	7	V
I_D	drain current		–	40	mA
I_{G1}	gate 1 current		–	±10	mA
I_{G2}	gate 2 current		–	±10	mA
P_{tot}	total power dissipation	up to T_{amb} = 50 °C; see Fig.2; note 1	–	280	mW
T_{stg}	storage temperature range		–65	+150	°C
T_j	operating junction temperature		–	+150	°C

Note

1. Device mounted on a printed-circuit board.

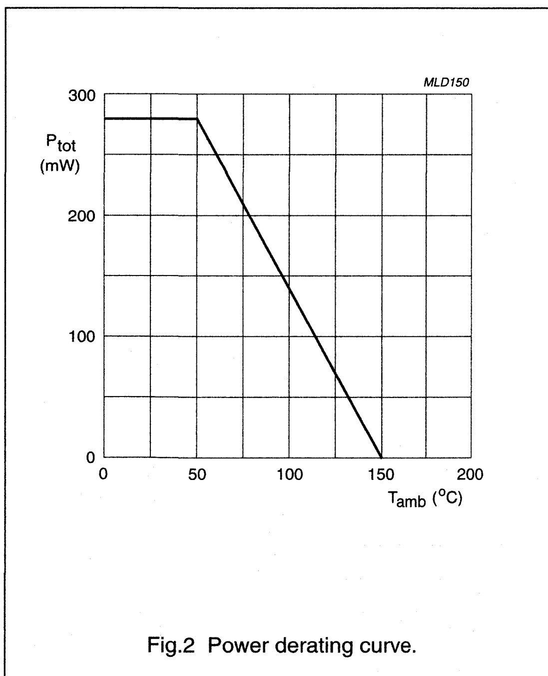


Fig.2 Power derating curve.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	note 1	350	K/W
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	T_s = 91 °C; note 2	210	K/W

Notes

1. Device mounted on a printed-circuit board.
2. T_s is the temperature at the soldering point of the source lead.

STATIC CHARACTERISTICS

T_j = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{(BR)G1\text{-}SS}$	gate 1-source breakdown voltage	$V_{G2\text{-}S} = V_{DS} = 0$; $I_{G1\text{-}S}$ = 10 mA	6	15	V
$V_{(BR)G2\text{-}SS}$	gate 2-source breakdown voltage	$V_{G1\text{-}S} = V_{DS} = 0$; $I_{G2\text{-}S}$ = 10 mA	6	15	V
$V_{(F)S\text{-}G1}$	forward source-gate 1 voltage	$V_{G2\text{-}S} = V_{DS} = 0$; $I_{S\text{-}G1}$ = 10 mA	0.5	1.5	V
$V_{(F)S\text{-}G2}$	forward source-gate 2 voltage	$V_{G1\text{-}S} = V_{DS} = 0$; $I_{S\text{-}G2}$ = 10 mA	0.5	1.5	V
$V_{G1\text{-}S(th)}$	gate 1-source threshold voltage	$V_{G2\text{-}S}$ = 4 V; V_{DS} = 5 V; I_D = 20 μA	0.3	1	V
$V_{G2\text{-}S(th)}$	gate 2-source threshold voltage	$V_{G1\text{-}S} = V_{DS}$ = 5 V; I_D = 20 μA	0.3	1.2	V
I_{DSX}	drain-source current	$V_{G2\text{-}S}$ = 4 V; V_{DS} = 5 V; R_{G1} = 120 kΩ; note 1	12	20	mA
$I_{G1\text{-}SS}$	gate 1 cut-off current	$V_{G2\text{-}S} = V_{DS} = 0$; $V_{G1\text{-}S}$ = 5 V	–	50	nA
$I_{G2\text{-}SS}$	gate 2 cut-off current	$V_{G1\text{-}S} = V_{DS} = 0$; $V_{G2\text{-}S}$ = 5 V	–	50	nA

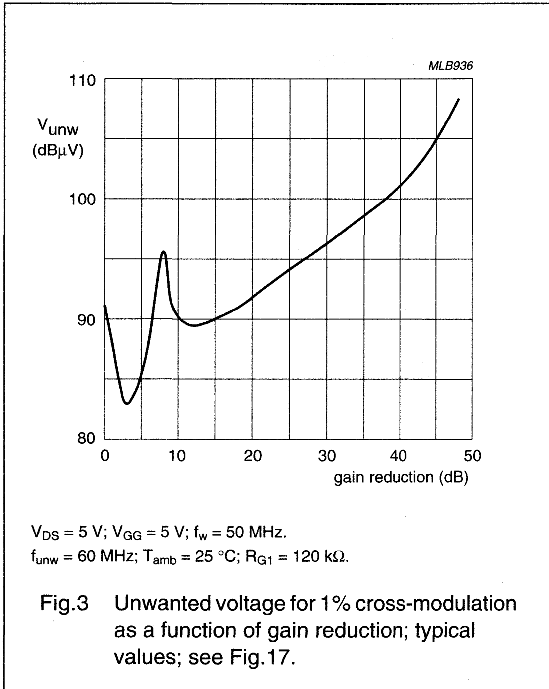
Note

1. R_{G1} connects gate 1 to V_{GG} = 5 V.

DYNAMIC CHARACTERISTICS

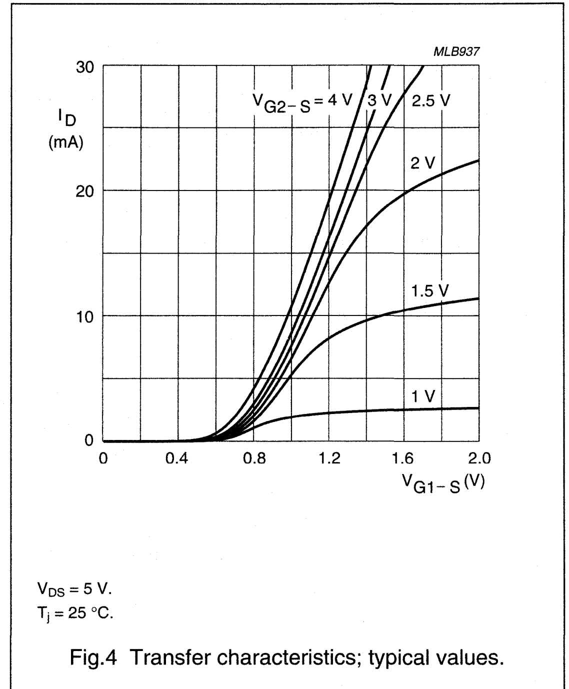
Common source; T_{amb} = 25 °C; V_{DS} = 5 V; $V_{G2\text{-}S}$ = 4 V; I_D = 15 mA; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\lvert y_{fs} \rvert$	forward transfer admittance	pulsed; T_j = 25 °C	36	43	50	mS
$C_{ig1\text{-}s}$	input capacitance at gate 1	f = 1 MHz	–	3.6	4.3	pF
$C_{ig2\text{-}s}$	input capacitance at gate 2	f = 1 MHz	–	2.3	3	pF
C_{os}	drain-source capacitance	f = 1 MHz	–	2.3	3	pF
C_{rs}	reverse transfer capacitance	f = 1 MHz	–	30	50	fF
F	noise figure	f = 800 MHz; $G_S = G_{Sopt}$; $B_S = B_{Sopt}$	–	2	2.8	dB



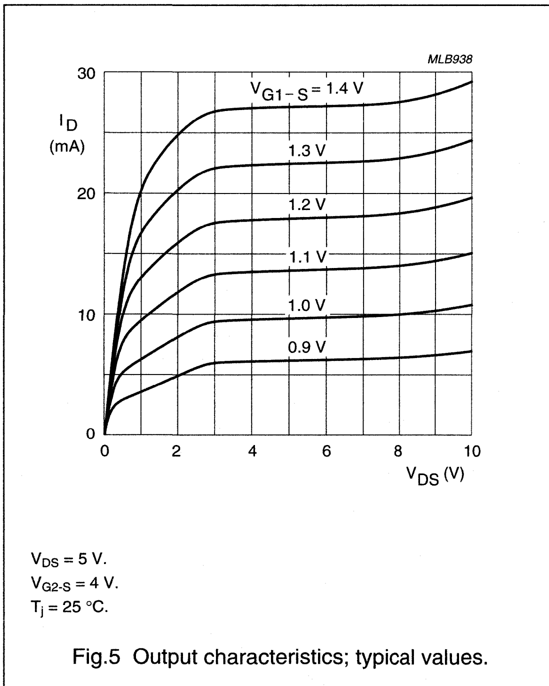
V_{DS} = 5 V; V_{GG} = 5 V; f_w = 50 MHz.
f_{unw} = 60 MHz; T_{amb} = 25 °C; R_{G1} = 120 kΩ.

Fig.3 Unwanted voltage for 1% cross-modulation as a function of gain reduction; typical values; see Fig.17.



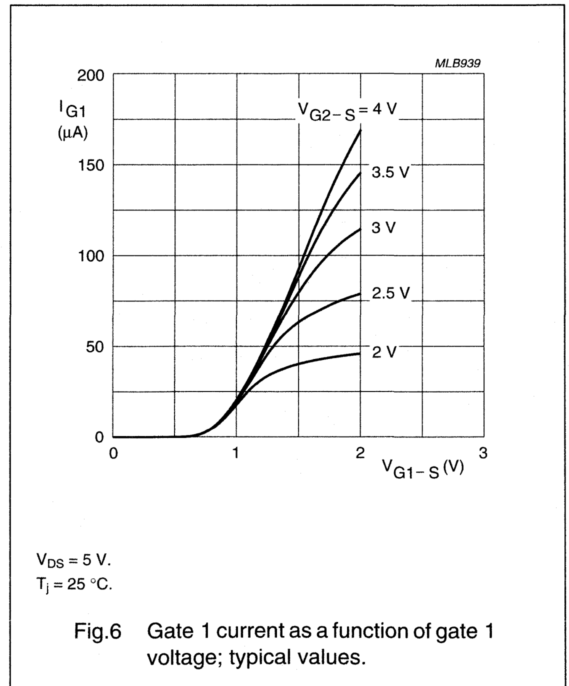
V_{DS} = 5 V.
T_j = 25 °C.

Fig.4 Transfer characteristics; typical values.



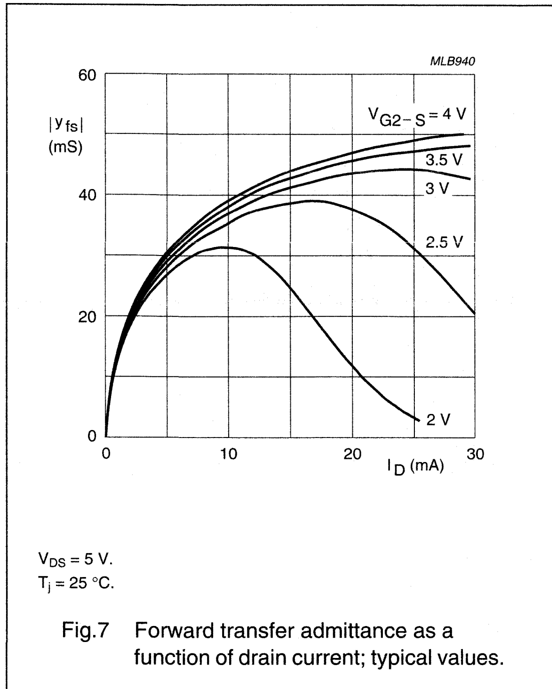
V_{DS} = 5 V.
V_{G2-S} = 4 V.
T_j = 25 °C.

Fig.5 Output characteristics; typical values.



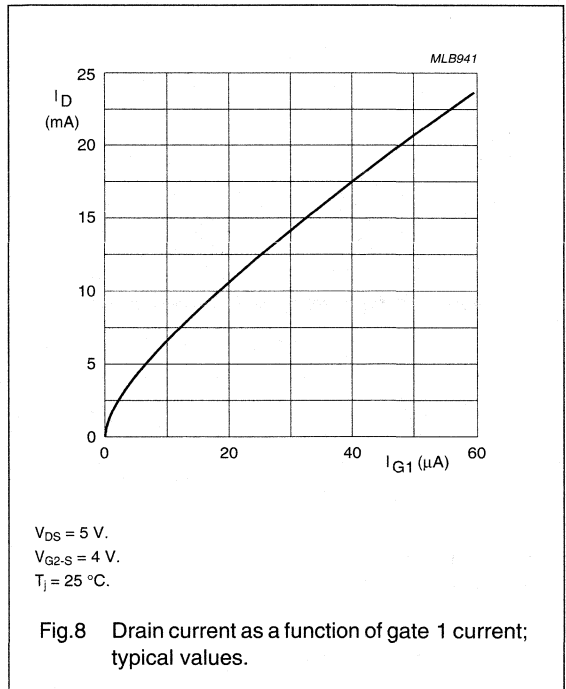
V_{DS} = 5 V.
T_j = 25 °C.

Fig.6 Gate 1 current as a function of gate 1 voltage; typical values.



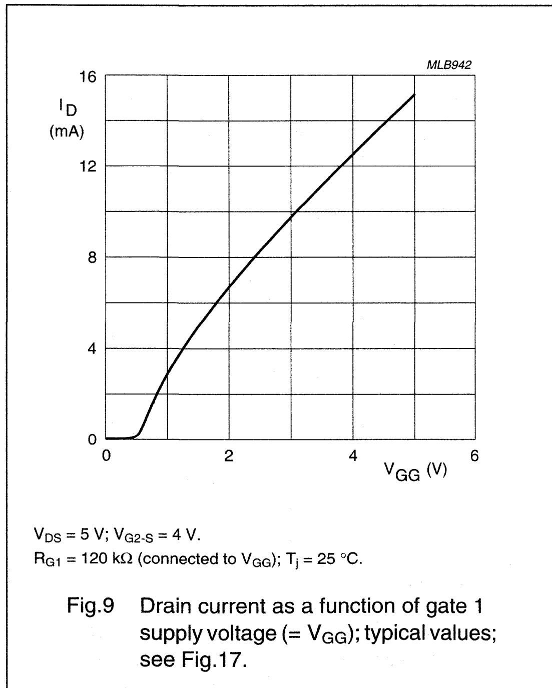
V_{DS} = 5 V.
T_j = 25 °C.

Fig.7 Forward transfer admittance as a function of drain current; typical values.



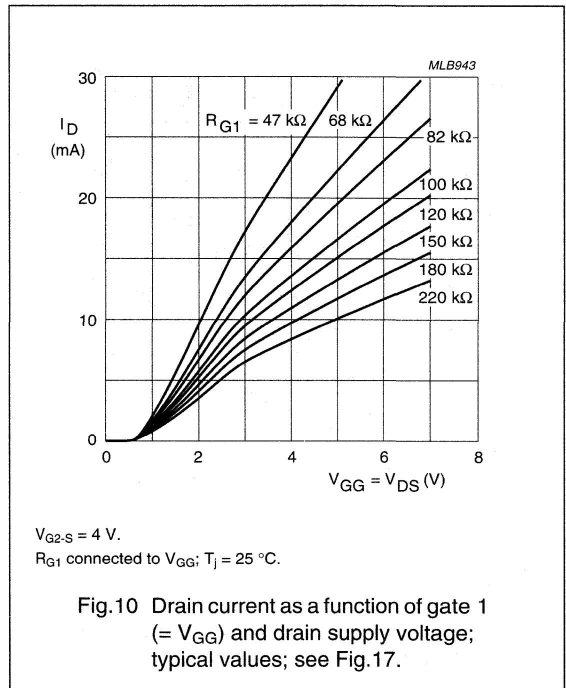
V_{DS} = 5 V.
$V_{G2\text{-}S}$ = 4 V.
T_j = 25 °C.

Fig.8 Drain current as a function of gate 1 current; typical values.



V_{DS} = 5 V; $V_{G2\text{-}S}$ = 4 V.
R_{G1} = 120 kΩ (connected to V_{GG}); T_j = 25 °C.

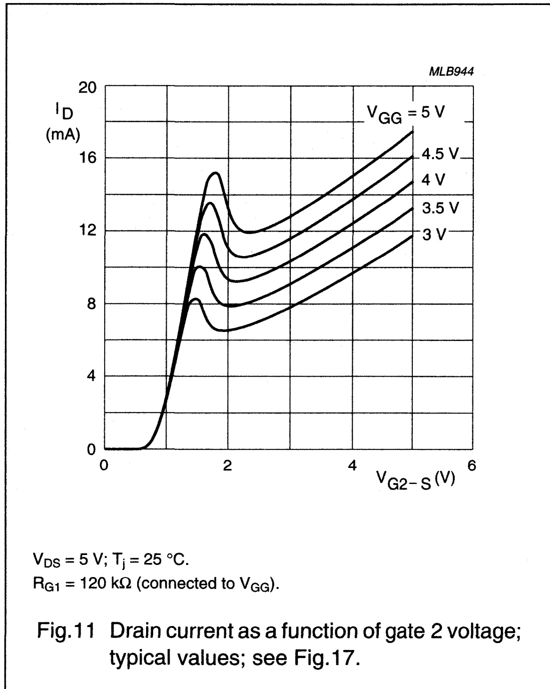
Fig.9 Drain current as a function of gate 1 supply voltage (= V_{GG}); typical values; see Fig.17.



$V_{G2\text{-}S}$ = 4 V.
R_{G1} connected to V_{GG}; T_j = 25 °C.

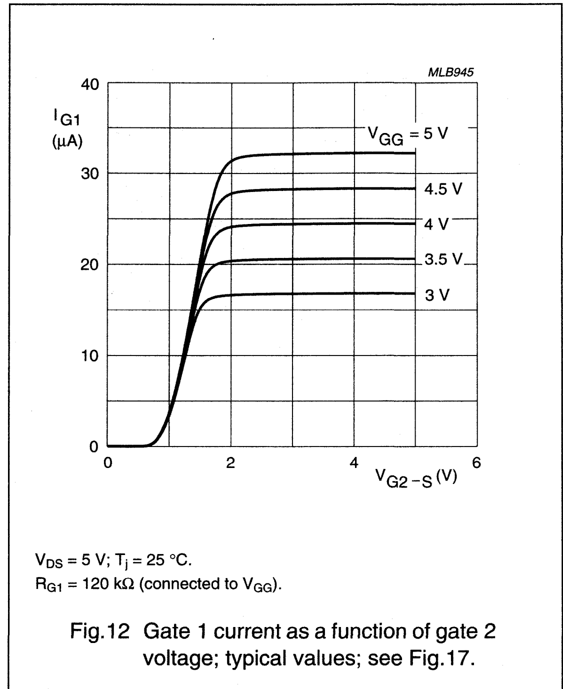
Fig.10 Drain current as a function of gate 1 (= V_{GG}) and drain supply voltage; typical values; see Fig.17.

N-channel dual-gate MOS-FET BF909WR



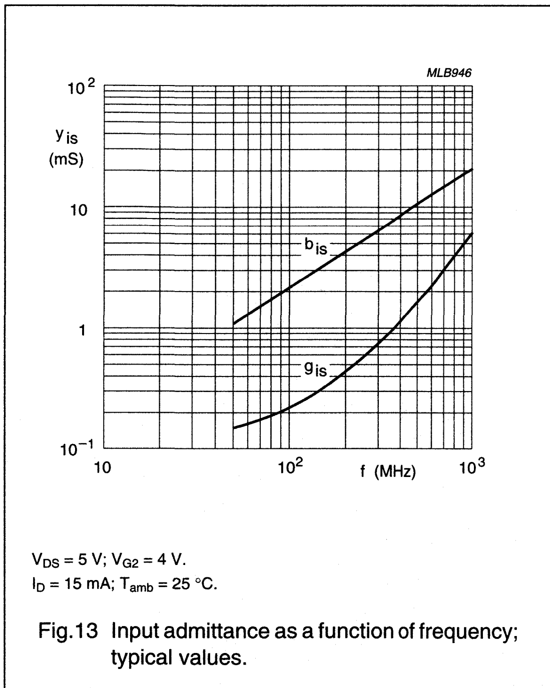
V_{DS} = 5 V; T_j = 25 °C.
R_{G1} = 120 kΩ (connected to V_{GG}).

Fig.11 Drain current as a function of gate 2 voltage; typical values; see Fig.17.



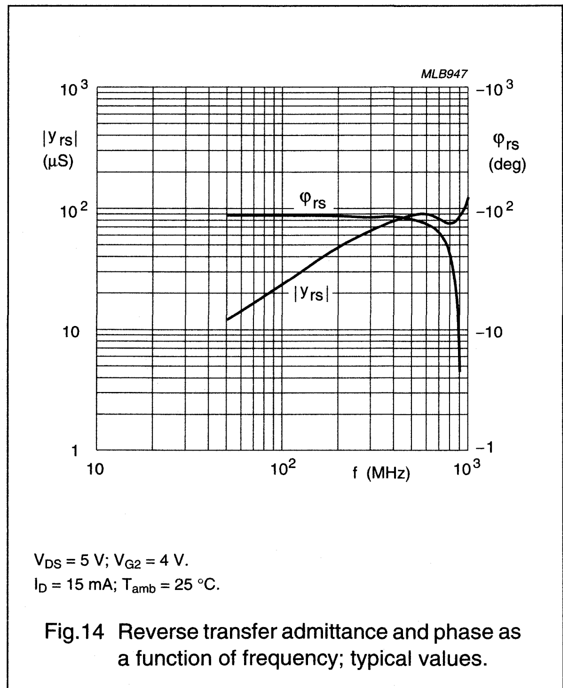
V_{DS} = 5 V; T_j = 25 °C.
R_{G1} = 120 kΩ (connected to V_{GG}).

Fig.12 Gate 1 current as a function of gate 2 voltage; typical values; see Fig.17.



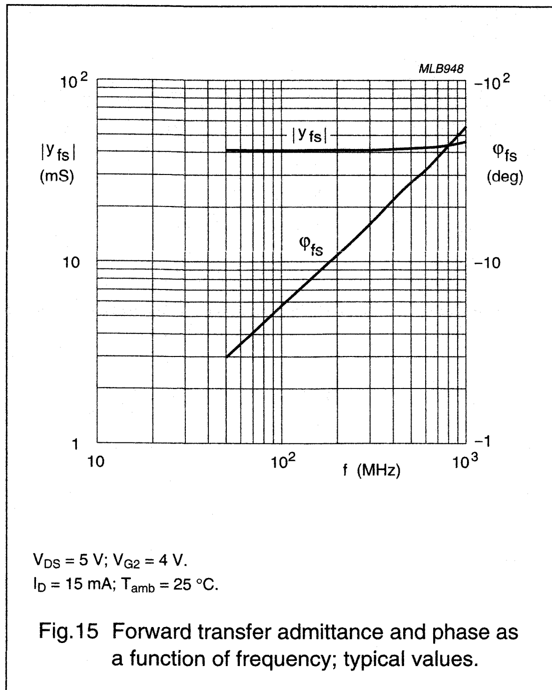
V_{DS} = 5 V; V_{G2} = 4 V.
I_D = 15 mA; T_{amb} = 25 °C.

Fig.13 Input admittance as a function of frequency; typical values.



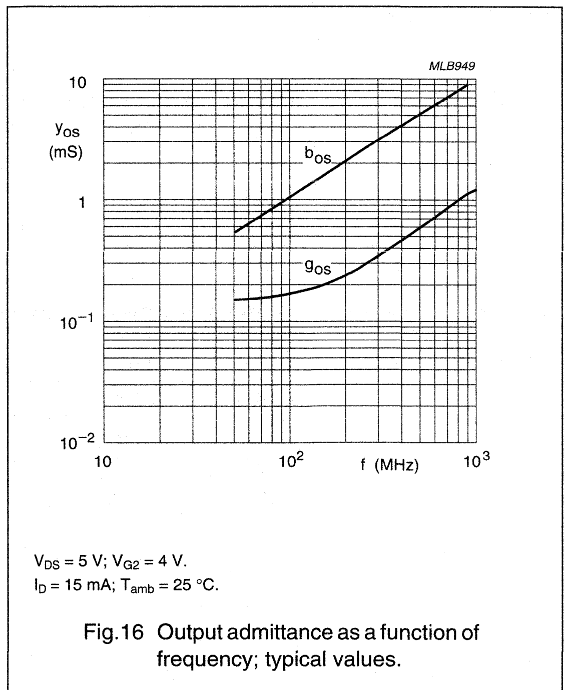
V_{DS} = 5 V; V_{G2} = 4 V.
I_D = 15 mA; T_{amb} = 25 °C.

Fig.14 Reverse transfer admittance and phase as a function of frequency; typical values.



V_{DS} = 5 V; V_{G2} = 4 V.
I_D = 15 mA; T_{amb} = 25 °C.

Fig.15 Forward transfer admittance and phase as a function of frequency; typical values.



V_{DS} = 5 V; V_{G2} = 4 V.
I_D = 15 mA; T_{amb} = 25 °C.

Fig.16 Output admittance as a function of frequency; typical values.

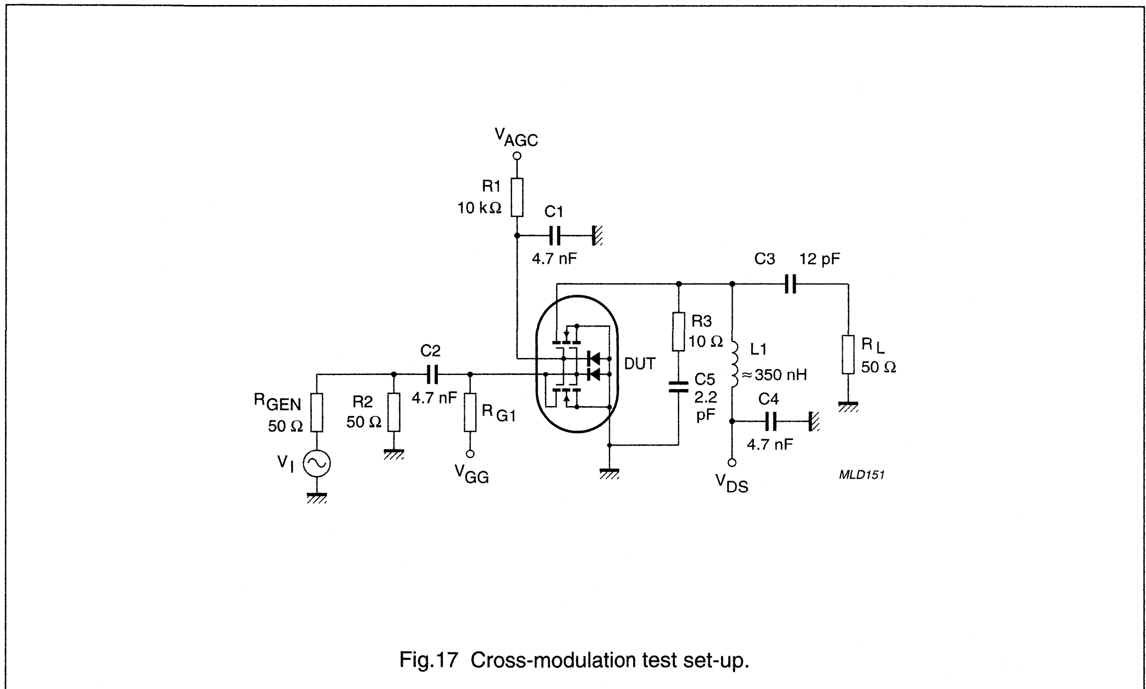


Fig.17 Cross-modulation test set-up.

Table 1 Scattering parameters: V_{DS} = 5 V; $V_{G2\text{-}S}$ = 4 V; I_D = 15 mA; T_{amb} = 25 °C

f (MHz)	s_{11}		s_{21}		s_{12}		s_{22}	
	MAGNITUDE (ratio)	**ANGLE (deg)**	**MAGNITUDE (ratio)**	**ANGLE (deg)**	**MAGNITUDE (ratio)**	**ANGLE (deg)**	**MAGNITUDE (ratio)**	**ANGLE (deg)**
50	0.985	−6.4	4.064	172.3	0.001	86.9	0.985	−3.2
100	0.978	−12.6	3.997	164.9	0.002	82.7	0.982	−6.4
200	0.957	−25.0	3.886	150.8	0.005	74.3	0.973	−12.6
300	0.931	−36.5	3.682	137.3	0.006	68.9	0.960	−18.6
400	0.899	−47.6	3.484	123.8	0.007	59.6	0.947	−24.2
500	0.868	−57.4	3.260	111.7	0.007	57.9	0.936	−29.6
600	0.848	−66.6	3.053	101.0	0.006	58.5	0.927	−34.8
700	0.816	−74.6	2.829	90.3	0.005	65.5	0.919	−39.8
800	0.792	−82.2	2.652	79.9	0.005	83.3	0.913	−44.6
900	0.772	−89.3	2.470	69.5	0.005	114.9	0.910	−49.5
1000	0.754	−95.6	2.328	59.5	0.006	138.7	0.909	−54.6

Table 2 Noise data: V_{DS} = 5 V; $V_{G2\text{-}S}$ = 4 V; I_D = 15 mA; T_{amb} = 25 °C

f (MHz)	F_{min} (dB)	Γ_{opt}		r_n
		(ratio)	**(deg)**	
800	2.00	0.603	67.71	0.581

N-channel dual-gate MOS-FET BF989

FEATURES

- Protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

APPLICATIONS

- UHF applications such as:
  - UHF television tuners
  - Professional communication equipment.

PINNING

PIN	SYMBOL	DESCRIPTION
1	s, b	source
2	d	drain
3	g_2	gate 2
4	g_1	gate 1

DESCRIPTION

Depletion type field-effect transistor in a plastic SOT143 microminiature package with interconnected source and substrate.

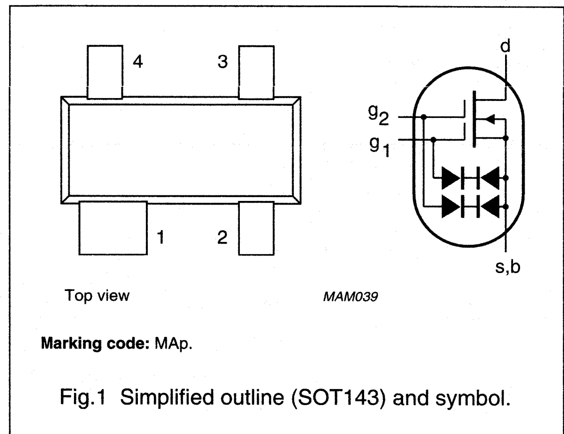


Fig.1 Simplified outline (SOT143) and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
V_{DS}	drain-source voltage		–	20	V
I_D	drain current		–	20	mA
P_{tot}	total power dissipation	up to T_{amb} = 60 °C	–	200	mW
T_j	junction temperature		–	150	°C
$\|Y_{fs}\|$	transfer admittance	f = 1 kHz; I_D = 7 mA; V_{DS} = 10 V; V_{G2-S} = 4 V	12	–	mS
C_{ig1-s}	input capacitance at gate 1	f = 1 MHz; I_D = 7 mA; V_{DS} = 10 V; V_{G2-S} = 4 V	1.8	–	pF
C_{rs}	feedback capacitance	f = 1 MHz; I_D = 7 mA; V_{DS} = 10 V; V_{G2-S} = 4 V	25	–	fF
F	noise figure	f = 800 MHz; G_S = 2 mS; B_S = B_{Sopt}; I_D = 7 mA; V_{DS} = 10 V; V_{G2-S} = 4 V	2.8	–	dB

LIMITING VALUES

In according with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	20	V
I_D	drain current (DC)		–	20	mA
$I_{D(AV)}$	average drain current		–	20	mA
I_{G1-S}	gate 1-source current		–	±10	mA
I_{G2-S}	gate 2-source current		–	±10	mA
P_{tot}	total power dissipation	up to T_{amb} = 60 °C; note 1	–	200	mW
T_{stg}	storage temperature range		–65	+150	°C
T_j	junction temperature		–	150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient	in free air; note 1	460	K/W

Note to the Limiting values and the Thermal characteristics

1. Device mounted on a ceramic substrate of 8 × 10 × 0.7 mm.

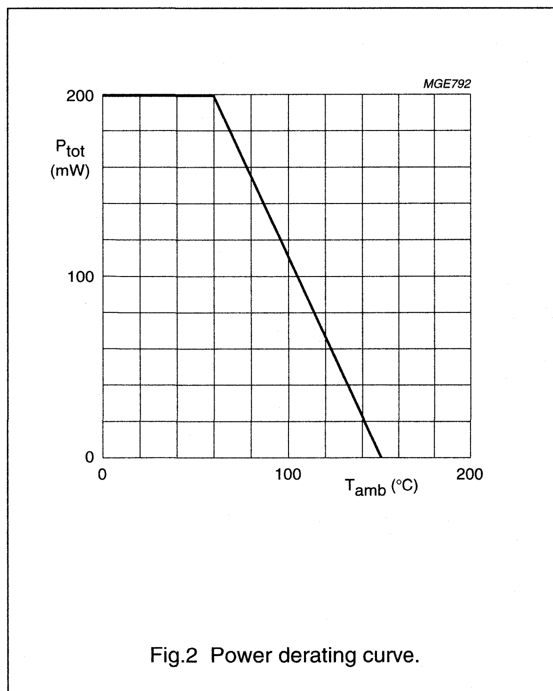


Fig.2 Power derating curve.

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{G1-SS}	gate 1 cut-off current	V_{G1-S} = ±5 V; V_{G2-S} = V_{DS} = 0	–	±50	nA
I_{G2-SS}	gate 2 cut-off current	V_{G2-S} = ±5 V; V_{G1-S} = V_{DS} = 0	–	±50	nA
I_{DSS}	drain-source cut-off voltage	V_{DS} = 10 V; V_{G1-S} = 0; V_{G2-S} = 4 V	2	20	mA
$V_{(BR)G1-SS}$	gate 1-source breakdown voltage	I_{G1-SS} = ±10 mA; V_{G2-S} = V_{DS} = 0	±6	±20	V
$V_{(BR)G2-SS}$	gate 2-source breakdown voltage	I_{G2-SS} = ±10 mA; V_{G1-S} = V_{DS} = 0	±6	±20	V
$V_{(P)G1-S}$	gate 1-source cut-off voltage	I_D = 20 μA; V_{DS} = 10 V; V_{G2-S} = 4 V	–	−2.7	V
$V_{(P)G2-S}$	gate 2-source cut-off voltage	I_D = 20 μA; V_{DS} = 10 V; V_{G1-S} = 0	–	−2.7	V

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): I_D = 7 mA; V_{DS} = 10 V; V_{G2-S} = 4 V; T_{amb} = 25 °C.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	UNIT
$\|Y_{fs}\|$	transfer admittance	f = 1 kHz	9.5	12	mS
C_{ig1-s}	input capacitance at gate 1	f = 1 MHz	–	1.8	pF
C_{ig2-s}	input capacitance at gate 2	f = 1 MHz	–	1	pF
C_{rs}	feedback capacitance	f = 1 MHz	–	25	fF
C_{os}	output capacitance	f = 1 MHz	–	0.9	pF
F	noise figure	f = 200 MHz; G_S = 2 mS; B_S = B_{Sopt}	–	1.6	dB
		f = 800 MHz; G_S = 2 mS; B_S = B_{Sopt}	–	2.8	dB

N-channel dual-gate MOS-FET — BF990A

FEATURES

- Protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

APPLICATIONS

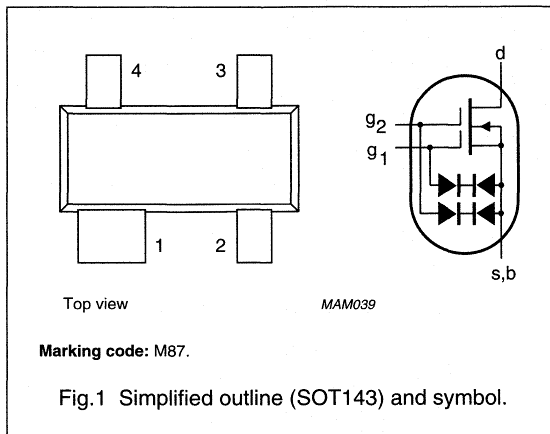
- RF applications such as:
  - Television tuners with 12 V supply voltage
  - Professional communication equipment.

PINNING

PIN	SYMBOL	DESCRIPTION
1	s, b	source
2	d	drain
3	g_2	gate 2
4	g_1	gate 1

DESCRIPTION

Depletion type field-effect transistor in a plastic SOT143 microminiature package with interconnected source and substrate.



Marking code: M87.

Fig.1 Simplified outline (SOT143) and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
V_{DS}	drain-source voltage		–	18	V
I_D	drain current		–	30	mA
P_{tot}	total power dissipation	up to T_{amb} = 60 °C	–	200	mW
T_j	junction temperature		–	150	°C
$\|Y_{fs}\|$	transfer admittance	f = 1 kHz; I_D = 10 mA; V_{DS} = 10 V; V_{G2-S} = 4 V	19	–	mS
C_{ig1-s}	input capacitance at gate 1	f = 1 MHz; I_D = 10 mA; V_{DS} = 10 V; V_{G2-S} = 4 V	2.6	3	pF
C_{rs}	feedback capacitance	f = 1 MHz; I_D = 10 mA; V_{DS} = 10 V; V_{G2-S} = 4 V	25	–	fF
F	noise figure	f = 800 MHz; G_S = 5 mS; B_S = B_{Sopt}; I_D = 10 mA; V_{DS} = 10 V; V_{G2-S} = 4 V	2	3	dB

LIMITING VALUES

In according with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	18	V
I_D	drain current (DC)		–	30	mA
$I_{G1\text{-}S}$	gate 1-source current		–	±10	mA
$I_{G2\text{-}S}$	gate 2-source current		–	±10	mA
P_{tot}	total power dissipation	up to T_{amb} = 60 °C; note 1	–	200	mW
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–	150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	in free air; note 1	460	K/W

Note to the Limiting values and the Thermal characteristics

1. Device mounted on a ceramic substrate of 8 × 10 × 0.7 mm.

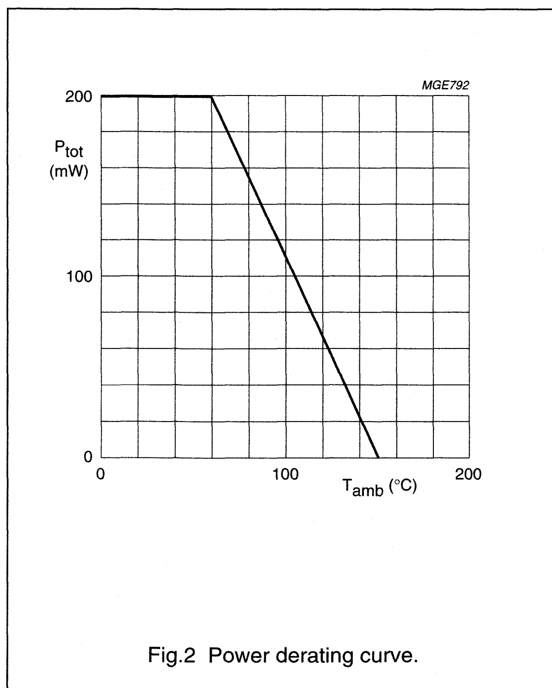


Fig.2 Power derating curve.

STATIC CHARACTERISTICS

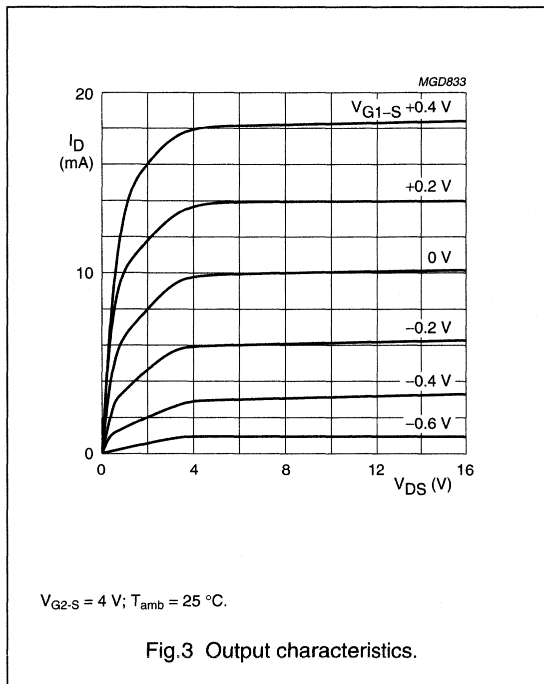
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{G1-SS}	gate 1 cut-off current	V_{G1-S} = ±7 V; V_{G2-S} = V_{DS} = 0	–	±25	nA
I_{G2-SS}	gate 2 cut-off current	V_{G2-S} = ±7 V; V_{G1-S} = V_{DS} = 0	–	±25	nA
$V_{(BR)G1-SS}$	gate 1-source breakdown voltage	I_{G1-SS} = ±10 mA; V_{G2-S} = V_{DS} = 0	±8	±20	V
$V_{(BR)G2-SS}$	gate 2-source breakdown voltage	I_{G2-SS} = ±10 mA; V_{G1-S} = V_{DS} = 0	±8	±20	V
$V_{(P)G1-S}$	gate 1-source cut-off voltage	I_D = 20 µA; V_{DS} = 10 V; V_{G2-S} = 4 V	–	−1.3	V
$V_{(P)G2-S}$	gate 2-source cut-off voltage	I_D = 20 µA; V_{DS} = 10 V; V_{G1-S} = 0	–	−1.1	V

DYNAMIC CHARACTERISTICS

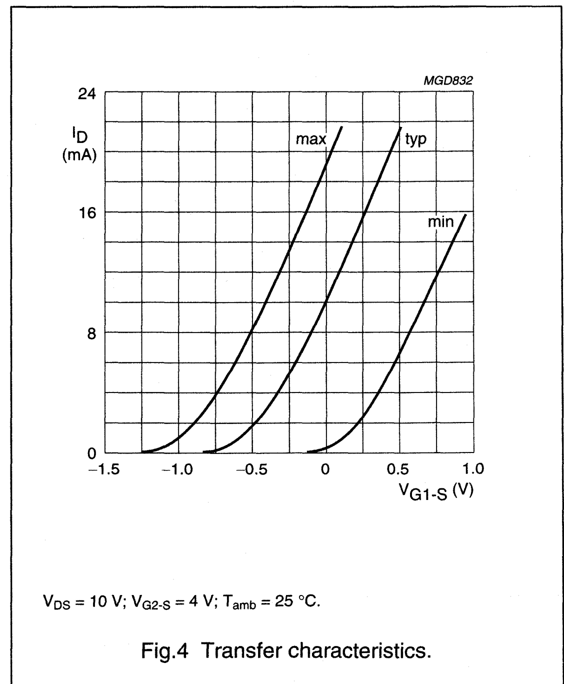
Measuring conditions (common source): I_D = 10 mA; V_{DS} = 10 V; V_{G2-S} = 4 V; T_{amb} = 25 °C.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\lvert Y_{fs} \rvert$	transfer admittance	f = 1 kHz	18	19	–	mS
C_{ig1-s}	input capacitance at gate 1	f = 1 MHz	–	2.6	3	pF
C_{ig2-s}	input capacitance at gate 2	f = 1 MHz	–	1.4	–	pF
C_{rs}	feedback capacitance	f = 1 MHz	–	25	–	fF
C_{os}	output capacitance	f = 1 MHz	–	1.2	–	pF
F	noise figure	f = 800 MHz; G_S = 5 mS; B_S = B_{Sopt}	–	2	3	dB



V_{G2-S} = 4 V; T_{amb} = 25 °C.

Fig.3 Output characteristics.



V_{DS} = 10 V; V_{G2-S} = 4 V; T_{amb} = 25 °C.

Fig.4 Transfer characteristics.

N-channel dual-gate MOS-FET BF991

FEATURES

- Protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

APPLICATIONS

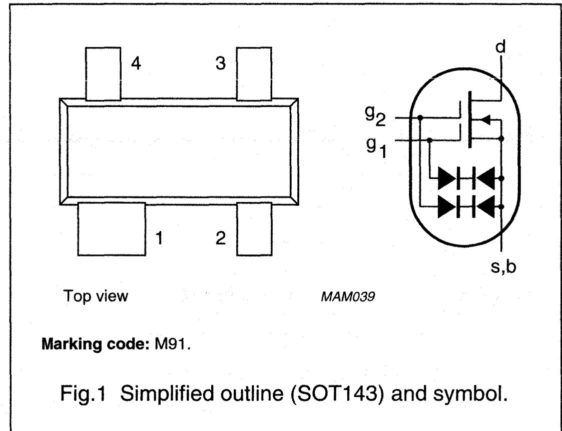
- VHF applications such as:
  - VHF television tuners and FM tuners
  - Professional communication equipment.

PINNING

PIN	SYMBOL	DESCRIPTION
1	s, b	source
2	d	drain
3	g_2	gate 2
4	g_1	gate 1

DESCRIPTION

Depletion type field-effect transistor in a plastic SOT143 microminiature package with interconnected source and substrate.



Marking code: M91.

Fig.1 Simplified outline (SOT143) and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
V_{DS}	drain-source voltage		–	20	V
I_D	drain current		–	20	mA
P_{tot}	total power dissipation	up to T_{amb} = 60 °C	–	200	mW
T_j	junction temperature		–	150	°C
$\|Y_{fs}\|$	transfer admittance	f = 1 kHz; I_D = 10 mA; V_{DS} = 10 V; $V_{G2\text{-}S}$ = 4 V	14	–	mS
$C_{ig1\text{-}s}$	input capacitance at gate 1	f = 1 MHz; I_D = 10 mA; V_{DS} = 10 V; $V_{G2\text{-}S}$ = 4 V	2.1	–	pF
C_{rs}	feedback capacitance	f = 1 MHz; I_D = 10 mA; V_{DS} = 10 V; $V_{G2\text{-}S}$ = 4 V	20	–	fF
F	noise figure	f = 200 MHz; G_S = 2 mS; B_S = B_{Sopt}; I_D = 10 mA; V_{DS} = 10 V; $V_{G2\text{-}S}$ = 4 V	1	2	dB

LIMITING VALUES

In according with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	20	V
I_D	drain current (DC)		–	20	mA
$I_{D(AV)}$	average drain current		–	20	mA
I_{G1-S}	gate 1-source current		–	±10	mA
I_{G2-S}	gate 2-source current		–	±10	mA
P_{tot}	total power dissipation	up to T_{amb} = 60 °C; note 1	–	200	mW
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–	150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	in free air; note 1	460	K/W

Note to the Limiting values and the Thermal characteristics

1. Device mounted on a ceramic substrate of 8 × 10 × 0.7 mm.

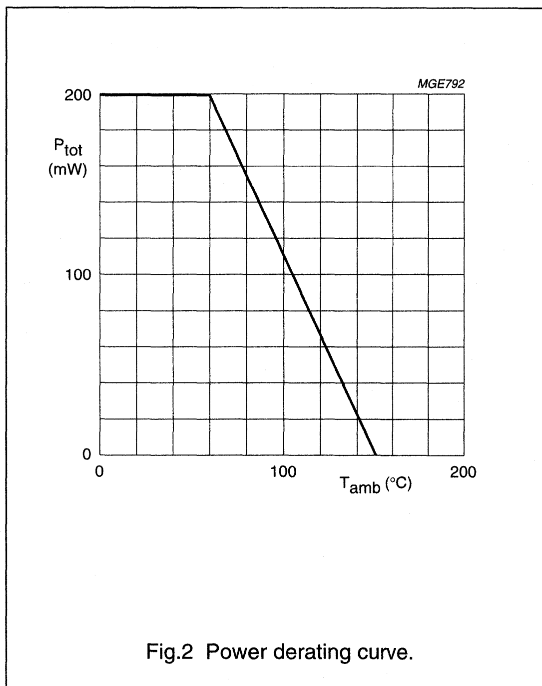


Fig.2 Power derating curve.

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{G1-SS}	gate 1 cut-off current	V_{G1-S} = 5 V; V_{G2-S} = V_{DS} = 0	–	50	nA
I_{G2-SS}	gate 2 cut-off current	V_{G2-S} = 5 V; V_{G1-S} = V_{DS} = 0	–	50	nA
I_{DSS}	drain current	V_{DS} = 10 V; V_{G1-S} = 0; V_{G2-S} = 4 V	4	25	mA
$V_{(BR)G1-SS}$	gate 1-source breakdown voltage	I_{G1-SS} = 10 mA; V_{G2-S} = V_{DS} = 0	6	20	V
$V_{(BR)G2-SS}$	gate 2-source breakdown voltage	I_{G2-SS} = 10 mA; V_{G1-S} = V_{DS} = 0	6	20	V
$V_{(P)G1-S}$	gate 1-source cut-off voltage	I_D = 20 μA; V_{DS} = 10 V; V_{G2-S} = 4 V	–	–2.5	V
$V_{(P)G2-S}$	gate 2-source cut-off voltage	I_D = 20 μA; V_{DS} = 10 V; V_{G1-S} = 0	–	–2.5	V

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): I_D = 10 mA; V_{DS} = 10 V; V_{G2-S} = 4 V; T_{amb} = 25 °C.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\lvert Y_{fs} \rvert$	transfer admittance	f = 1 kHz	10	14	–	mS
C_{ig1-s}	input capacitance at gate 1	f = 1 MHz	–	2.1	–	pF
C_{ig2-s}	input capacitance at gate 2	f = 1 MHz	–	1	–	pF
C_{rs}	feedback capacitance	f = 1 MHz	–	20	–	fF
C_{os}	output capacitance	f = 1 MHz	–	1.1	–	pF
F	noise figure	f = 100 MHz; G_S = 1 mS; B_S = B_{Sopt}	–	0.7	1.7	dB
		f = 200 MHz; G_S = 2 mS; B_S = B_{Sopt}	–	1	2	dB
G_{tr}	transducer gain; note 1	f = 100 MHz; G_S = 1 mS; B_S = B_{Sopt}; G_L = 0.5 mS; B_L = B_{Lopt}	–	29	–	dB
		f = 200 MHz; G_S = 2 mS; B_S = B_{Sopt}; G_L = 0.5 mS; B_L = B_{Lopt}	–	26	–	dB

Note

1. Crystal mounted in a SOT103 package.

Silicon N-channel dual-gate MOS-FETs

BF992; BF992R

APPLICATIONS

- VHF applications such as VHF television tuners and FM tuners with 12 V supply voltage. The device is also suitable for use in professional communications equipment.

DESCRIPTION

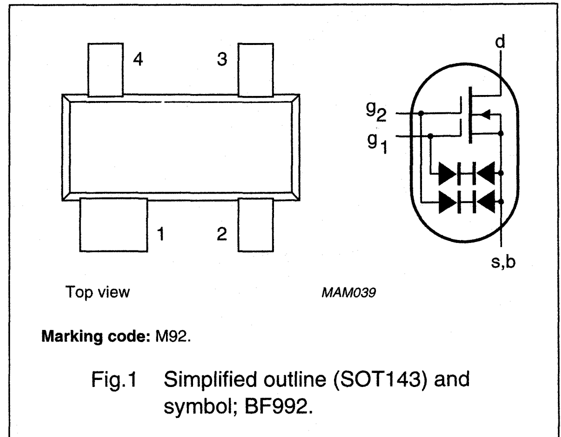
Depletion type field-effect transistor in a plastic micro-miniature SOT143 or SOT143R package with source and substrate interconnected.

The transistors are protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

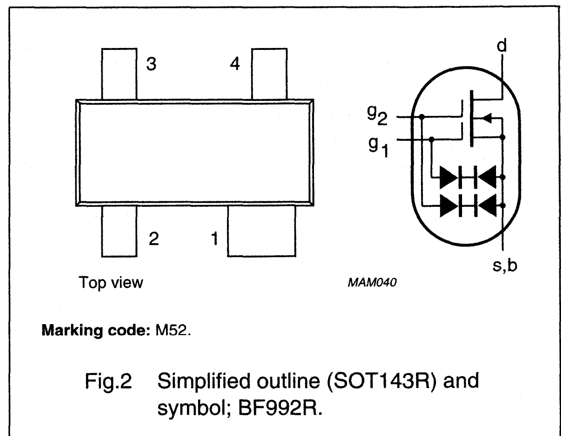
PINNING

PIN	SYMBOL	DESCRIPTION
1	s,b	source
2	d	drain
3	g_2	gate 2
4	g_1	gate 1



Marking code: M92.

Fig.1 Simplified outline (SOT143) and symbol; BF992.



Marking code: M52.

Fig.2 Simplified outline (SOT143R) and symbol; BF992R.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	20	V
I_D	drain current (DC)		–	40	mA
P_{tot}	total power dissipation	T_{amb} = 60 °C	–	200	mW
$\|Y_{fs}\|$	forward transfer admittance	f = 1 kHz; I_D = 15 mA; V_{DS} = 10 V; V_{G2-S} = 4 V	25	–	mS
C_{ig1-s}	input capacitance at gate 1	f = 1 MHz; I_D = 15 mA; V_{DS} = 10 V; V_{G2-S} = 4 V	4	–	pF
C_{rs}	reverse transfer capacitance	f = 1 MHz; I_D = 15 mA; V_{DS} = 10 V; V_{G2-S} = 4 V	30	–	fF
F	noise figure	G_S = 2 mS; I_D = 15 mA; V_{DS} = 10 V; V_{G2-S} = 4 V; f = 200 MHz	1.2	–	dB
T_j	operating junction temperature		–	150	°C

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	20	V
I_D	drain current		–	40	mA
$\pm I_{G1}$	gate 1 current		–	10	mA
$\pm I_{G2}$	gate 2 current		–	10	mA
P_{tot}	total power dissipation	up to T_{amb} = 60 °C; see Fig.3; note 1	–	200	mW
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–	150	°C

Note

1. Device mounted on a ceramic substrate, 8 mm × 10 mm × 0.7 mm.

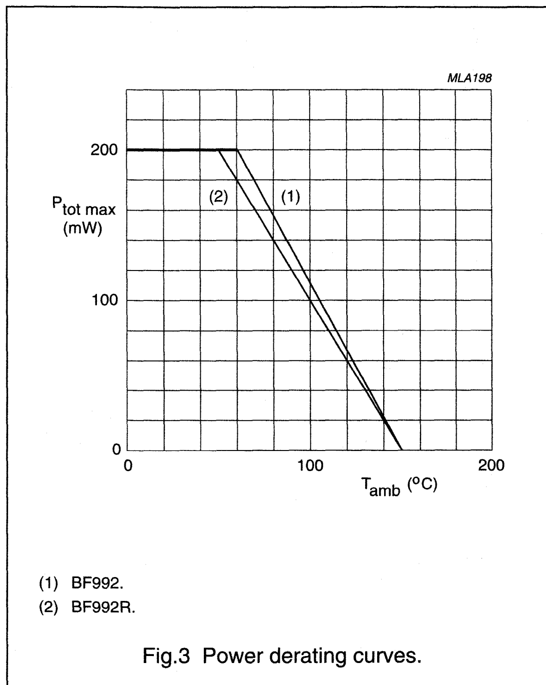


Fig.3 Power derating curves.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	note 1		
	BF992		460	K/W
	BF992R		500	K/W

Note

1. Device mounted on a ceramic substrate, 8 mm × 10 mm × 0.7 mm.

STATIC CHARACTERISTICS

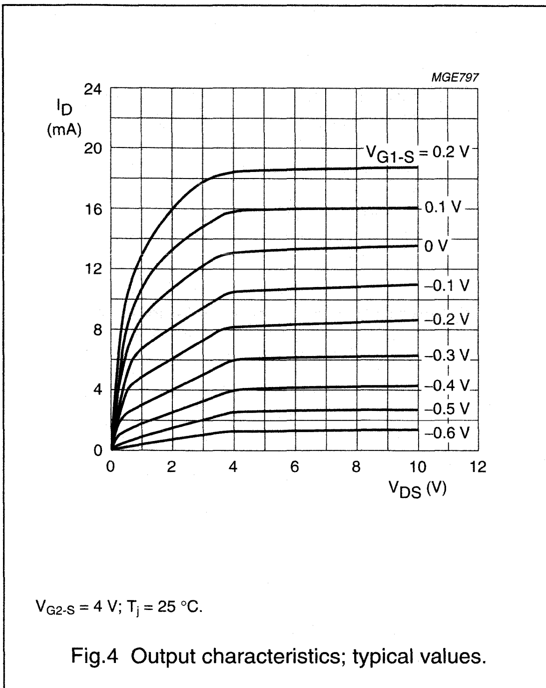
T_j = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$\pm V_{(BR)G1\text{-}SS}$	gate 1-source breakdown voltage	$V_{G2\text{-}S} = V_{DS} = 0$; $I_{G1\text{-}SS} = \pm10$ mA	8	20	V
$\pm V_{(BR)G2\text{-}SS}$	gate 2-source breakdown voltage	$V_{G1\text{-}S} = V_{DS} = 0$; $I_{G2\text{-}SS} = \pm10$ mA	8	20	V
$-V_{(P)G1\text{-}S}$	gate 1-source cut-off voltage	$V_{G2\text{-}S} = 4$ V; $V_{DS} = 10$ V; $I_D = 20$ µA	0.2	1.3	V
$-V_{(P)G2\text{-}S}$	gate 2-source cut-off voltage	$V_{G1\text{-}S} = 0$; $V_{DS} = 10$ V; $I_D = 20$ µA	0.2	1.1	V
$\pm I_{G1\text{-}SS}$	gate 1 cut-off current	$V_{G2\text{-}S} = V_{DS} = 0$; $V_{G1\text{-}S} = \pm7$ V	–	25	nA
$\pm I_{G2\text{-}SS}$	gate 2 cut-off current	$V_{G1\text{-}S} = V_{DS} = 0$; $V_{G2\text{-}S} = \pm7$ V	–	25	nA

DYNAMIC CHARACTERISTICS

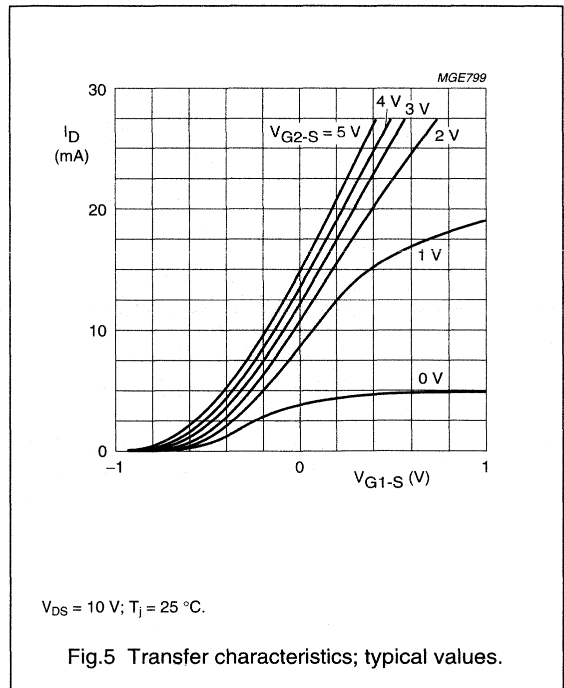
Common source; T_{amb} = 25 °C; V_{DS} = 10 V; $V_{G2\text{-}S}$ = 4 V; I_D = 15 mA; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\lvert y_{fs} \rvert$	forward transfer admittance		20	25	–	mS
$C_{ig1\text{-}s}$	input capacitance at gate 1	f = 1 MHz	–	4	–	pF
$C_{ig2\text{-}s}$	input capacitance at gate 2	f = 1 MHz	–	1.7	–	pF
C_{os}	output capacitance	f = 1 MHz	–	2	–	pF
C_{rs}	reverse transfer capacitance	f = 1 MHz	–	30	40	fF
F	noise figure	f = 200 MHz; G_S = 2 mS	–	1.2	–	dB



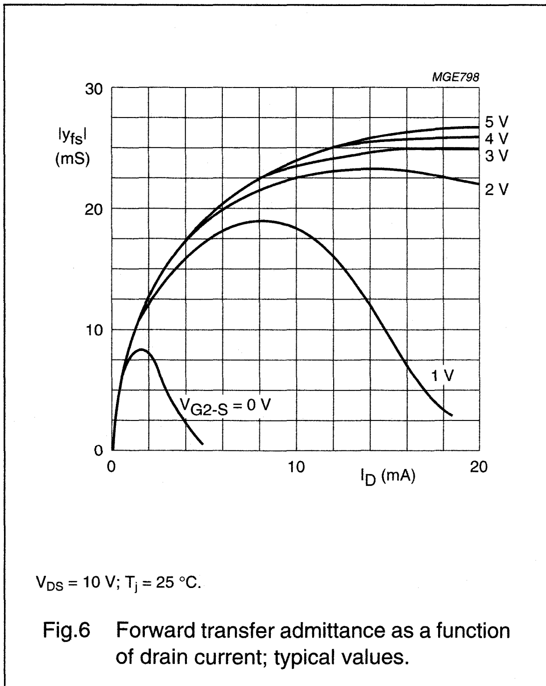
V_{G2-S} = 4 V; T_j = 25 °C.

Fig.4 Output characteristics; typical values.



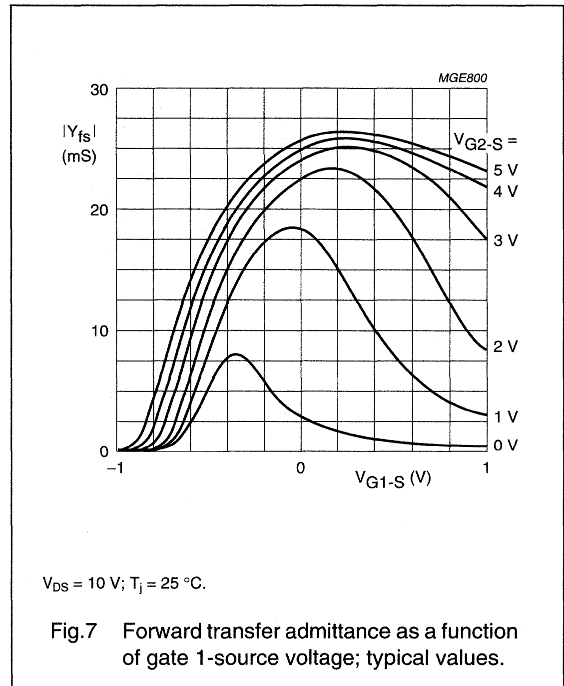
V_{DS} = 10 V; T_j = 25 °C.

Fig.5 Transfer characteristics; typical values.



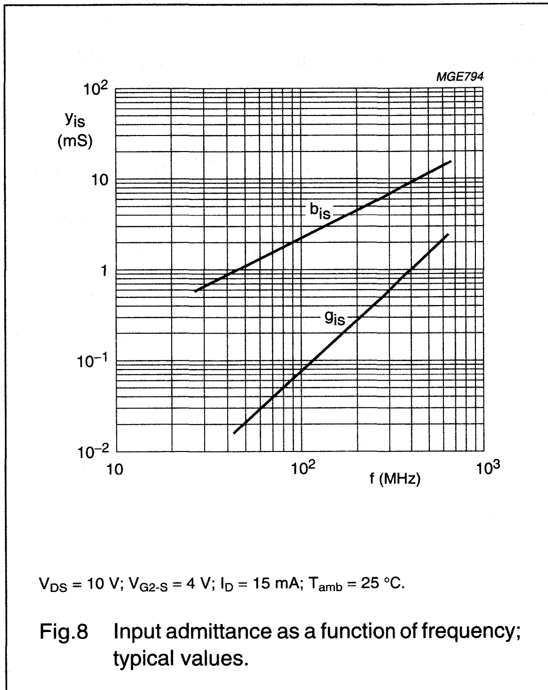
V_{DS} = 10 V; T_j = 25 °C.

Fig.6 Forward transfer admittance as a function of drain current; typical values.



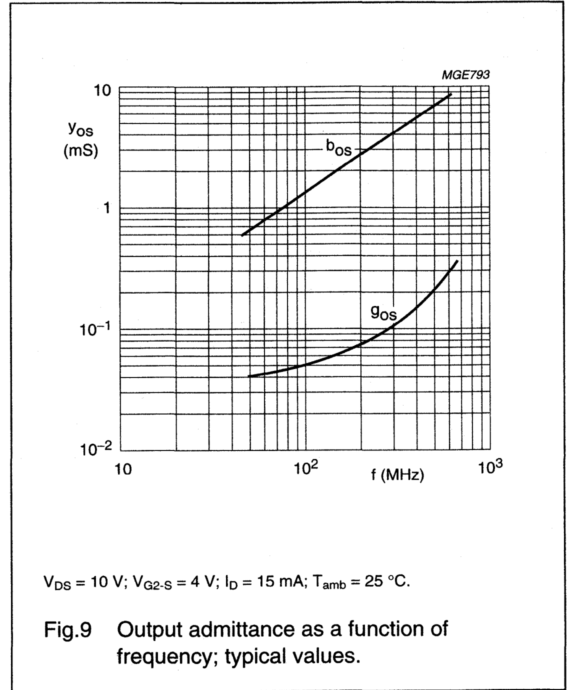
V_{DS} = 10 V; T_j = 25 °C.

Fig.7 Forward transfer admittance as a function of gate 1-source voltage; typical values.



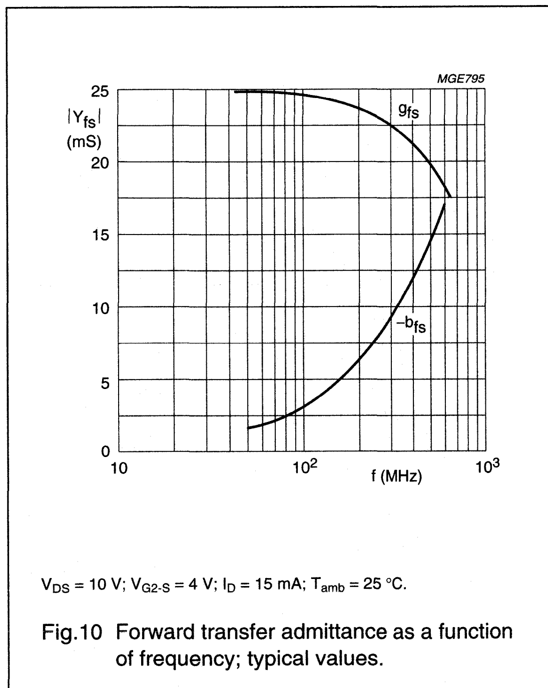
V_{DS} = 10 V; $V_{G2\text{-}S}$ = 4 V; I_D = 15 mA; T_{amb} = 25 °C.

Fig.8 Input admittance as a function of frequency; typical values.



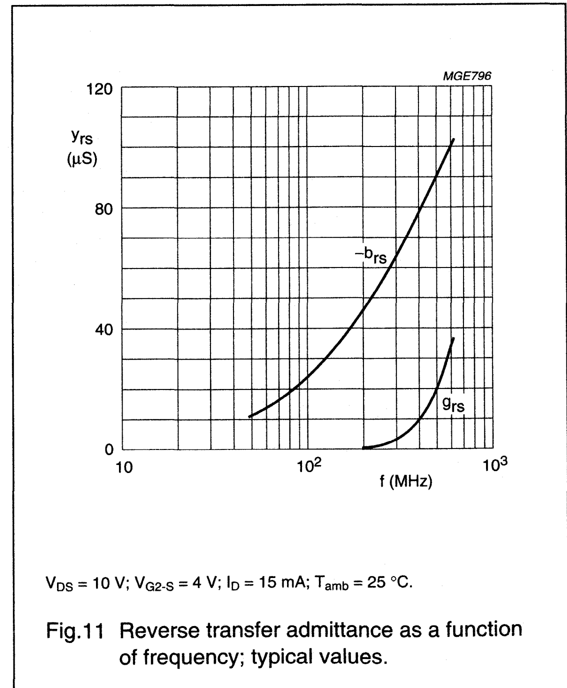
V_{DS} = 10 V; $V_{G2\text{-}S}$ = 4 V; I_D = 15 mA; T_{amb} = 25 °C.

Fig.9 Output admittance as a function of frequency; typical values.



V_{DS} = 10 V; $V_{G2\text{-}S}$ = 4 V; I_D = 15 mA; T_{amb} = 25 °C.

Fig.10 Forward transfer admittance as a function of frequency; typical values.



V_{DS} = 10 V; $V_{G2\text{-}S}$ = 4 V; I_D = 15 mA; T_{amb} = 25 °C.

Fig.11 Reverse transfer admittance as a function of frequency; typical values.

N-channel dual-gate MOS-FET

BF994S

FEATURES

- Protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

APPLICATIONS

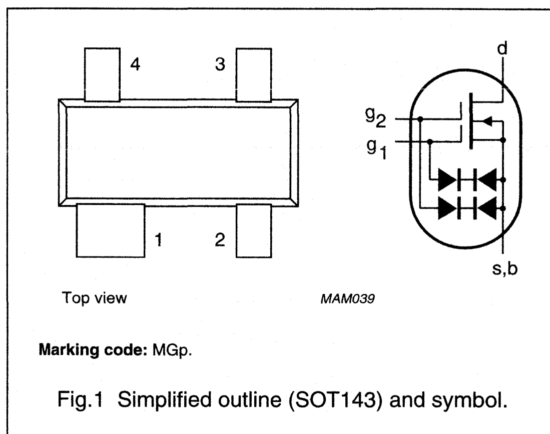
- VHF applications such as:
  - VHF television tuners
  - Professional communication equipment.

PINNING

PIN	SYMBOL	DESCRIPTION
1	s, b	source
2	d	drain
3	g_2	gate 2
4	g_1	gate 1

DESCRIPTION

Depletion type field-effect transistor in a plastic SOT143 microminiature package with interconnected source and substrate.



Marking code: MGp.

Fig.1 Simplified outline (SOT143) and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
V_{DS}	drain-source voltage		–	20	V
I_D	drain current		–	30	mA
P_{tot}	total power dissipation	up to T_{amb} = 60 °C	–	200	mW
T_j	junction temperature		–	150	°C
$\lvert Y_{fs} \rvert$	transfer admittance	f = 1 kHz; I_D = 10 mA; V_{DS} = 15 V; V_{G2-S} = 4 V	18	–	mS
C_{ig1-s}	input capacitance at gate 1	f = 1 MHz; I_D = 10 mA; V_{DS} = 15 V; V_{G2-S} = 4 V	2.5	3	pF
C_{rs}	feedback capacitance	f = 1 MHz; I_D = 10 mA; V_{DS} = 15 V; V_{G2-S} = 4 V	25	–	fF
F	noise figure	f = 200 MHz; G_S = 2 mS; B_S = B_{Sopt}; I_D = 10 mA; V_{DS} = 15 V; V_{G2-S} = 4 V	1	–	dB

LIMITING VALUES

In according with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	20	V
I_D	drain current (DC)		–	30	mA
$I_{D(AV)}$	average drain current		–	30	mA
I_{G1-S}	gate 1-source current		–	±10	mA
I_{G2-S}	gate 2-source current		–	±10	mA
P_{tot}	total power dissipation	up to T_{amb} = 60 °C; note 1	–	200	mW
T_{stg}	storage temperature range		–65	+150	°C
T_j	junction temperature		–	150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient	in free air; note 1	460	K/W

Note to the Limiting values and the Thermal characteristics

1. Device mounted on a ceramic substrate of 8 × 10 × 0.7 mm.

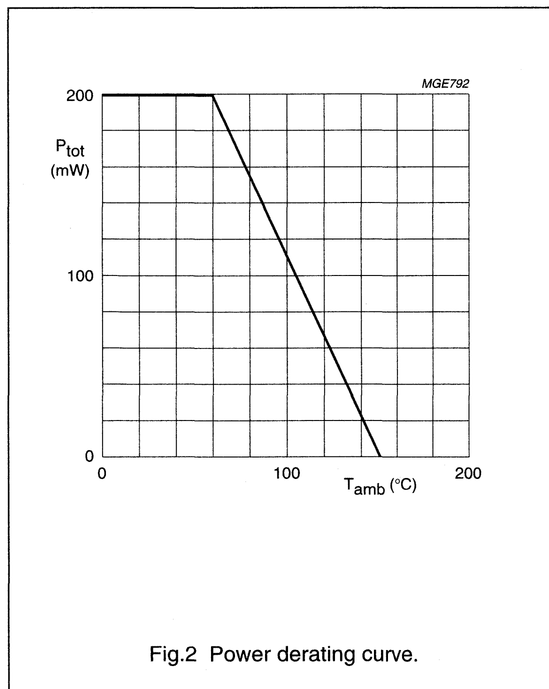


Fig.2 Power derating curve.

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$I_{G1\text{-}SS}$	gate 1 cut-off currents	$V_{G1\text{-}S}$ = ±5 V; $V_{G2\text{-}S}$ = V_{DS} = 0	–	±50	nA
$I_{G2\text{-}SS}$	gate 2 cut-off currents	$V_{G2\text{-}S}$ = ±5 V; $V_{G1\text{-}S}$ = V_{DS} = 0	–	±50	nA
$V_{(BR)G1\text{-}SS}$	gate 1-source breakdown voltage	$I_{G1\text{-}SS}$ = ±10 mA; $V_{G2\text{-}S}$ = V_{DS} = 0	±6	±20	V
$V_{(BR)G2\text{-}SS}$	gate 2-source breakdown voltage	$I_{G2\text{-}SS}$ = ±10 mA; $V_{G1\text{-}S}$ = V_{DS} = 0	±6	±20	V
I_{DSS}	drain-source cut-off voltage	V_{DS} = 15 V; $V_{G1\text{-}S}$ = 0; $V_{G2\text{-}S}$ = 4 V	4	20	mA
$V_{(P)G1\text{-}S}$	gate 1-source cut-off voltage	I_D = 20 μA; V_{DS} = 15 V; $V_{G2\text{-}S}$ = 4 V	–	–2.5	V
$V_{(P)G2\text{-}S}$	gate 2-source cut-off voltage	I_D = 20 μA; V_{DS} = 15 V; $V_{G1\text{-}S}$ = 0	–	–2	V

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): I_D = 10 mA; V_{DS} = 15 V; $V_{G2\text{-}S}$ = 4 V; T_{amb} = 25 °C.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\|Y_{fs}\|$	transfer admittance	f = 1 kHz	15	18	–	mS
$C_{ig1\text{-}s}$	input capacitance at gate 1	f = 1 MHz	–	2.5	3	pF
$C_{ig2\text{-}s}$	input capacitance at gate 2	f = 1 MHz	–	1.2	–	pF
C_{rs}	feedback capacitance	f = 1 MHz	–	25	–	fF
C_{os}	output capacitance	f = 1 MHz	–	1	–	pF
F	noise figure	f = 200 MHz; G_S = 2 mS; B_S = B_{Sopt}	–	1	–	dB
G_p	power gain	f = 200 MHz; G_S = 2 mS; B_S = B_{Sopt}; G_L = 0.5 mS; B_L = B_{Lopt}	–	25	–	dB

N-channel dual-gate MOS-FET — BF996S

FEATURES

- Protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

APPLICATIONS

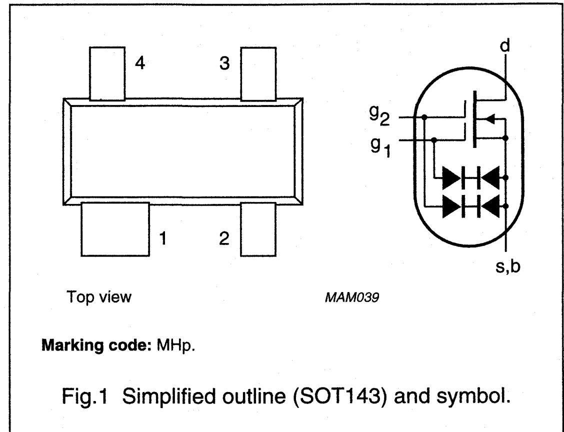
- RF applications such as:
  - UHF television tuners
  - Professional communication equipment.

PINNING

PIN	SYMBOL	DESCRIPTION
1	s, b	source
2	d	drain
3	g_2	gate 2
4	g_1	gate 1

DESCRIPTION

Depletion type field-effect transistor in a plastic SOT143 microminiature package with interconnected source and substrate.



Marking code: MHp.

Fig.1 Simplified outline (SOT143) and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
V_{DS}	drain-source voltage		–	20	V
I_D	drain current		–	30	mA
P_{tot}	total power dissipation	up to T_{amb} = 60 °C	–	200	mW
T_j	junction temperature		–	150	°C
$\|Y_{fs}\|$	transfer admittance	f = 1 kHz; I_D = 10 mA; V_{DS} = 15 V; V_{G2-S} = 4 V	18	–	mS
C_{ig-1s}	input capacitance at gate 1	f = 1 MHz; I_D = 10 mA; V_{DS} = 15 V; V_{G2-S} = 4 V	2.3	2.6	pF
C_{rs}	feedback capacitance	f = 1 MHz; I_D = 10 mA; V_{DS} = 15 V; V_{G2-S} = 4 V	25	–	fF
F	noise figure	f = 200 MHz G_S = 2 mS; B_S = B_{Sopt}; I_D = 10 mA; V_{DS} = 15 V; V_{GS-2} = 4 V	1	–	dB

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	20	V
I_D	drain current (DC)		–	30	mA
$I_{D(AV)}$	average drain current		–	30	mA
I_{G1-S}	gate 1 source		–	±10	mA
I_{G1-S}	gate 2 source		–	±10	mA
P_{tot}	total power dissipation	up to T_{amb} = 60 °C; note 1	–	200	mW
T_{stg}	storage temperature range		–65	+150	°C
T_j	junction temperature		–	150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient	in free air; note 1	460	K/W

Note to the Limiting values and the Thermal characteristics

1. Device mounted on a ceramic substrate of 8 × 10 × 0.7 mm.

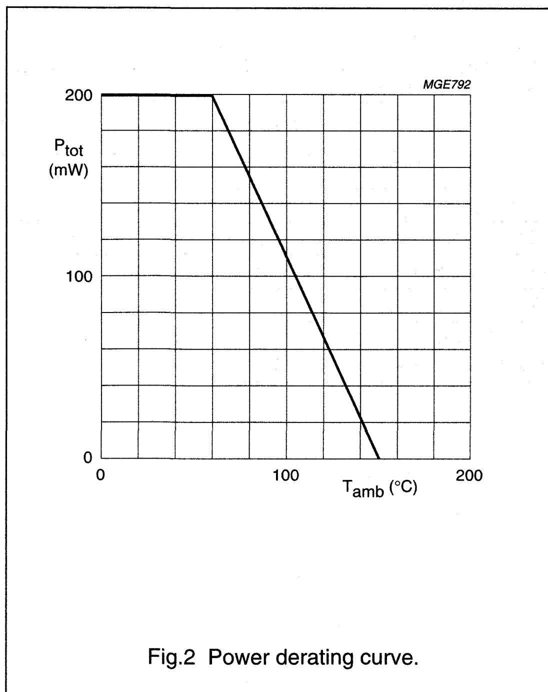


Fig.2 Power derating curve.

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{G1-SS}	gate cut-off current	V_{G1-S} = ±5 V; V_{G2-S} = V_{DS} = 0	–	±50	nA
I_{G2-SS}	gate cut-off current	V_{G2-S} = ±5 V; V_{G1-S} = V_{DS} = 0	–	±50	nA
$V_{(BR)G1-SS}$	gate-source breakdown voltage	I_{G1-S} = ±10 mA; V_{G2-S} = V_{DS} = 0	±6	±20	V
$V_{(BR)G2-SS}$	gate-source breakdown voltage	I_{G2-S} = ±10 mA; V_{G1-S} = V_{DS} = 0	±6	±20	V
I_{DSS}	drain current	V_{DS} = 15 V; V_{G1-S} = 0; V_{G2-S} = 4 V	4	20	mA
$V_{(P)G1-S}$	gate-source cut-off current	I_D = 20 µA; V_{DS} = 15 V; V_{G2-S} = 4 V	–	–2.5	V
$V_{(P)G2-S}$	gate-source cut-off current	I_D = 20 µA; V_{DS} = 15 V; V_{G1-S} = 0	–	–2	V

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): I_D = 10 mA; V_{DS} = 15 V; V_{G2-S} = 4 V; T_{amb} = 25 °C.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\|Y_{fs}\|$	transfer admittance	f = 1 kHz	15	18	–	mS
C_{ig1-s}	input capacitance at gate 1	f = 1 MHz	–	2.3	2.6	pF
C_{ig2-s}	input capacitance at gate 2	f = 1 MHz	–	1.2	–	pF
C_{rs}	feedback capacitance	f = 1 MHz	–	25	–	fF
C_{os}	output capacitance	f = 1 MHz	–	0.8	–	pF
F	noise figure	f = 200 MHz; G_S = 2 mS; B_S = B_{Sopt}	–	1	–	dB
		f = 800 MHz; G_S = 3.3 mS; B_S = B_{Sopt}	–	1.8	–	dB
G_P	power gain	f = 200 MHz; G_S = 2 mS; B_S = B_{Sopt}; G_L = 0.5 mS; B_L = B_{Lopt}	–	25	–	dB
		f = 800 MHz; G_S = 3.3 mS; B_S = B_{Sopt}; G_L = 1 mS; B_L = B_{Lopt}	–	18	–	dB

Silicon N-channel dual-gate MOS-FETs

BF998; BF998R

FEATURES

- Short channel transistor with high forward transfer admittance to input capacitance ratio
- Low noise gain controlled amplifier up to 1 GHz.

APPLICATIONS

- VHF and UHF applications with 12 V supply voltage, such as television tuners and professional communications equipment.

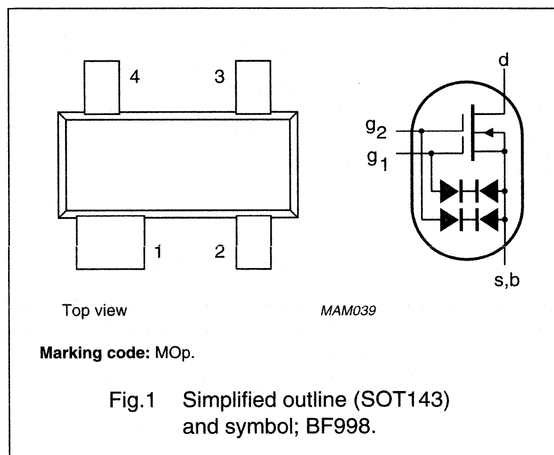
DESCRIPTION

Depletion type field effect transistor in a plastic microminiature SOT143 or SOT143R package with source and substrate interconnected. The transistors are protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

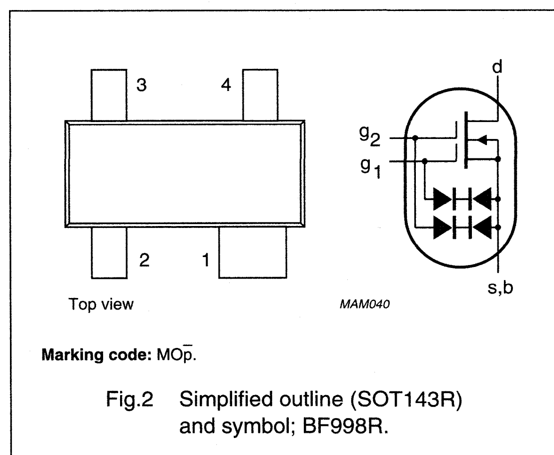
PINNING

PIN	SYMBOL	DESCRIPTION
1	s, b	source
2	d	drain
3	g_2	gate 2
4	g_1	gate 1



Marking code: MOp.

Fig.1 Simplified outline (SOT143) and symbol; BF998.



Marking code: MOp̄.

Fig.2 Simplified outline (SOT143R) and symbol; BF998R.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
V_{DS}	drain-source voltage		–	12	V
I_D	drain current		–	30	mA
P_{tot}	total power dissipation		–	200	mW
$\lvert y_{fs} \rvert$	forward transfer admittance		24	–	mS
$C_{ig1\text{-}s}$	input capacitance at gate 1		2.1	–	pF
C_{rs}	reverse transfer capacitance	f = 1 MHz	25	–	fF
F	noise figure	f = 800 MHz	1	–	dB
T_j	operating junction temperature		–	150	°C

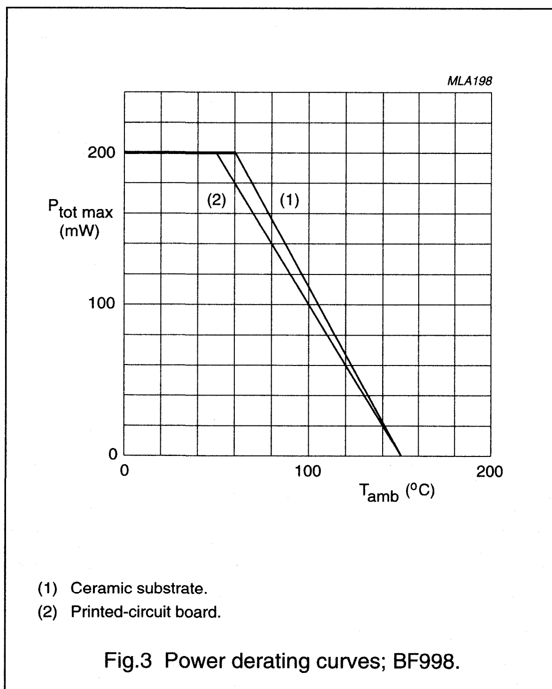
LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	12	V
I_D	drain current		–	30	mA
$\pm I_{G1}$	gate 1 current		–	10	mA
$\pm I_{G2}$	gate 2 current		–	10	mA
P_{tot}	total power dissipation; BF998	up to T_{amb} = 60 °C; see Fig.3; note 1	–	200	mW
		up to T_{amb} = 50 °C; see Fig.3; note 2	–	200	mW
P_{tot}	total power dissipation; BF998R	up to T_{amb} = 50 °C; see Fig.4; note 1	–	200	mW
T_{stg}	storage temperature		−65	+150	°C
T_j	operating junction temperature		–	150	°C

Notes

1. Device mounted on a ceramic substrate, 8 mm × 10 mm × 0.7 mm.
2. Device mounted on a printed-circuit board.



(1) Ceramic substrate.
(2) Printed-circuit board.

Fig.3 Power derating curves; BF998.

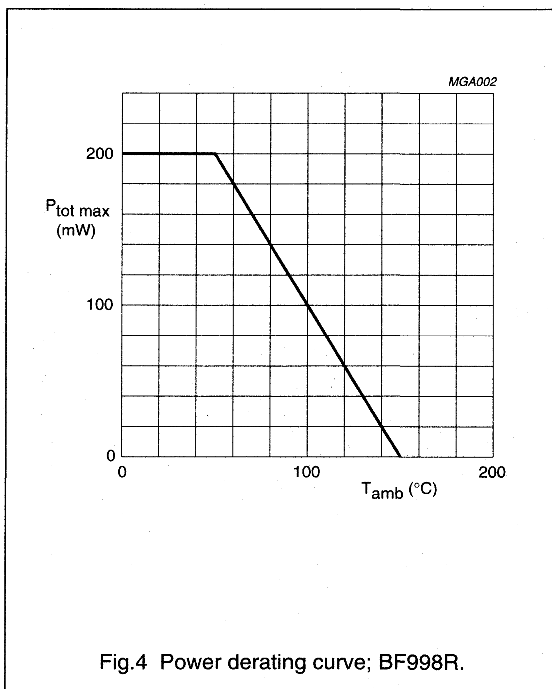


Fig.4 Power derating curve; BF998R.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air; BF998	note 1	460	K/W
		note 2	500	K/W
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air; BF998R	note 1	500	K/W

Notes

1. Device mounted on a ceramic substrate, 8 mm × 10 mm × 0.7 mm.
2. Device mounted on a printed-circuit board.

STATIC CHARACTERISTICS

T_j = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$\pm V_{(BR)G1\text{-}SS}$	gate 1-source breakdown voltage	$V_{G2\text{-}S} = V_{DS} = 0$; $I_{G1\text{-}SS} = \pm 10$ mA	6	20	V
$\pm V_{(BR)G2\text{-}SS}$	gate 2-source breakdown voltage	$V_{G1\text{-}S} = V_{DS} = 0$; $I_{G2\text{-}SS} = \pm 10$ mA	6	20	V
$-V_{(P)G1\text{-}S}$	gate 1-source cut-off voltage	$V_{G2\text{-}S} = 4$ V; $V_{DS} = 8$ V; $I_D = 20$ μA	–	2.0	V
$-V_{(P)G2\text{-}S}$	gate 2-source cut-off voltage	$V_{G1\text{-}S} = 0$; $V_{DS} = 8$ V; $I_D = 20$ μA	–	1.5	V
I_{DSS}	drain-source current	$V_{G2\text{-}S} = 4$ V; $V_{DS} = 8$ V; $V_{G1\text{-}S} = 0$; note 1	2	18	mA
$\pm I_{G1\text{-}SS}$	gate 1 cut-off current	$V_{G2\text{-}S} = V_{DS} = 0$; $V_{G1\text{-}S} = \pm 5$ V	–	50	nA
$\pm I_{G2\text{-}SS}$	gate 2 cut-off current	$V_{G1\text{-}S} = V_{DS} = 0$; $V_{G2\text{-}S} = \pm 5$ V	–	50	nA

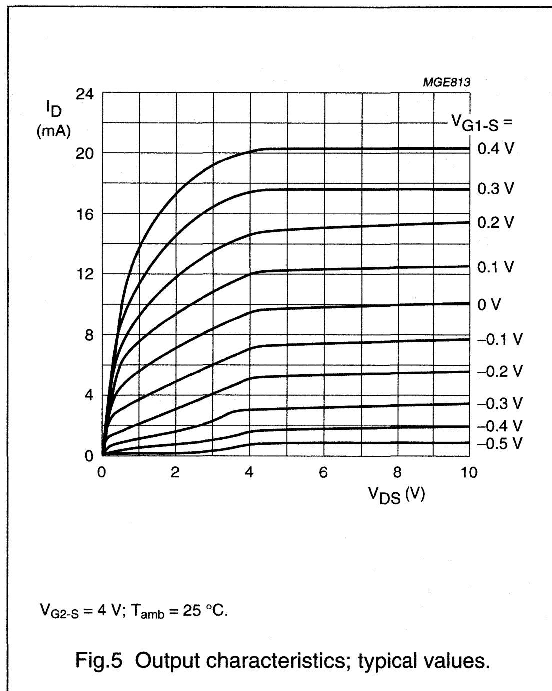
Note

1. Measured under pulse condition.

DYNAMIC CHARACTERISTICS

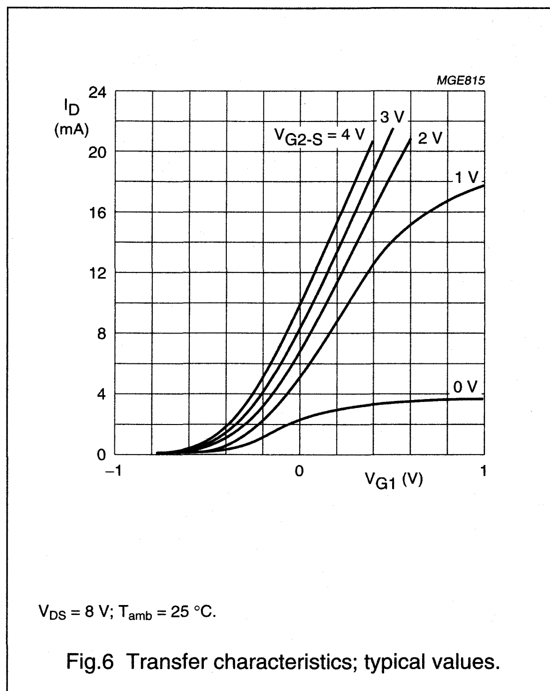
Common source; T_{amb} = 25 °C; V_{DS} = 8 V; $V_{G2\text{-}S}$ = 4 V; I_D = 10 mA.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\lvert y_{fs} \rvert$	forward transfer admittance	f = 1 kHz	21	24	–	mS
$C_{ig1\text{-}s}$	input capacitance at gate 1	f = 1 MHz	–	2.1	2.5	pF
$C_{ig2\text{-}s}$	input capacitance at gate 2	f = 1 MHz	–	1.2	–	pF
C_{os}	output capacitance	f = 1 MHz	–	1.05	–	pF
C_{rs}	reverse transfer capacitance	f = 1 MHz	–	25	–	fF
F	noise figure	f = 200 MHz; G_S = 2 mS; $B_S = B_{Sopt}$	–	0.6	–	dB
		f = 800 MHz; G_S = 3.3 mS; $B_S = B_{Sopt}$	–	1.0	–	dB



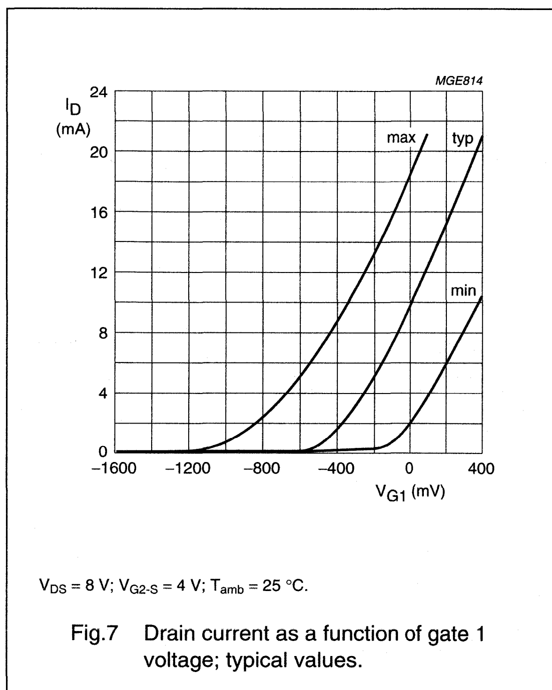
V_{G2-S} = 4 V; T_{amb} = 25 °C.

Fig.5 Output characteristics; typical values.



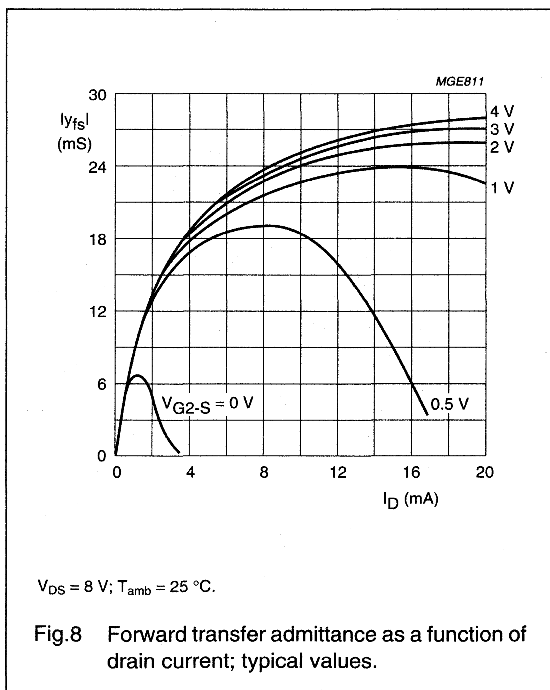
V_{DS} = 8 V; T_{amb} = 25 °C.

Fig.6 Transfer characteristics; typical values.



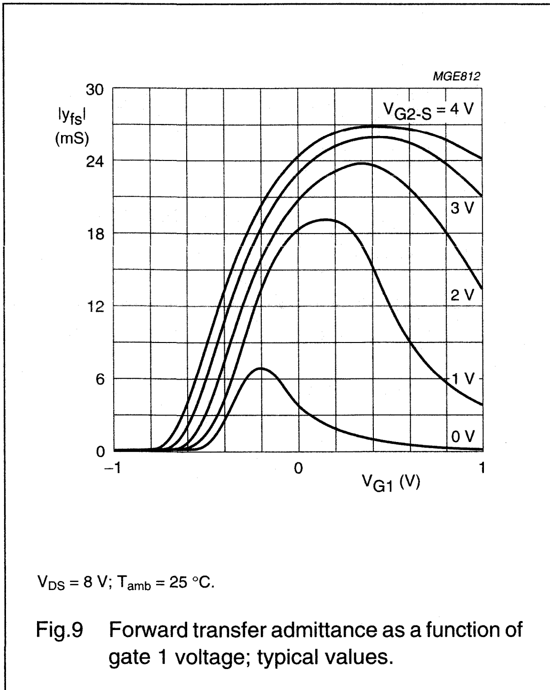
V_{DS} = 8 V; V_{G2-S} = 4 V; T_{amb} = 25 °C.

Fig.7 Drain current as a function of gate 1 voltage; typical values.



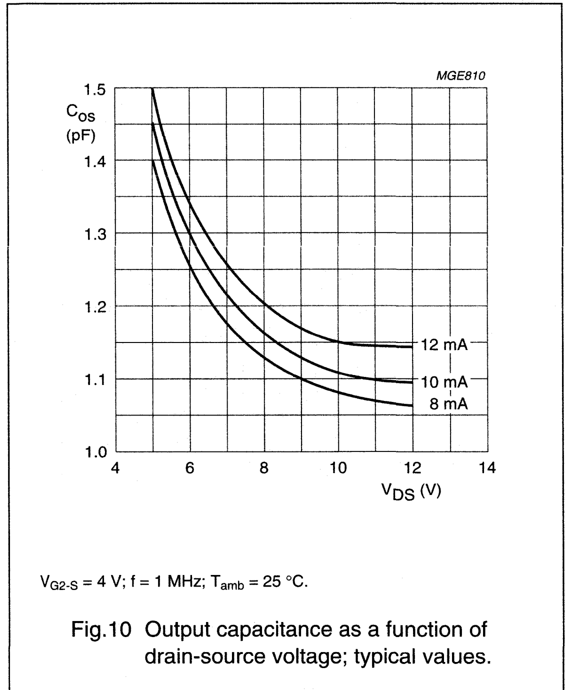
V_{DS} = 8 V; T_{amb} = 25 °C.

Fig.8 Forward transfer admittance as a function of drain current; typical values.



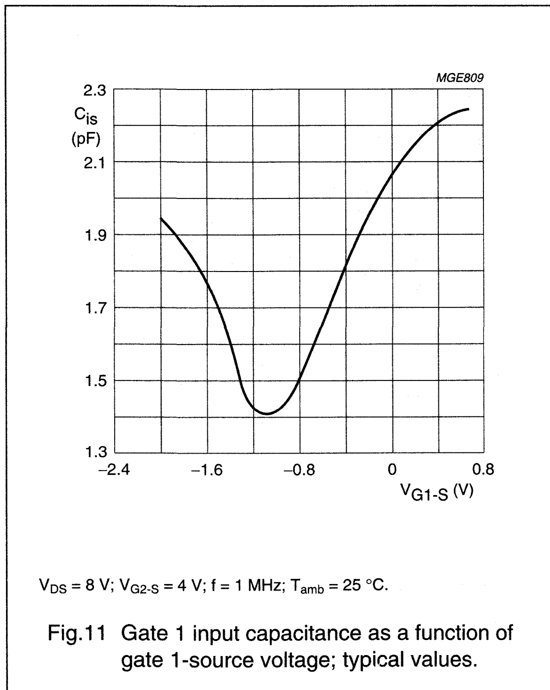
V_{DS} = 8 V; T_{amb} = 25 °C.

Fig.9 Forward transfer admittance as a function of gate 1 voltage; typical values.



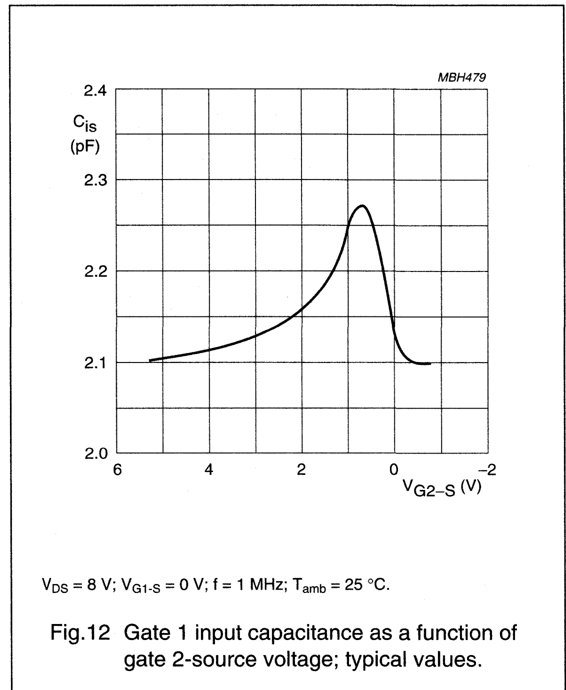
V_{G2-S} = 4 V; f = 1 MHz; T_{amb} = 25 °C.

Fig.10 Output capacitance as a function of drain-source voltage; typical values.



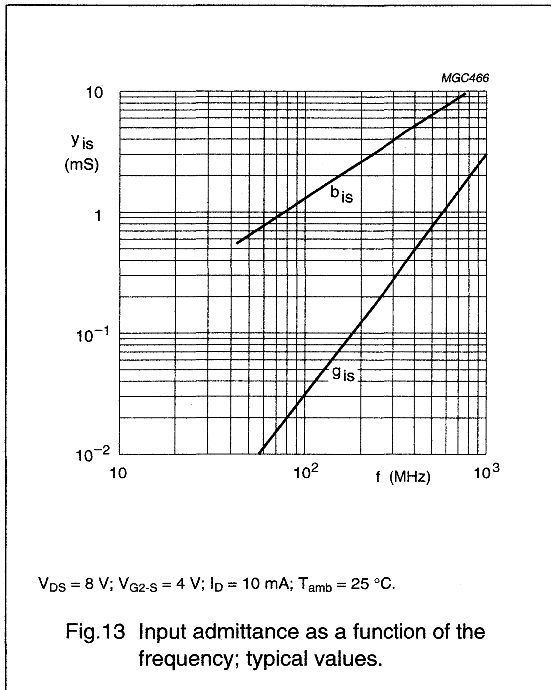
V_{DS} = 8 V; V_{G2-S} = 4 V; f = 1 MHz; T_{amb} = 25 °C.

Fig.11 Gate 1 input capacitance as a function of gate 1-source voltage; typical values.



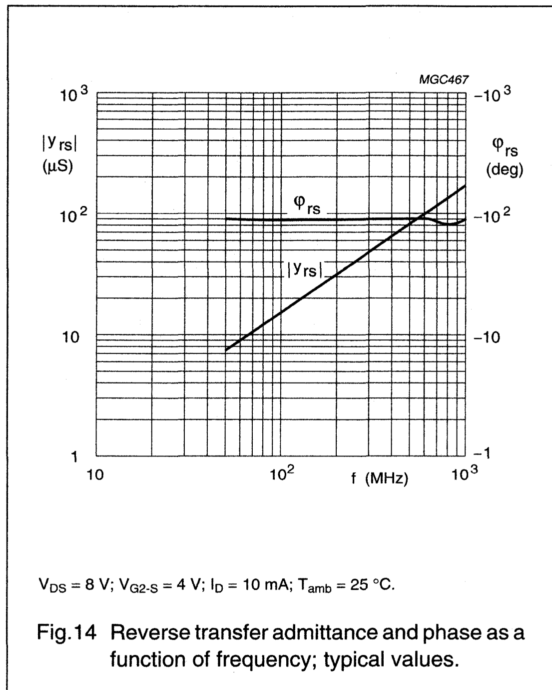
V_{DS} = 8 V; V_{G1-S} = 0 V; f = 1 MHz; T_{amb} = 25 °C.

Fig.12 Gate 1 input capacitance as a function of gate 2-source voltage; typical values.



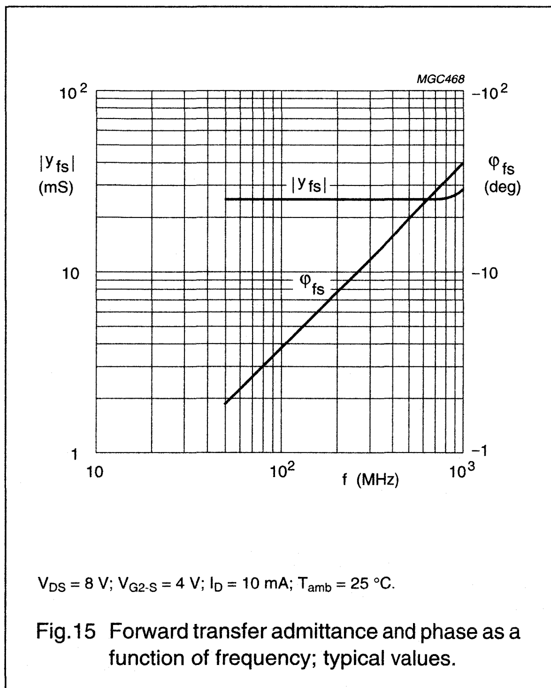
V_{DS} = 8 V; V_{G2-S} = 4 V; I_D = 10 mA; T_{amb} = 25 °C.

Fig.13 Input admittance as a function of the frequency; typical values.



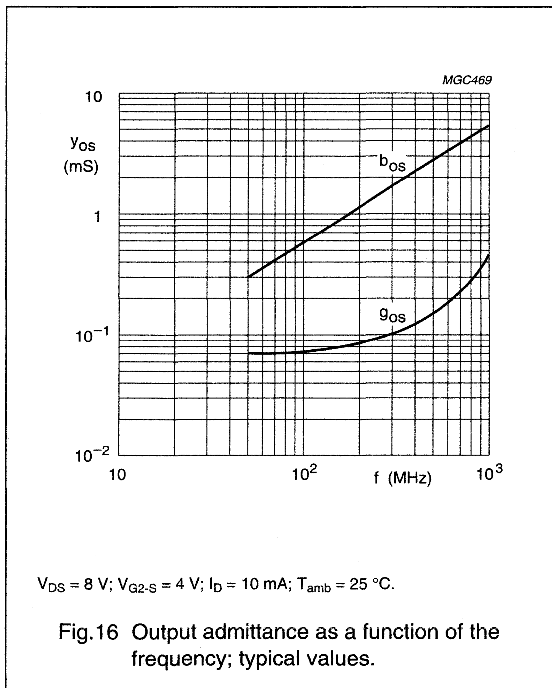
V_{DS} = 8 V; V_{G2-S} = 4 V; I_D = 10 mA; T_{amb} = 25 °C.

Fig.14 Reverse transfer admittance and phase as a function of frequency; typical values.



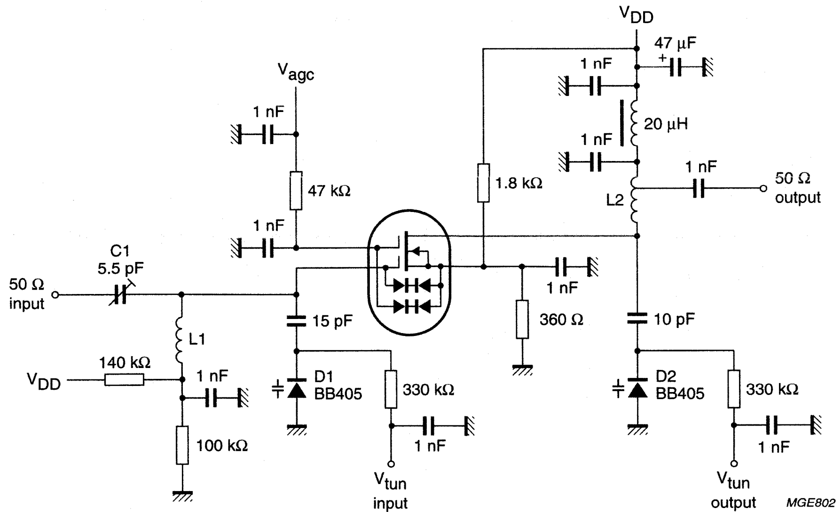
V_{DS} = 8 V; V_{G2-S} = 4 V; I_D = 10 mA; T_{amb} = 25 °C.

Fig.15 Forward transfer admittance and phase as a function of frequency; typical values.



V_{DS} = 8 V; V_{G2-S} = 4 V; I_D = 10 mA; T_{amb} = 25 °C.

Fig.16 Output admittance as a function of the frequency; typical values.



V_{DD} = 12 V; G_S = 2 mS; G_L = 0.5 mS.

L1 = 45 nH; 4 turns 0.8 mm copper wire, internal diameter 4 mm.

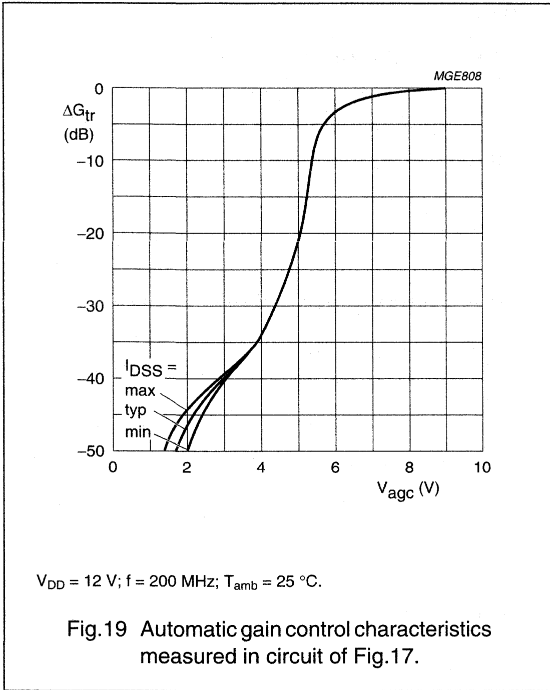
L2 = 160 nH; 3 turns 0.8 mm copper wire, internal diameter 8 mm.

Tapped at approximately half a turn from the cold side, to adjust G_L = 0.5 mS. C1 adjusted for G_S = 2 mS.

Fig.17 Gain control test circuit at f = 200 MHz.

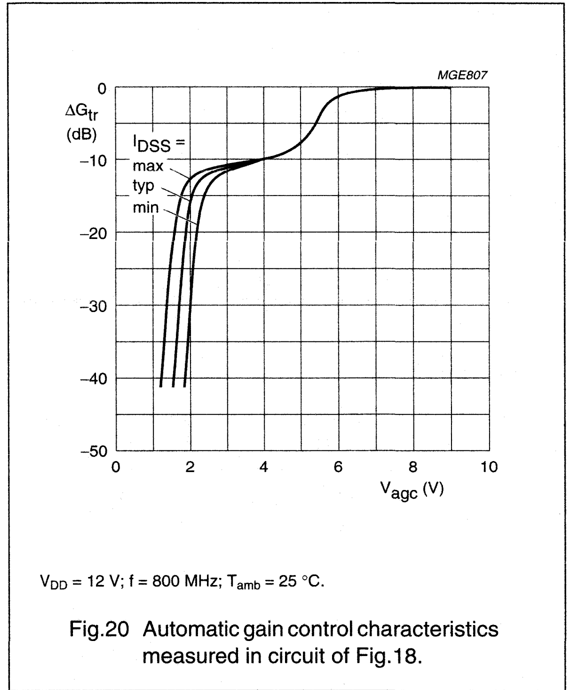
V_{DD} = 12 V; G_S = 3.3 mS; G_L = 1 mS.
L1 = L4 = 200 nH; 11 turns 0.5 mm copper wire, without spacing, internal diameter 3 mm.
L2 = 2 cm, silvered 0.8 mm copper wire, 4 mm above ground plane.
L3 = 2 cm, silvered 0.5 mm copper wire, 4 mm above ground plane.

Fig.18 Gain control test circuit at f = 800 MHz.



V_{DD} = 12 V; f = 200 MHz; T_{amb} = 25 °C.

Fig.19 Automatic gain control characteristics measured in circuit of Fig.17.



V_{DD} = 12 V; f = 800 MHz; T_{amb} = 25 °C.

Fig.20 Automatic gain control characteristics measured in circuit of Fig.18.

N-channel dual-gate MOS-FET BF998WR

FEATURES

- High forward transfer admittance
- Short channel transistor with high forward transfer admittance to input capacitance ratio
- Low noise gain controlled amplifier up to 1 GHz.

APPLICATIONS

- VHF and UHF applications with 12 V supply voltage, such as television tuners and professional communications equipment.

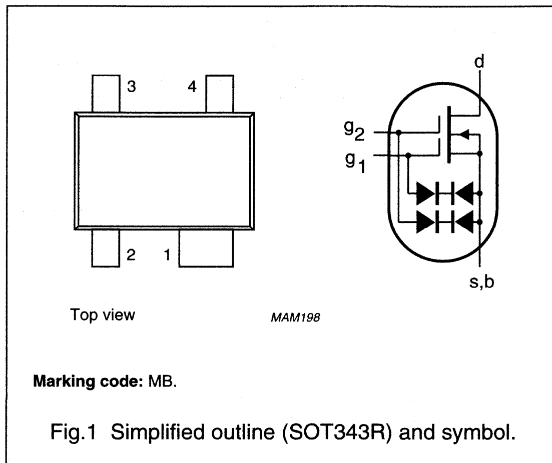
DESCRIPTION

Depletion type field-effect transistor in a plastic microminiature SOT343R package with source and substrate interconnected. The transistor is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING

PIN	SYMBOL	DESCRIPTION
1	s, b	source
2	d	drain
3	g_2	gate 2
4	g_1	gate 1



Marking code: MB.

Fig.1 Simplified outline (SOT343R) and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DS}	drain-source voltage		–	–	12	V
I_D	drain current		–	–	30	mA
P_{tot}	total power dissipation		–	–	300	mW
T_j	operating junction temperature		–	–	150	°C
$\|y_{fs}\|$	forward transfer admittance		–	24	–	mS
C_{ig1-s}	input capacitance at gate 1		–	2.1	–	pF
C_{rs}	reverse transfer capacitance	f = 1 MHz	–	25	–	fF
F	noise figure	f = 800 MHz	–	1	–	dB

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	12	V
I_D	drain current		–	30	mA
I_{G1}	gate 1 current		–	±10	mA
I_{G2}	gate 2 current		–	±10	mA
P_{tot}	total power dissipation	up to T_{amb} = 45 °C; see Fig.2; note 1	–	300	mW
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–	+150	°C

Note

1. Device mounted on a printed-circuit board.

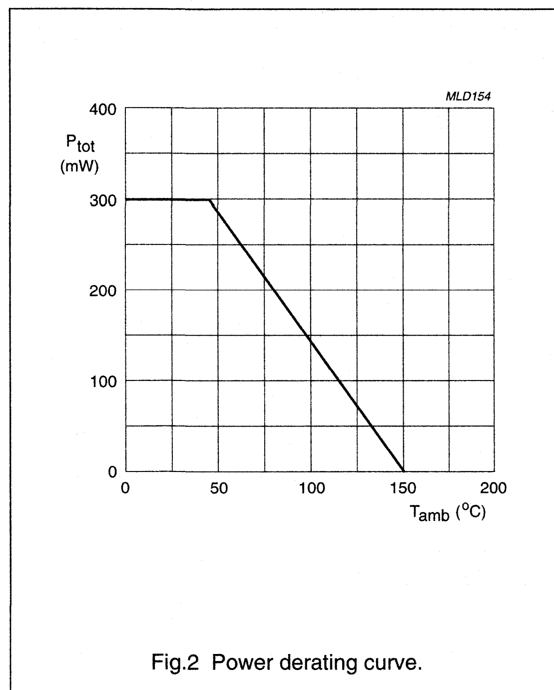


Fig.2 Power derating curve.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	note 1	350	K/W
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	note 2; T_s = 90 °C	200	K/W

Notes

1. Device mounted on a printed-circuit board.
2. T_s is the temperature at the soldering point of the source lead.

STATIC CHARACTERISTICS

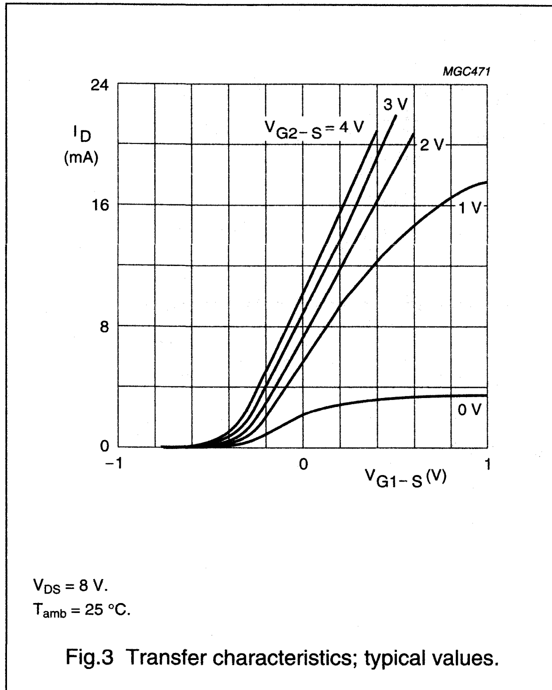
T_j = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{(BR)G1\text{-}SS}$	gate 1-source breakdown voltage	$V_{G2\text{-}S} = V_{DS} = 0$; $I_{G1\text{-}S}$ = 10 mA	6	20	V
$V_{(BR)G2\text{-}SS}$	gate 2-source breakdown voltage	$V_{G1\text{-}S} = V_{DS} = 0$; $I_{G2\text{-}S}$ = 10 mA	6	20	V
$V_{(P)G1\text{-}S}$	gate 1-source cut-off voltage	$V_{G2\text{-}S}$ = 4 V; V_{DS} = 8 V; I_D = 20 µA	–	–2.5	V
$V_{(P)G2\text{-}S}$	gate 2-source cut-off voltage	$V_{G1\text{-}S}$ = 0; V_{DS} = 8 V; I_D = 20 µA	–	–2	V
I_{DSS}	drain-source current	$V_{G2\text{-}S}$ = 4 V; V_{DS} = 8 V; $V_{G1\text{-}S}$ = 0	2	18	mA
$I_{G1\text{-}SS}$	gate 1 cut-off current	$V_{G2\text{-}S} = V_{DS} = 0$; $V_{G1\text{-}S}$ = 5 V	–	50	nA
$I_{G2\text{-}SS}$	gate 2 cut-off current	$V_{G1\text{-}S} = V_{DS} = 0$; $V_{G2\text{-}S}$ = 5 V	–	50	nA

DYNAMIC CHARACTERISTICS

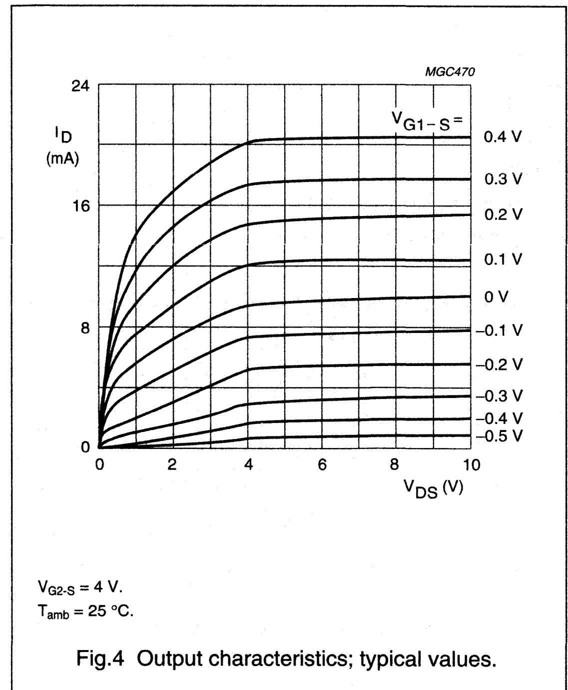
Common source; T_{amb} = 25 °C; $V_{G2\text{-}S}$ = 4 V; I_D = 10 mA; V_{DS} = 8 V; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\lvert y_{fs} \rvert$	forward transfer admittance	pulsed; T_j = 25 °C	22	25	–	mS
$C_{ig1\text{-}s}$	input capacitance at gate 1	f = 1 MHz	–	2.1	2.5	pF
$C_{ig2\text{-}s}$	input capacitance at gate 2	f = 1 MHz	–	1.2	–	pF
C_{os}	drain-source capacitance	f = 1 MHz	–	1.05	–	pF
C_{rs}	reverse transfer capacitance	f = 1 MHz	–	25	–	fF
F	noise figure	f = 200 MHz; G_S = 2 mS; $B_S = B_{Sopt}$	–	0.6	–	dB
		f = 800 MHz; G_S = 3.3 mS; $B_S = B_{Sopt}$	–	1	–	dB



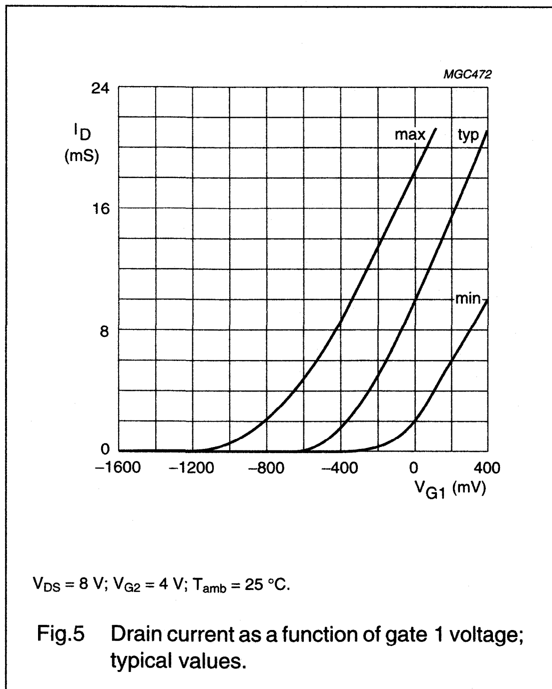
V_{DS} = 8 V.
T_{amb} = 25 °C.

Fig.3 Transfer characteristics; typical values.



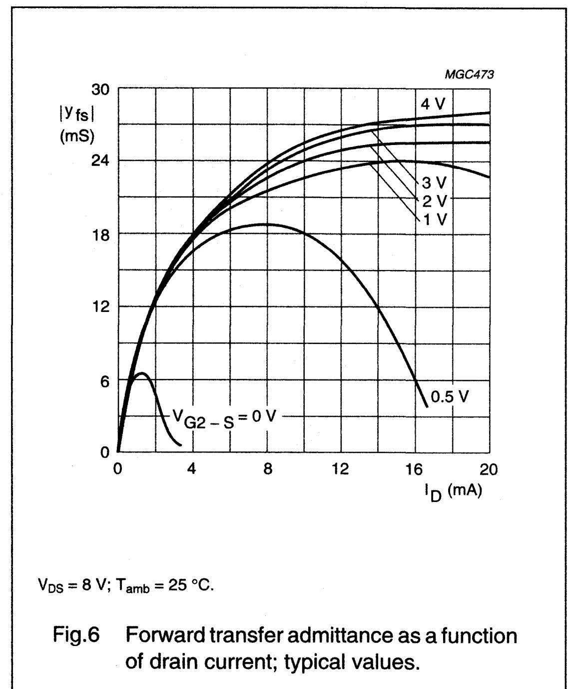
V_{G2-S} = 4 V.
T_{amb} = 25 °C.

Fig.4 Output characteristics; typical values.



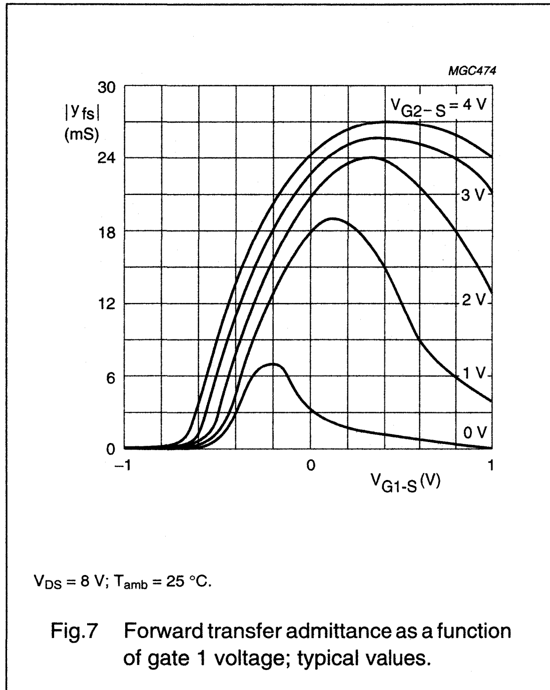
V_{DS} = 8 V; V_{G2} = 4 V; T_{amb} = 25 °C.

Fig.5 Drain current as a function of gate 1 voltage; typical values.



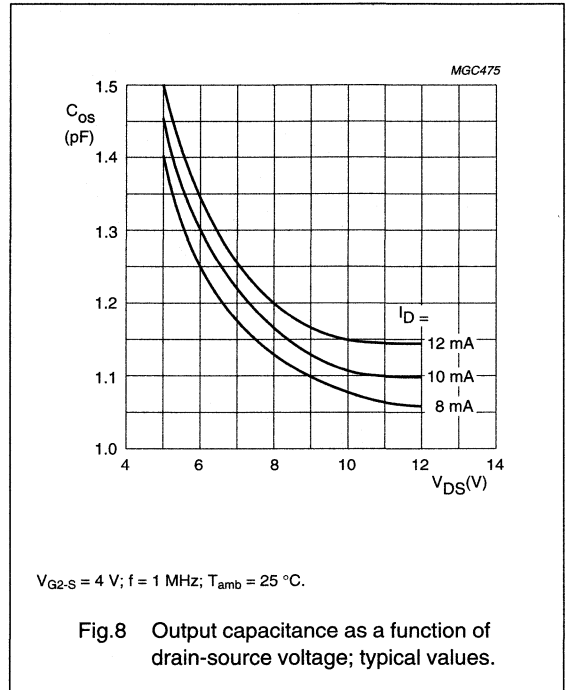
V_{DS} = 8 V; T_{amb} = 25 °C.

Fig.6 Forward transfer admittance as a function of drain current; typical values.



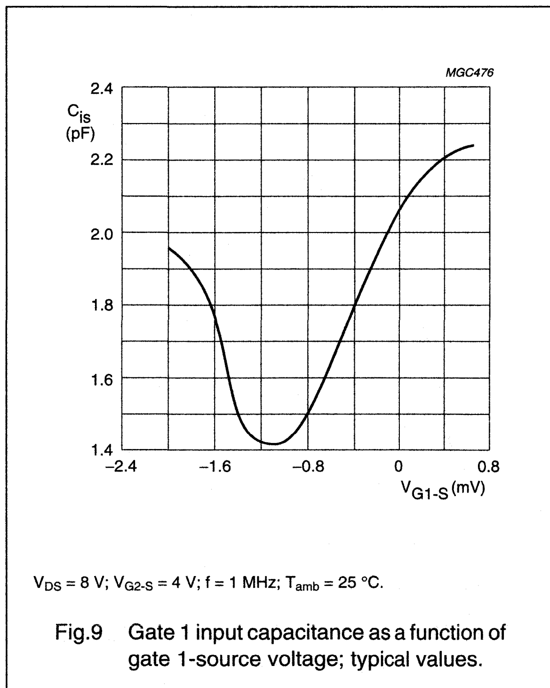
V_{DS} = 8 V; T_{amb} = 25 °C.

Fig.7 Forward transfer admittance as a function of gate 1 voltage; typical values.



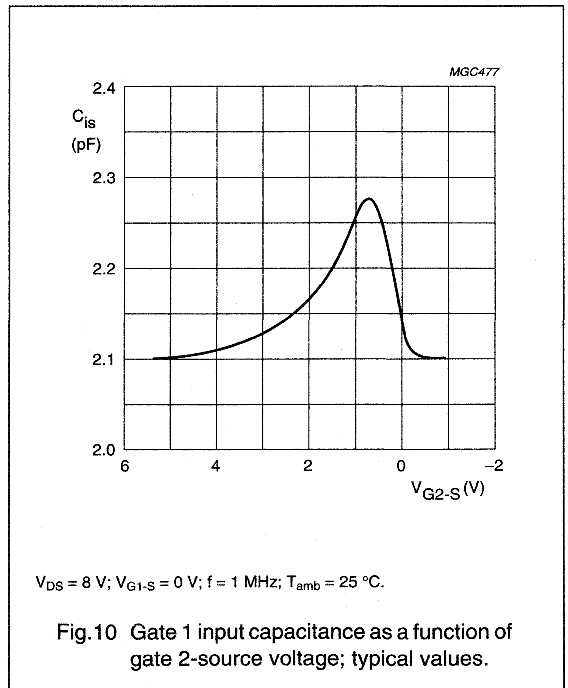
$V_{G2\text{-}S}$ = 4 V; f = 1 MHz; T_{amb} = 25 °C.

Fig.8 Output capacitance as a function of drain-source voltage; typical values.



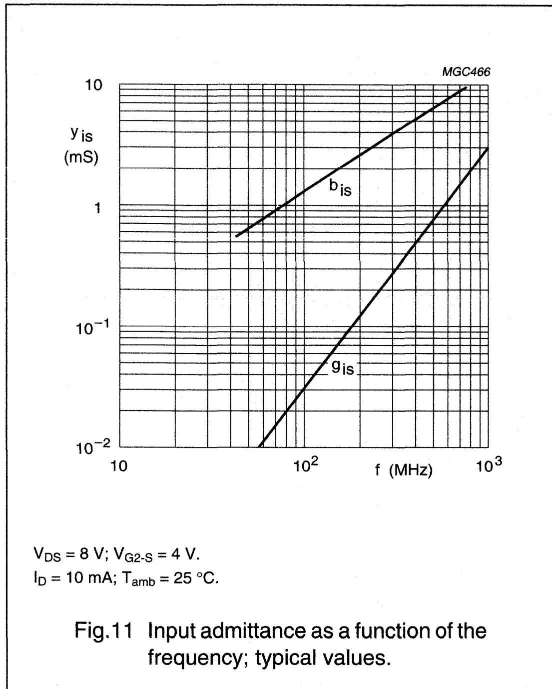
V_{DS} = 8 V; $V_{G2\text{-}S}$ = 4 V; f = 1 MHz; T_{amb} = 25 °C.

Fig.9 Gate 1 input capacitance as a function of gate 1-source voltage; typical values.



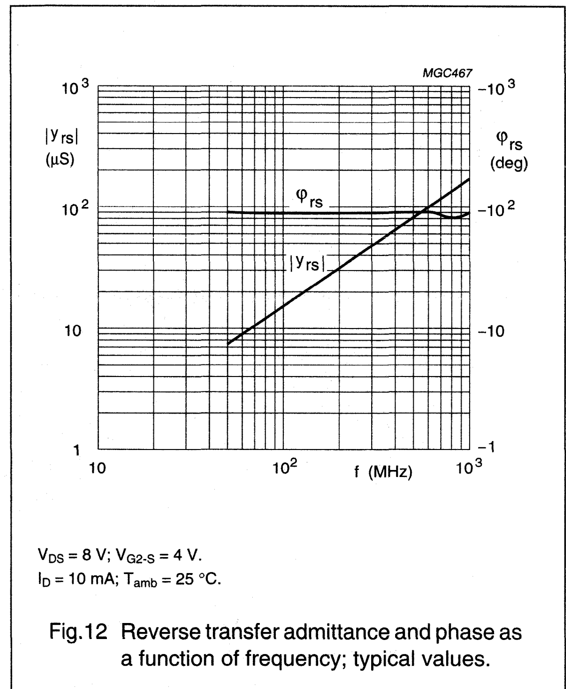
V_{DS} = 8 V; $V_{G1\text{-}S}$ = 0 V; f = 1 MHz; T_{amb} = 25 °C.

Fig.10 Gate 1 input capacitance as a function of gate 2-source voltage; typical values.



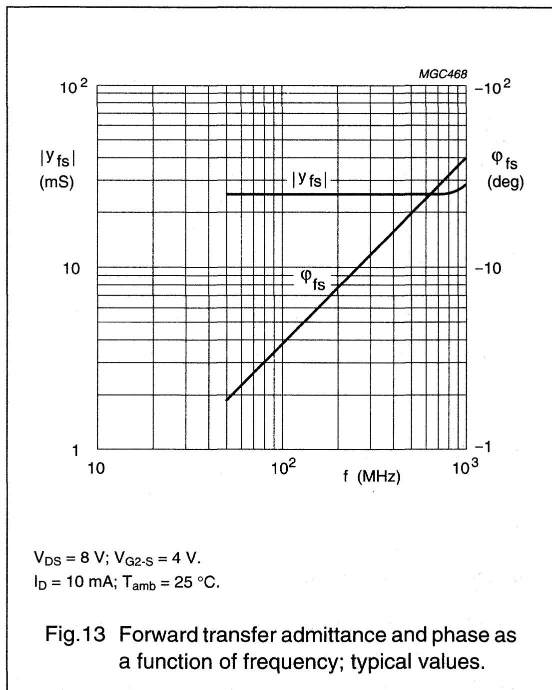
V_{DS} = 8 V; V_{G2-S} = 4 V.
I_D = 10 mA; T_{amb} = 25 °C.

Fig.11 Input admittance as a function of the frequency; typical values.



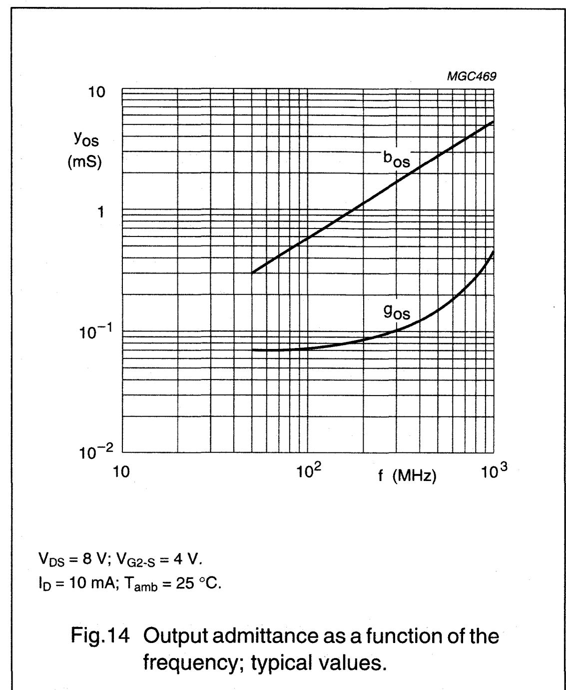
V_{DS} = 8 V; V_{G2-S} = 4 V.
I_D = 10 mA; T_{amb} = 25 °C.

Fig.12 Reverse transfer admittance and phase as a function of frequency; typical values.



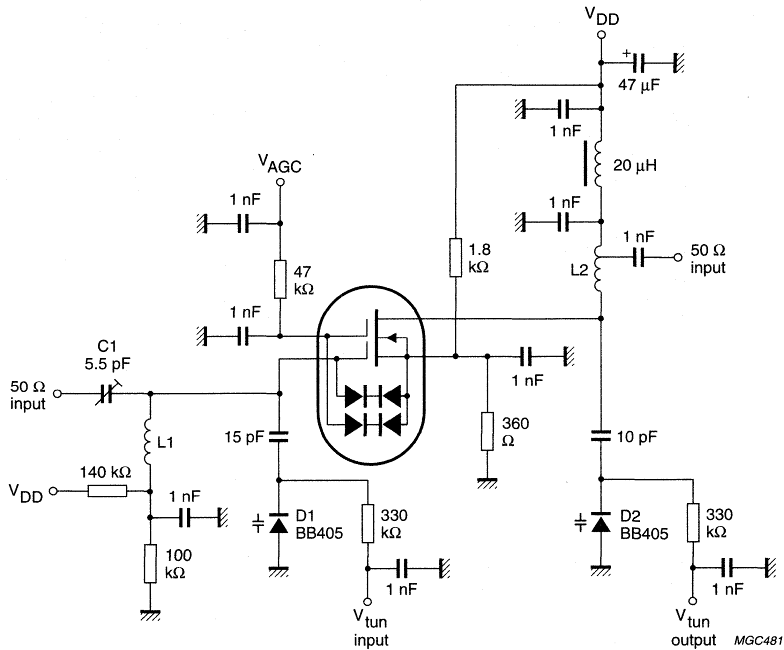
V_{DS} = 8 V; V_{G2-S} = 4 V.
I_D = 10 mA; T_{amb} = 25 °C.

Fig.13 Forward transfer admittance and phase as a function of frequency; typical values.



V_{DS} = 8 V; V_{G2-S} = 4 V.
I_D = 10 mA; T_{amb} = 25 °C.

Fig.14 Output admittance as a function of the frequency; typical values.



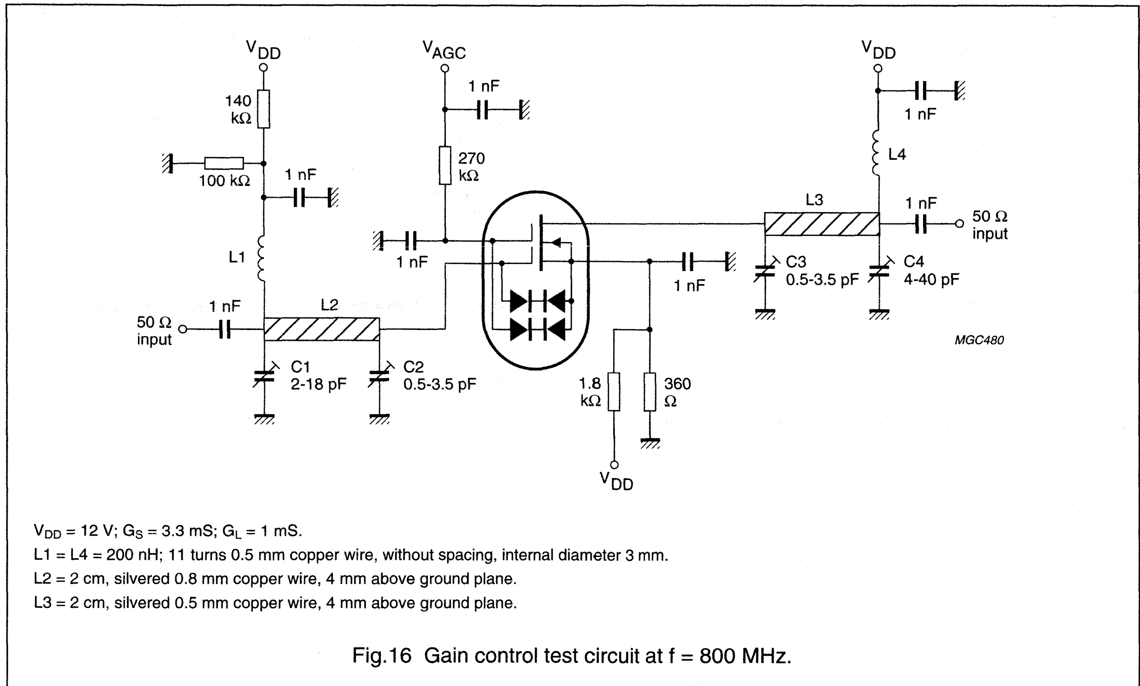
V_{DD} = 12 V; G_S = 2 mS; G_L = 0.5 mS.

L1 = 45 nH; 4 turns 0.8 mm copper wire, internal diameter 4 mm.

L2 = 160 nH; 3 turns 0.8 mm copper wire, internal diameter 8 mm.

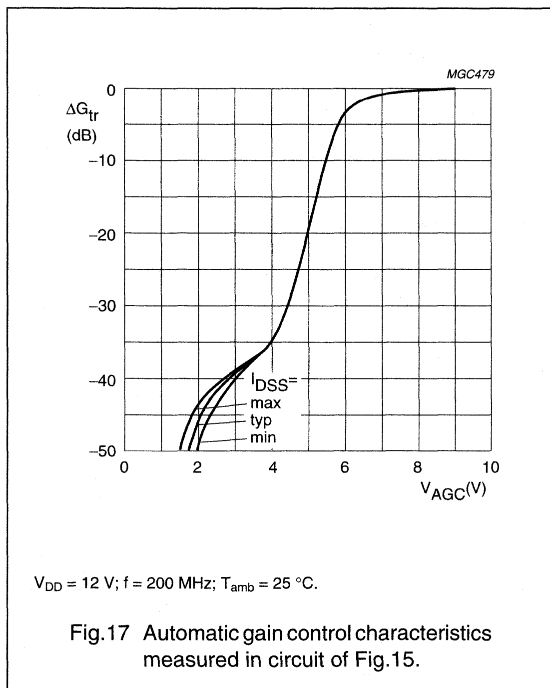
Tapped at approximately half a turn from the cold side, to adjust G_L = 0.5 mS. C1 adjusted for G_S = 2 mS.

Fig.15 Gain control testcircuit at f = 200 MHz.



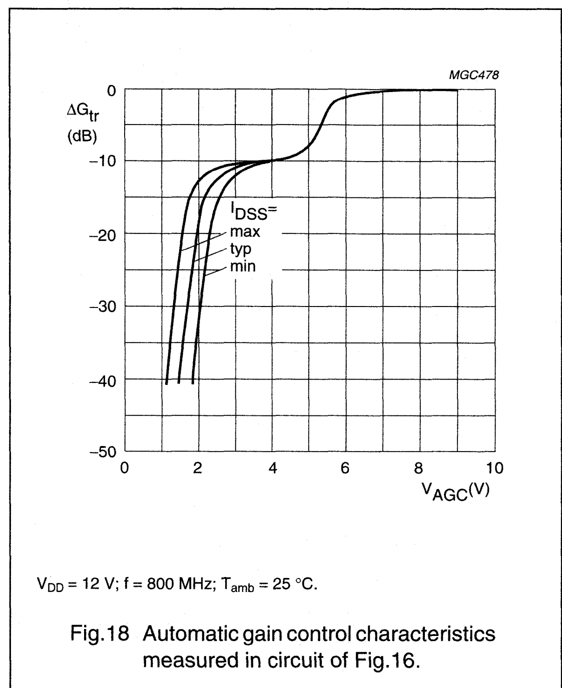
V_{DD} = 12 V; G_S = 3.3 mS; G_L = 1 mS.
L1 = L4 = 200 nH; 11 turns 0.5 mm copper wire, without spacing, internal diameter 3 mm.
L2 = 2 cm, silvered 0.8 mm copper wire, 4 mm above ground plane.
L3 = 2 cm, silvered 0.5 mm copper wire, 4 mm above ground plane.

Fig.16 Gain control test circuit at f = 800 MHz.



V_{DD} = 12 V; f = 200 MHz; T_{amb} = 25 °C.

Fig.17 Automatic gain control characteristics measured in circuit of Fig.15.



V_{DD} = 12 V; f = 800 MHz; T_{amb} = 25 °C.

Fig.18 Automatic gain control characteristics measured in circuit of Fig.16.

Dual-gate MOS-FETs | BF1100; BF1100R

FEATURES

- Specially designed for use at 9 to 12 V supply voltage
- Short channel transistor with high forward transfer admittance to input capacitance ratio
- Low noise gain controlled amplifier up to 1 GHz
- Superior cross-modulation performance during AGC.

APPLICATIONS

- VHF and UHF applications such as television tuners and professional communications equipment.

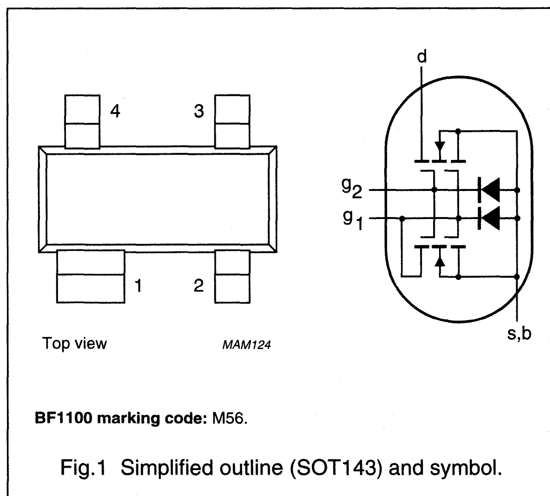
DESCRIPTION

Enhancement type field-effect transistor in a plastic microminiature SOT143 or SOT143R package. The transistor consists of an amplifier MOS-FET with source and substrate interconnected and an internal bias circuit to ensure good cross-modulation performance during AGC.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

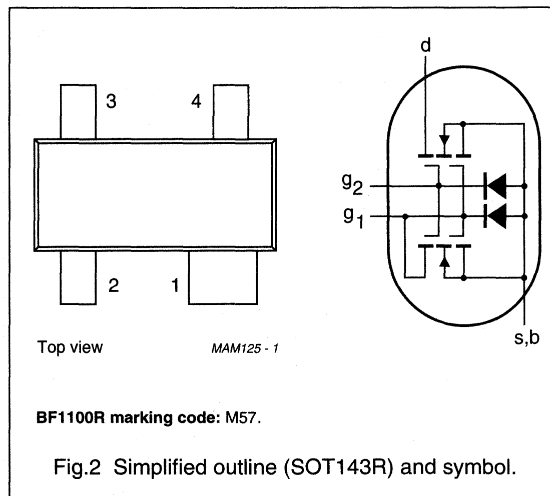
PINNING

PIN	SYMBOL	DESCRIPTION
1	s, b	source
2	d	drain
3	g_2	gate 2
4	g_1	gate 1



BF1100 marking code: M56.

Fig.1 Simplified outline (SOT143) and symbol.



BF1100R marking code: M57.

Fig.2 Simplified outline (SOT143R) and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DS}	drain-source voltage		–	–	14	V
I_D	drain current		–	–	30	mA
P_{tot}	total power dissipation		–	–	200	mW
T_j	operating junction temperature		–	–	150	°C
$\lvert y_{fs} \rvert$	forward transfer admittance		24	28	33	mS
C_{ig1-s}	input capacitance at gate 1		–	2.2	2.6	pF
C_{rs}	reverse transfer capacitance	f = 1 MHz	–	25	35	fF
F	noise figure	f = 800 MHz	–	2	–	dB

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	14	V
I_D	drain current		–	30	mA
I_{G1}	gate 1 current		–	±10	mA
I_{G2}	gate 2 current		–	±10	mA
P_{tot}	total power dissipation	see Fig.3			
	BF1100	up to T_{amb} = 50 °C; note 1	–	200	mW
	BF1100R	up to T_{amb} = 40 °C; note 1	–	200	mW
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–	+150	°C

Note

1. Device mounted on a printed-circuit board.

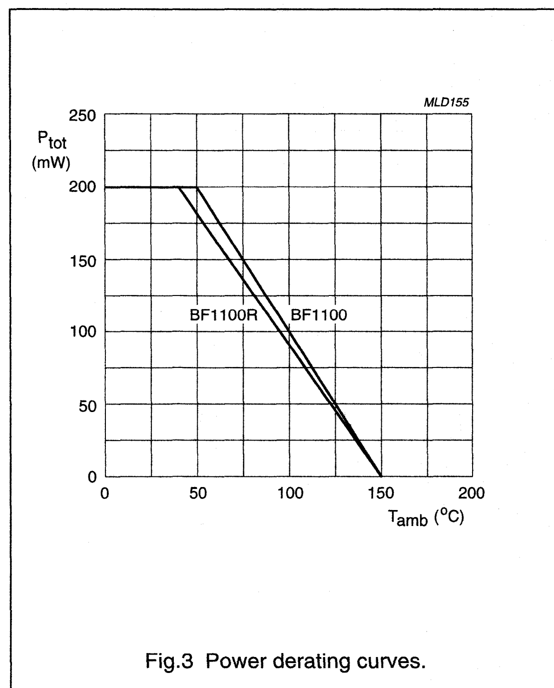


Fig.3 Power derating curves.

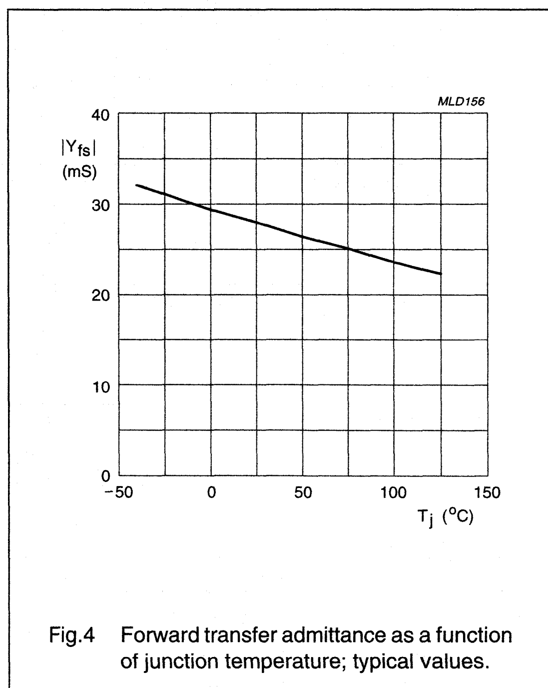


Fig.4 Forward transfer admittance as a function of junction temperature; typical values.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	note 1		
	BF1100		500	K/W
	BF1100R		550	K/W
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	note 2		
	BF1100	T_s = 92 °C	290	K/W
	BF1100R	T_s = 78 °C	360	K/W

Notes

1. Device mounted on a printed-circuit board.
2. T_s is the temperature at the soldering point of the source lead.

STATIC CHARACTERISTICS

T_j = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{(BR)G1\text{-}SS}$	gate 1-source breakdown voltage	$V_{G2\text{-}S} = V_{DS} = 0$; $I_{G1\text{-}S}$ = 1 mA	13.2	20	V
$V_{(BR)G2\text{-}SS}$	gate 2-source breakdown voltage	$V_{G1\text{-}S} = V_{DS} = 0$; $I_{G2\text{-}S}$ = 1 mA	13.2	20	V
$V_{(F)S\text{-}G1}$	forward source-gate 1 voltage	$V_{G2\text{-}S} = V_{DS} = 0$; $I_{S\text{-}G1}$ = 10 mA	0.5	1.5	V
$V_{(F)S\text{-}G2}$	forward source-gate 2 voltage	$V_{G1\text{-}S} = V_{DS} = 0$; $I_{S\text{-}G2}$ = 10 mA	0.5	1.5	V
$V_{G1\text{-}S(th)}$	gate 1-source threshold voltage	$V_{G2\text{-}S}$ = 4 V; V_{DS} = 9 V; I_D = 20 μA	0.3	1	V
		$V_{G2\text{-}S}$ = 4 V; V_{DS} = 12 V; I_D = 20 μA	0.3	1	V
$V_{G2\text{-}S(th)}$	gate 2-source threshold voltage	$V_{G1\text{-}S}$ = 4 V; V_{DS} = 9 V; I_D = 20 μA	0.3	1.2	V
		$V_{G1\text{-}S}$ = 4 V; V_{DS} = 12 V; I_D = 20 μA	0.3	1.2	V
I_{DSX}	drain-source current	$V_{G2\text{-}S}$ = 4 V; V_{DS} = 9 V; R_{G1} = 180 kΩ; note 1	8	13	mA
		$V_{G2\text{-}S}$ = 4 V; V_{DS} = 12 V; R_{G1} = 250 kΩ; note 2	8	13	mA
$I_{G1\text{-}SS}$	gate 1 cut-off current	$V_{G2\text{-}S} = V_{DS} = 0$; $V_{G1\text{-}S}$ = 12 V	–	50	nA
$I_{G2\text{-}SS}$	gate 2 cut-off current	$V_{G1\text{-}S} = V_{DS} = 0$; $V_{G2\text{-}S}$ = 12 V	–	50	nA

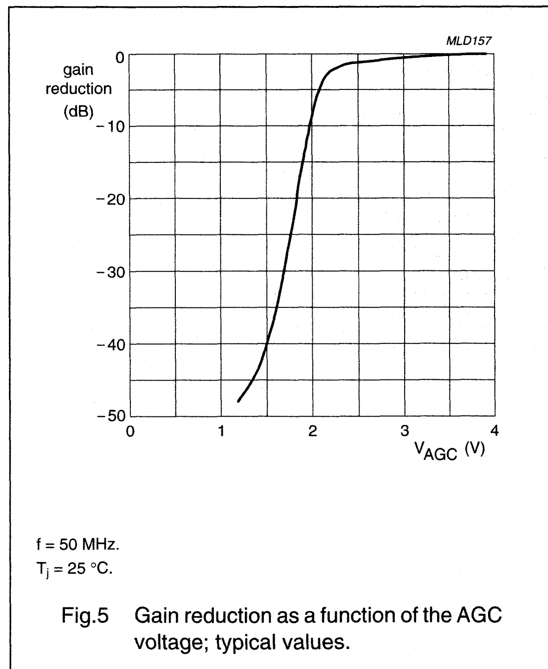
Notes

1. R_{G1} connects gate 1 to V_{GG} = 9 V; see Fig.27.
2. R_{G1} connects gate 1 to V_{GG} = 12 V; see Fig.27.

DYNAMIC CHARACTERISTICS

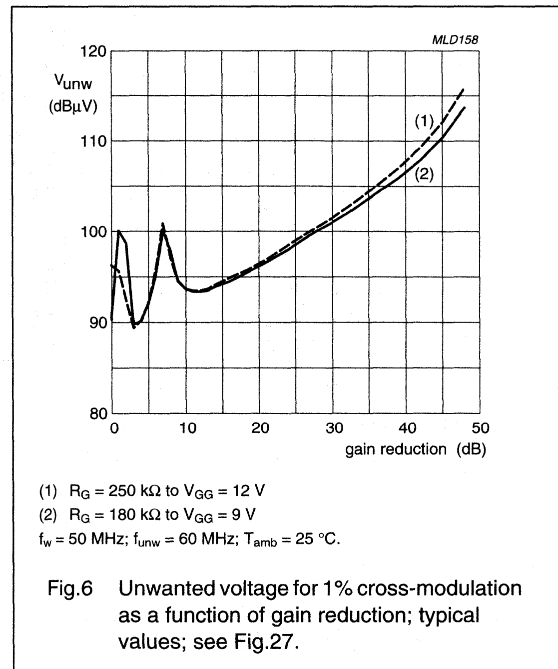
Common source; T_{amb} = 25 °C; V_{G2-S} = 4 V; I_D = 10 mA; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\lvert y_{fs} \rvert$	forward transfer admittance	pulsed; T_j = 25 °C				
		V_{DS} = 9 V	24	28	33	mS
		V_{DS} = 12 V	24	28	33	mS
C_{ig1-s}	input capacitance at gate 1	f = 1 MHz				
		V_{DS} = 9 V	–	2.2	2.6	pF
		V_{DS} = 12 V	–	2.2	2.6	pF
C_{ig2-s}	input capacitance at gate 2	f = 1 MHz				
		V_{DS} = 9 V	–	1.6	–	pF
		V_{DS} = 12 V	–	1.4	–	pF
C_{os}	drain-source capacitance	f = 1 MHz				
		V_{DS} = 9 V	–	1.4	1.8	pF
		V_{DS} = 12 V	–	1.1	1.5	pF
C_{rs}	reverse transfer capacitance	f = 1 MHz				
		V_{DS} = 9 V	–	25	35	fF
		V_{DS} = 12 V	–	25	35	fF
F	noise figure	f = 800 MHz; $G_S = G_{Sopt}$; $B_S = B_{Sopt}$				
		V_{DS} = 9 V	–	2	2.8	dB
		V_{DS} = 12 V	–	2	2.8	dB



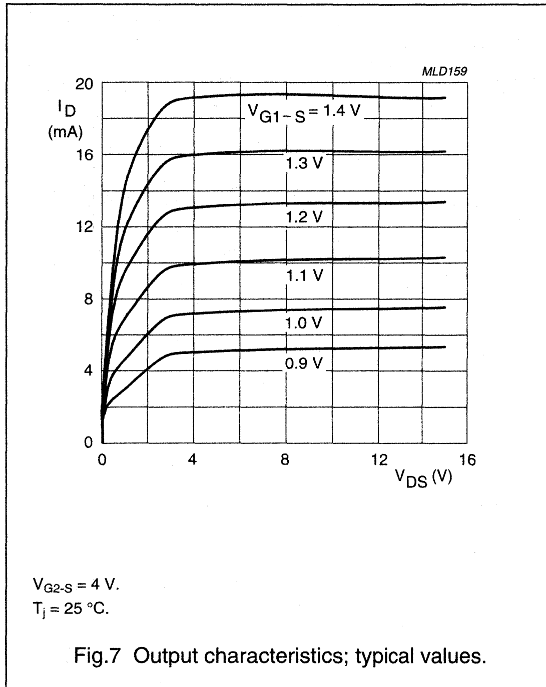
f = 50 MHz.
T_j = 25 °C.

Fig.5 Gain reduction as a function of the AGC voltage; typical values.



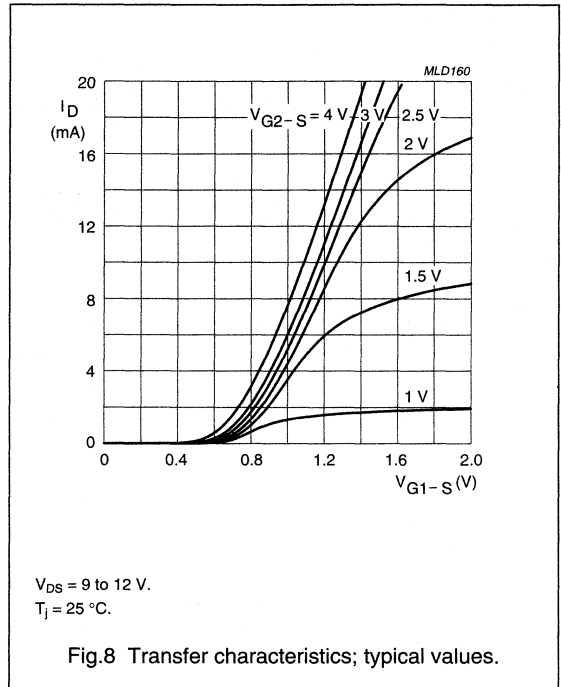
(1) R_G = 250 kΩ to V_{GG} = 12 V
(2) R_G = 180 kΩ to V_{GG} = 9 V
f_w = 50 MHz; f_{unw} = 60 MHz; T_{amb} = 25 °C.

Fig.6 Unwanted voltage for 1% cross-modulation as a function of gain reduction; typical values; see Fig.27.



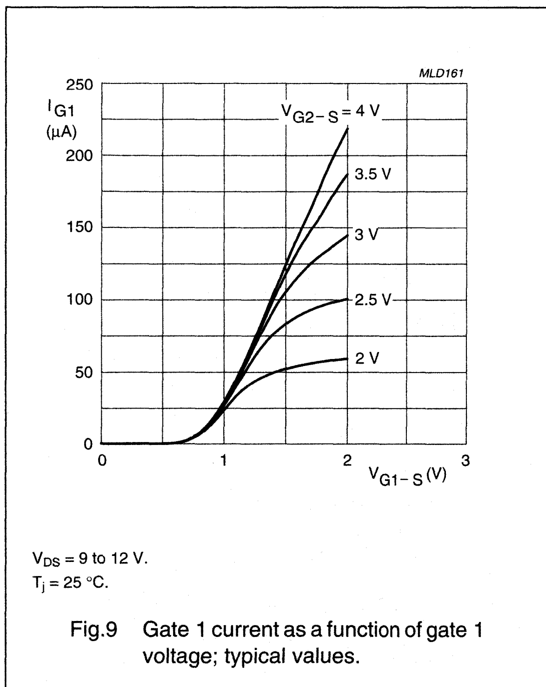
V_{G2-S} = 4 V.
T_j = 25 °C.

Fig.7 Output characteristics; typical values.



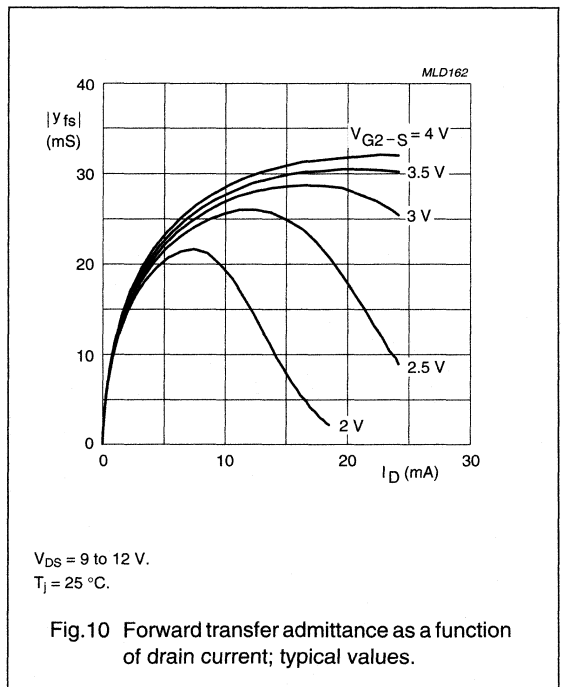
V_{DS} = 9 to 12 V.
T_j = 25 °C.

Fig.8 Transfer characteristics; typical values.



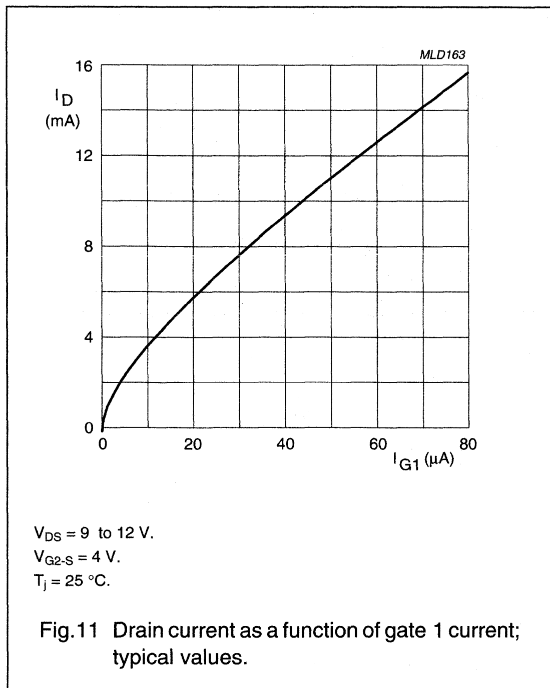
V_{DS} = 9 to 12 V.
T_j = 25 °C.

Fig.9 Gate 1 current as a function of gate 1 voltage; typical values.



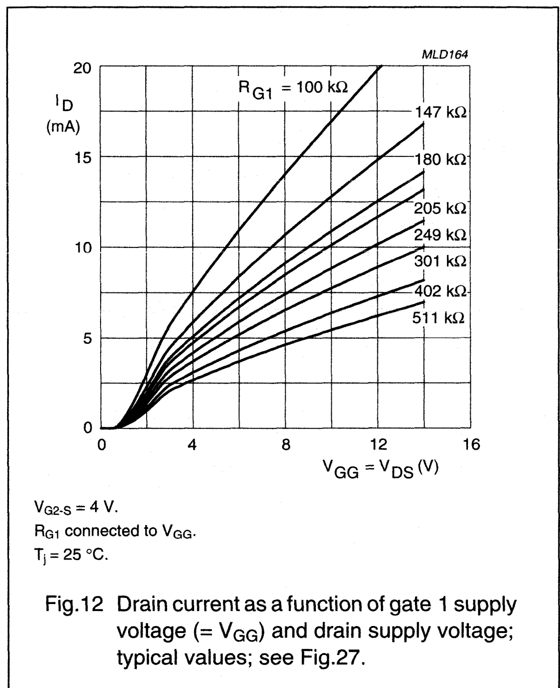
V_{DS} = 9 to 12 V.
T_j = 25 °C.

Fig.10 Forward transfer admittance as a function of drain current; typical values.



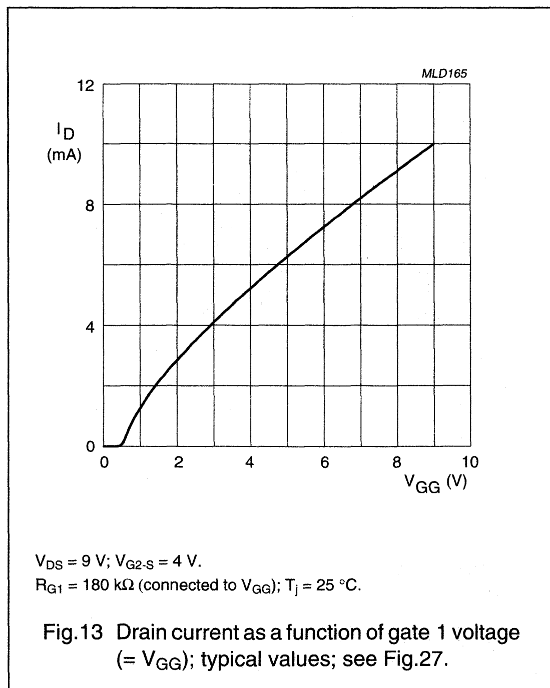
V_{DS} = 9 to 12 V.
V_{G2-S} = 4 V.
T_j = 25 °C.

Fig.11 Drain current as a function of gate 1 current; typical values.



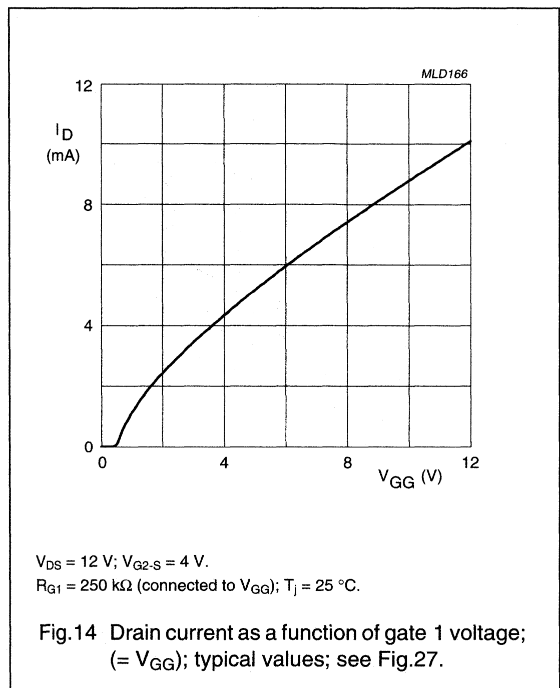
V_{G2-S} = 4 V.
R_{G1} connected to V_{GG}.
T_j = 25 °C.

Fig.12 Drain current as a function of gate 1 supply voltage (= V_{GG}) and drain supply voltage; typical values; see Fig.27.



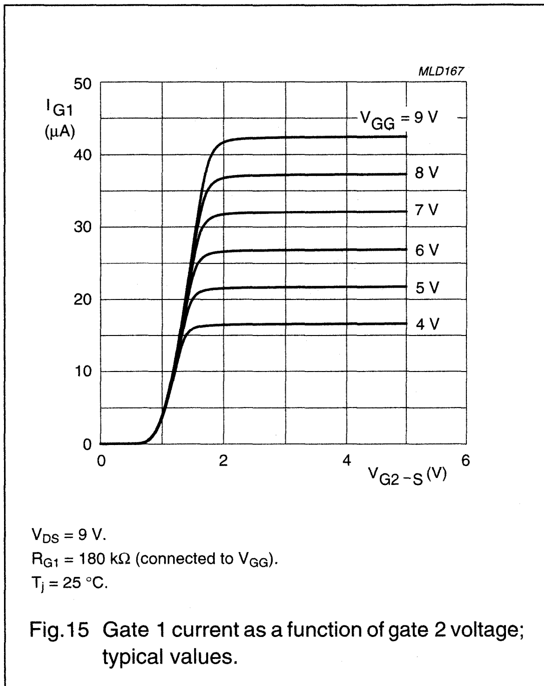
V_{DS} = 9 V; V_{G2-S} = 4 V.
R_{G1} = 180 kΩ (connected to V_{GG}); T_j = 25 °C.

Fig.13 Drain current as a function of gate 1 voltage (= V_{GG}); typical values; see Fig.27.



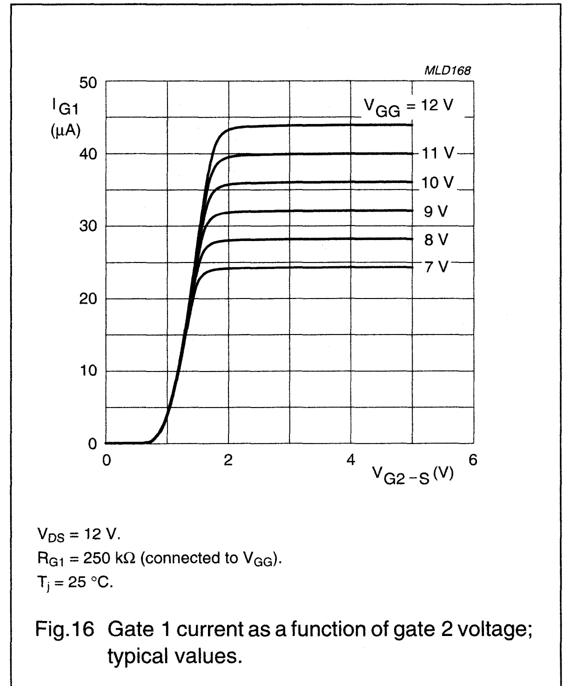
V_{DS} = 12 V; V_{G2-S} = 4 V.
R_{G1} = 250 kΩ (connected to V_{GG}); T_j = 25 °C.

Fig.14 Drain current as a function of gate 1 voltage; (= V_{GG}); typical values; see Fig.27.



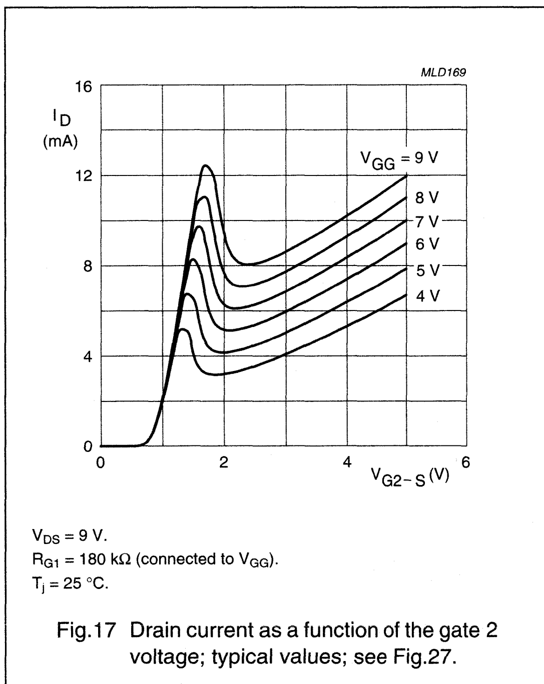
V_{DS} = 9 V.
R_{G1} = 180 kΩ (connected to V_{GG}).
T_j = 25 °C.

Fig.15 Gate 1 current as a function of gate 2 voltage; typical values.



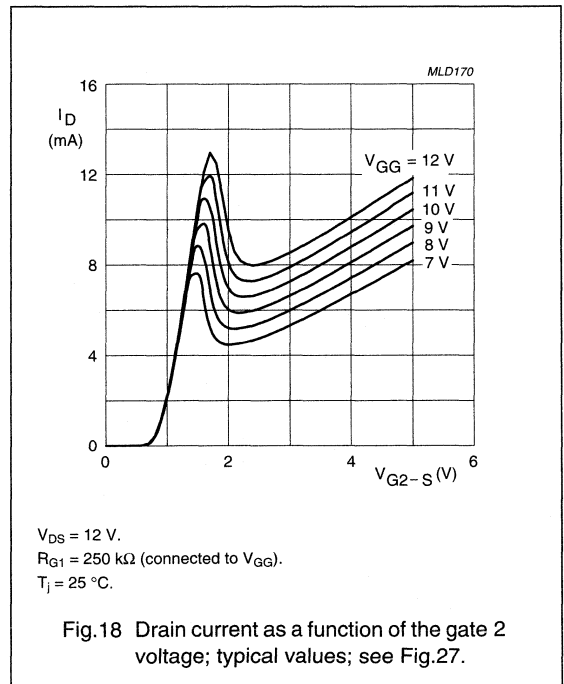
V_{DS} = 12 V.
R_{G1} = 250 kΩ (connected to V_{GG}).
T_j = 25 °C.

Fig.16 Gate 1 current as a function of gate 2 voltage; typical values.



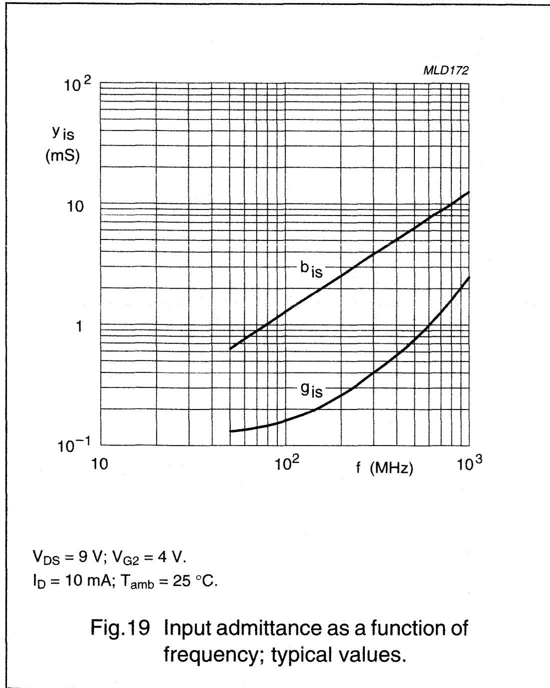
V_{DS} = 9 V.
R_{G1} = 180 kΩ (connected to V_{GG}).
T_j = 25 °C.

Fig.17 Drain current as a function of the gate 2 voltage; typical values; see Fig.27.



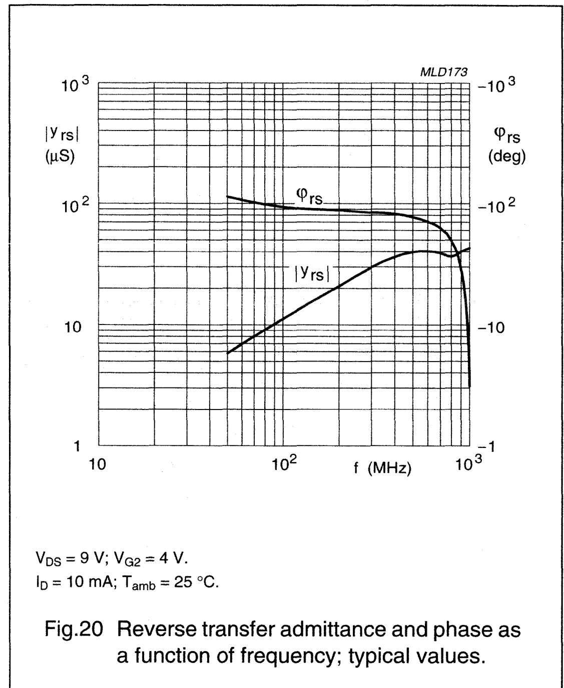
V_{DS} = 12 V.
R_{G1} = 250 kΩ (connected to V_{GG}).
T_j = 25 °C.

Fig.18 Drain current as a function of the gate 2 voltage; typical values; see Fig.27.



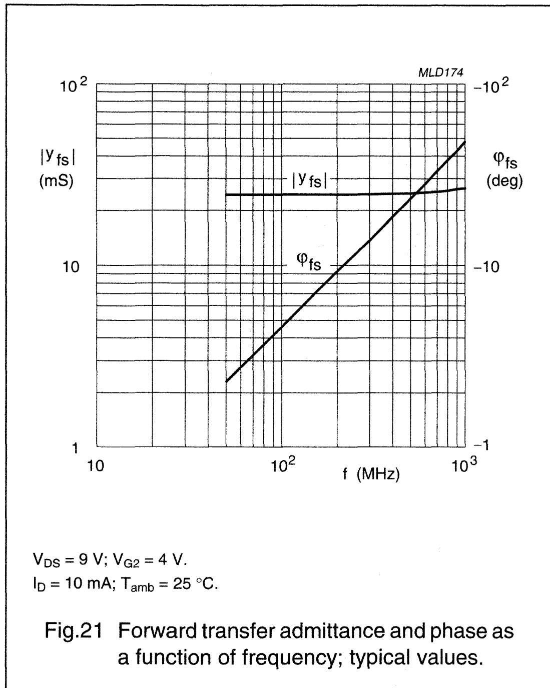
V_{DS} = 9 V; V_{G2} = 4 V.
I_D = 10 mA; T_{amb} = 25 °C.

Fig.19 Input admittance as a function of frequency; typical values.



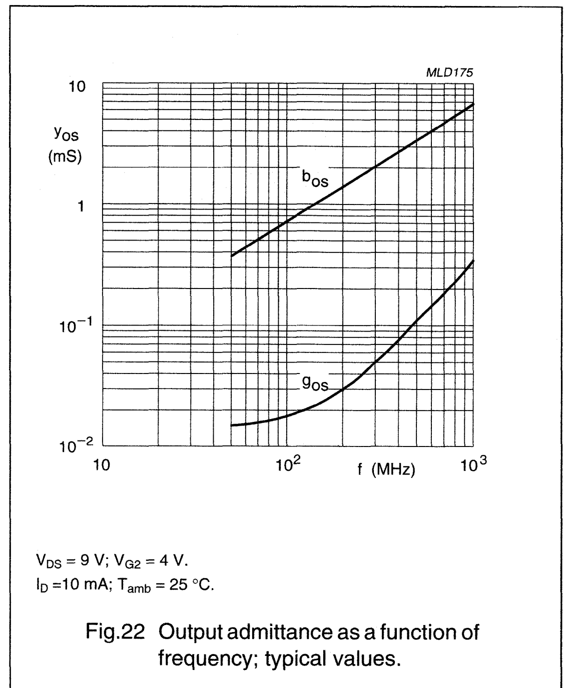
V_{DS} = 9 V; V_{G2} = 4 V.
I_D = 10 mA; T_{amb} = 25 °C.

Fig.20 Reverse transfer admittance and phase as a function of frequency; typical values.



V_{DS} = 9 V; V_{G2} = 4 V.
I_D = 10 mA; T_{amb} = 25 °C.

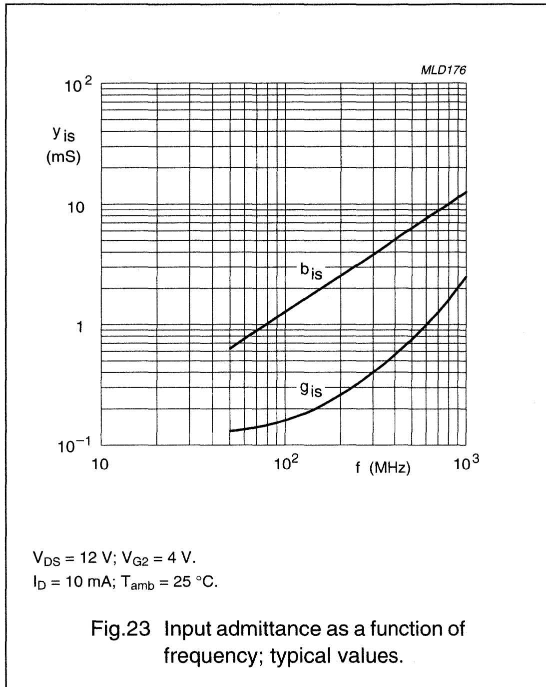
Fig.21 Forward transfer admittance and phase as a function of frequency; typical values.



V_{DS} = 9 V; V_{G2} = 4 V.
I_D =10 mA; T_{amb} = 25 °C.

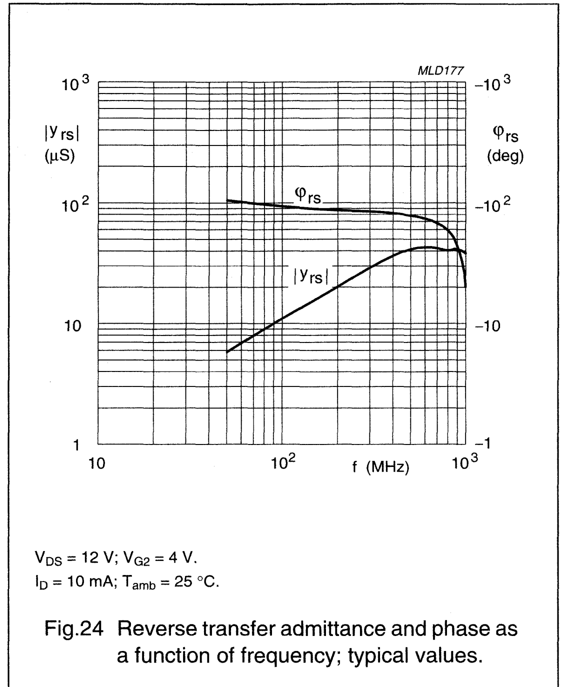
Fig.22 Output admittance as a function of frequency; typical values.

Dual-gate MOS-FETs BF1100; BF1100R



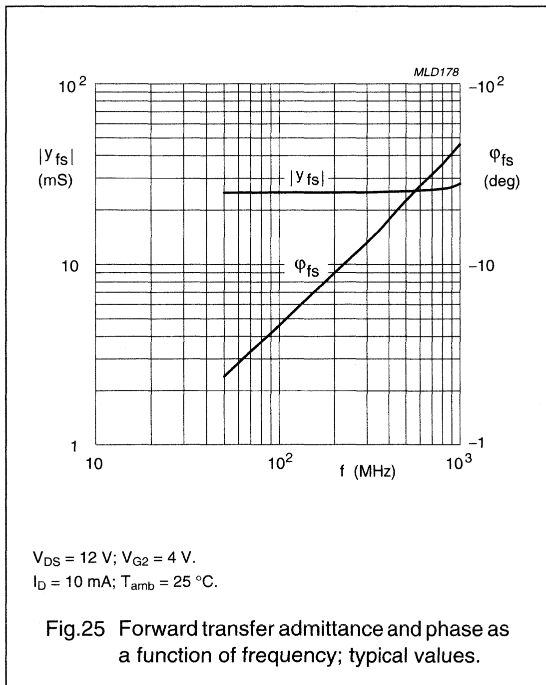
V_{DS} = 12 V; V_{G2} = 4 V.
I_D = 10 mA; T_{amb} = 25 °C.

Fig.23 Input admittance as a function of frequency; typical values.



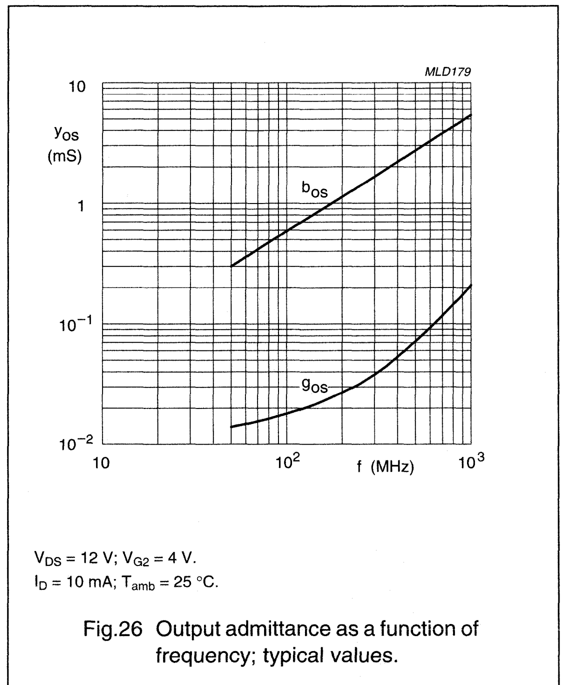
V_{DS} = 12 V; V_{G2} = 4 V.
I_D = 10 mA; T_{amb} = 25 °C.

Fig.24 Reverse transfer admittance and phase as a function of frequency; typical values.



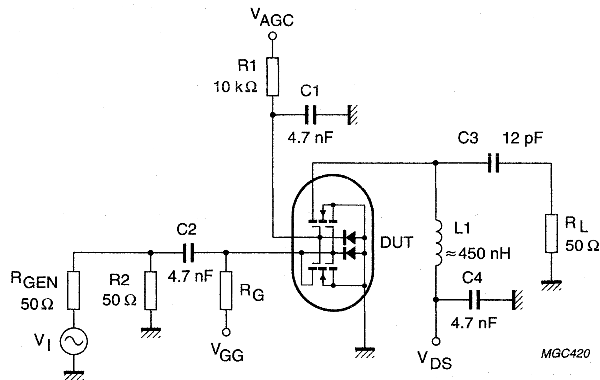
V_{DS} = 12 V; V_{G2} = 4 V.
I_D = 10 mA; T_{amb} = 25 °C.

Fig.25 Forward transfer admittance and phase as a function of frequency; typical values.



V_{DS} = 12 V; V_{G2} = 4 V.
I_D = 10 mA; T_{amb} = 25 °C.

Fig.26 Output admittance as a function of frequency; typical values.



For $V_{GG} = V_{DS} = 9$ V, $R_G = 180$ kΩ.
For $V_{GG} = V_{DS} = 12$ V, $R_G = 250$ kΩ.

Fig.27 Cross-modulation test set-up.

Table 1 Scattering parameters: V_{DS} = 9 V; $V_{G2\text{-}S}$ = 4 V; I_D = 10 mA

f (MHz)	s_{11}		s_{21}		s_{12}		s_{22}	
	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)
50	0.986	−3.6	2.528	174.4	0.001	63.7	1.000	−2.0
100	0.983	−7.4	2.531	169.8	0.001	80.7	1.000	−4.2
200	0.974	−14.7	2.490	159.5	0.002	81.0	0.996	−8.1
300	0.960	−21.8	2.446	149.8	0.002	80.3	0.994	−11.9
400	0.953	−28.7	2.412	139.8	0.003	76.3	0.992	−15.7
500	0.933	−35.4	2.341	130.1	0.003	76.5	0.987	−19.4
600	0.915	−42.0	2.283	120.4	0.004	79.0	0.984	−23.0
700	0.895	−47.9	2.205	111.6	0.003	81.5	0.981	−26.7
800	0.880	−53.5	2.146	102.9	0.003	90.8	0.978	−30.3
900	0.864	−59.6	2.087	93.4	0.003	106.6	0.974	−33.9
1000	0.839	−65.0	1.998	84.4	0.003	135.4	0.971	−37.6

Table 2 Noise data: V_{DS} = 9 V; $V_{G2\text{-}S}$ = 4 V; I_D = 10 mA

f (MHz)	F_{min} (dB)	Γ_{opt}		r_n
		(ratio)	(deg)	
800	2.00	0.67	43.9	0.89

Table 3 Scattering parameters: V_{DS} = 12 V; $V_{G2\text{-}S}$ = 4 V; I_D = 10 mA

f (MHz)	s_{11}		s_{21}		s_{12}		s_{22}	
	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)
50	0.986	−3.7	2.478	174.7	0.001	72.2	1.000	−1.6
100	0.984	−7.4	2.480	170.3	0.001	80.9	1.000	−3.5
200	0.974	−14.6	2.440	160.6	0.002	82.7	0.997	−6.6
300	0.960	−21.8	2.400	151.4	0.002	79.9	0.996	−9.7
400	0.953	−28.7	2.371	141.9	0.003	77.7	0.994	−12.8
500	0.933	−35.3	2.306	132.7	0.003	77.1	0.991	−15.8
600	0.915	−41.9	2.255	123.6	0.004	77.1	0.989	−18.7
700	0.894	−47.8	2.183	115.3	0.004	79.3	0.986	−21.7
800	0.879	−53.5	2.131	107.2	0.003	83.9	0.984	−24.6
900	0.863	−59.5	2.080	98.2	0.003	95.1	0.982	−27.5
1000	0.838	−65.0	1.999	89.7	0.003	115.8	0.980	−30.4

Table 4 Noise data: V_{DS} = 12 V; $V_{G2\text{-}S}$ = 4 V; I_D = 10 mA

f (MHz)	F_{min} (dB)	Γ_{opt}		r_n
		(ratio)	(deg)	
800	2.00	0.66	43.3	0.97

Dual-gate MOS-FET BF1100WR

FEATURES

- Specially designed for use at 9 to 12 V supply voltage
- Short channel transistor with high forward transfer admittance to input capacitance ratio
- Low noise gain controlled amplifier up to 1 GHz
- Superior cross-modulation performance during AGC.

APPLICATIONS

- VHF and UHF applications such as television tuners and professional communications equipment.

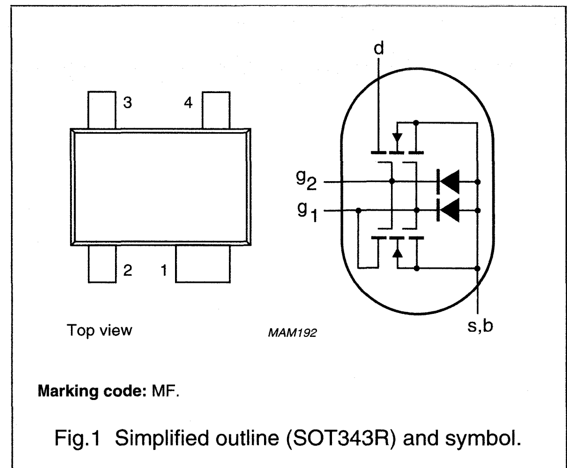
DESCRIPTION

Enhancement type field-effect transistor in a plastic microminiature SOT343R package. The transistor consists of an amplifier MOS-FET with source and substrate interconnected and an internal bias circuit to ensure good cross-modulation performance during AGC.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING

PIN	SYMBOL	DESCRIPTION
1	s, b	source
2	d	drain
3	g_2	gate 2
4	g_1	gate 1



Marking code: MF.

Fig.1 Simplified outline (SOT343R) and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DS}	drain-source voltage		–	–	14	V
I_D	drain current		–	–	30	mA
P_{tot}	total power dissipation		–	–	280	mW
T_j	operating junction temperature		–	–	150	°C
$\lvert y_{fs} \rvert$	forward transfer admittance		24	28	33	mS
C_{ig1-s}	input capacitance at gate 1		–	2.2	2.6	pF
C_{rs}	reverse transfer capacitance	f = 1 MHz	–	25	35	fF
F	noise figure	f = 800 MHz	–	2	–	dB

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	14	V
I_D	drain current		–	30	mA
I_{G1}	gate 1 current		–	±10	mA
I_{G2}	gate 2 current		–	±10	mA
P_{tot}	total power dissipation	see Fig.2; up to T_{amb} = 50 °C; note 1	–	280	mW
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–	+150	°C

Note

1. Device mounted on a printed-circuit board.

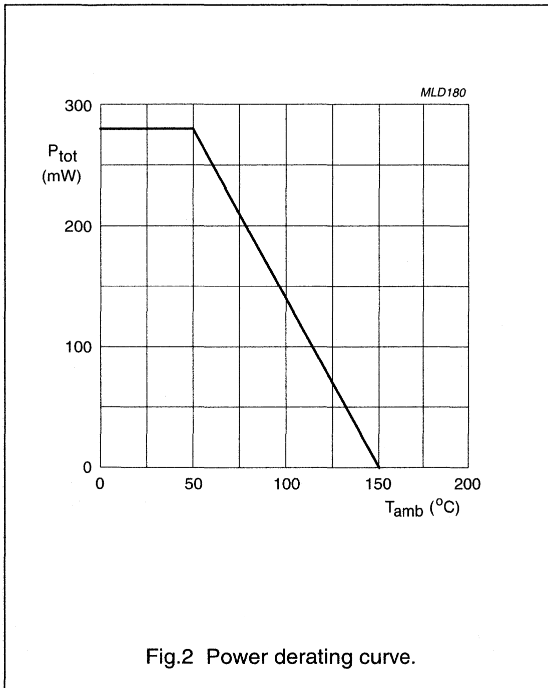


Fig.2 Power derating curve.

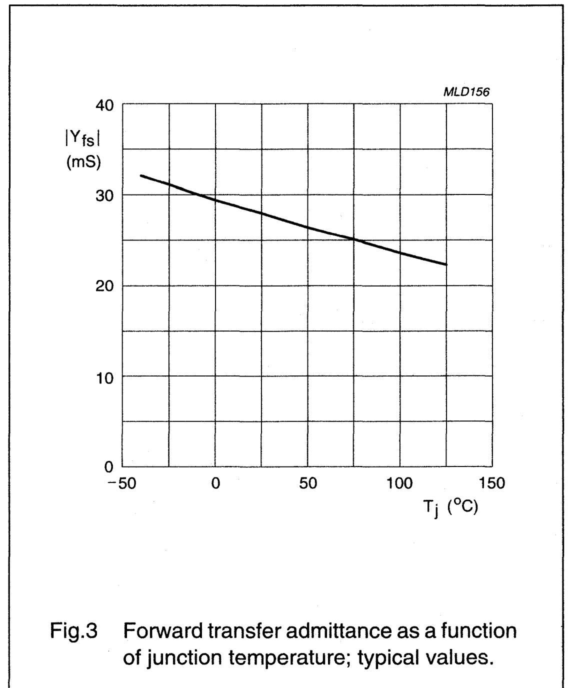


Fig.3 Forward transfer admittance as a function of junction temperature; typical values.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	note 1	350	K/W
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	T_s = 91 °C; note 2	210	K/W

Notes

1. Device mounted on a printed-circuit board.
2. T_s is the temperature at the soldering point of the source lead.

STATIC CHARACTERISTICS

T_j = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{(BR)G1\text{-}SS}$	gate 1-source breakdown voltage	$V_{G2\text{-}S} = V_{DS} = 0$; $I_{G1\text{-}S}$ = 1 mA	13.2	20	V
$V_{(BR)G2\text{-}SS}$	gate 2-source breakdown voltage	$V_{G1\text{-}S} = V_{DS} = 0$; $I_{G2\text{-}S}$ = 1 mA	13.2	20	V
$V_{(F)S\text{-}G1}$	forward source-gate 1 voltage	$V_{G2\text{-}S} = V_{DS} = 0$; $I_{S\text{-}G1}$ = 10 mA	0.5	1.5	V
$V_{(F)S\text{-}G2}$	forward source-gate 2 voltage	$V_{G1\text{-}S} = V_{DS} = 0$; $I_{S\text{-}G2}$ = 10 mA	0.5	1.5	V
$V_{G1\text{-}S(th)}$	gate 1-source threshold voltage	$V_{G2\text{-}S}$ = 4 V; V_{DS} = 9 V; I_D = 20 μA	0.3	1	V
		$V_{G2\text{-}S}$ = 4 V; V_{DS} = 12 V; I_D = 20 μA	0.3	1	V
$V_{G2\text{-}S(th)}$	gate 2-source threshold voltage	$V_{G1\text{-}S}$ = 4 V; V_{DS} = 9 V; I_D = 20 μA	0.3	1.2	V
		$V_{G1\text{-}S}$ = 4 V; V_{DS} = 12 V; I_D = 20 μA	0.3	1.2	V
I_{DSX}	drain-source current	$V_{G2\text{-}S}$ = 4 V; V_{DS} = 9 V; R_{G1} = 180 kΩ; note 1	8	13	mA
		$V_{G2\text{-}S}$ = 4 V; V_{DS} = 12 V; R_{G1} = 250 kΩ; note 2	8	13	mA
$I_{G1\text{-}SS}$	gate 1 cut-off current	$V_{G2\text{-}S} = V_{DS} = 0$; $V_{G1\text{-}S}$ = 12 V	–	50	nA
$I_{G2\text{-}SS}$	gate 2 cut-off current	$V_{G1\text{-}S} = V_{DS} = 0$; $V_{G2\text{-}S}$ = 12 V	–	50	nA

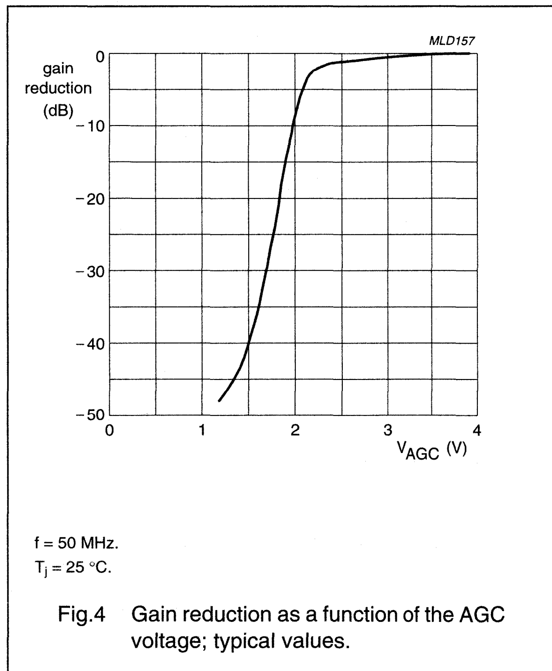
Notes

1. R_{G1} connects gate 1 to V_{GG} = 9 V; see Fig.26.
2. R_{G1} connects gate 1 to V_{GG} = 12 V; see Fig.26.

DYNAMIC CHARACTERISTICS

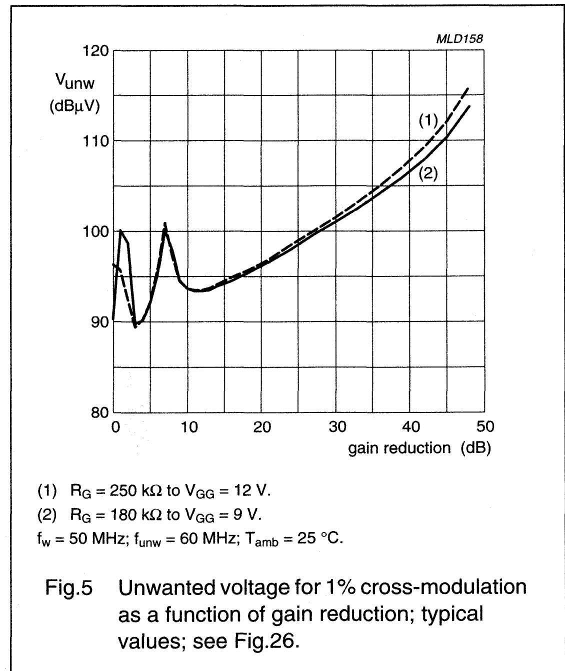
Common source; T_{amb} = 25 °C; V_{G2-S} = 4 V; I_D = 10 mA; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\|y_{fs}\|$	forward transfer admittance	pulsed; T_j = 25 °C				
		V_{DS} = 9 V	24	28	33	mS
		V_{DS} = 12 V	24	28	33	mS
C_{ig1-s}	input capacitance at gate 1	f = 1 MHz				
		V_{DS} = 9 V	–	2.2	2.6	pF
		V_{DS} = 12 V	–	2.2	2.6	pF
C_{ig2-s}	input capacitance at gate 2	f = 1 MHz				
		V_{DS} = 9 V	–	1.6	–	pF
		V_{DS} = 12 V	–	1.4	–	pF
C_{os}	drain-source capacitance	f = 1 MHz				
		V_{DS} = 9 V	–	1.4	1.8	pF
		V_{DS} = 12 V	–	1.1	1.5	pF
C_{rs}	reverse transfer capacitance	f = 1 MHz				
		V_{DS} = 9 V	–	25	35	fF
		V_{DS} = 12 V	–	25	35	fF
F	noise figure	f = 800 MHz; $G_S = G_{Sopt}$; $B_S = B_{Sopt}$				
		V_{DS} = 9 V	–	2	2.8	dB
		V_{DS} = 12 V	–	2	2.8	dB



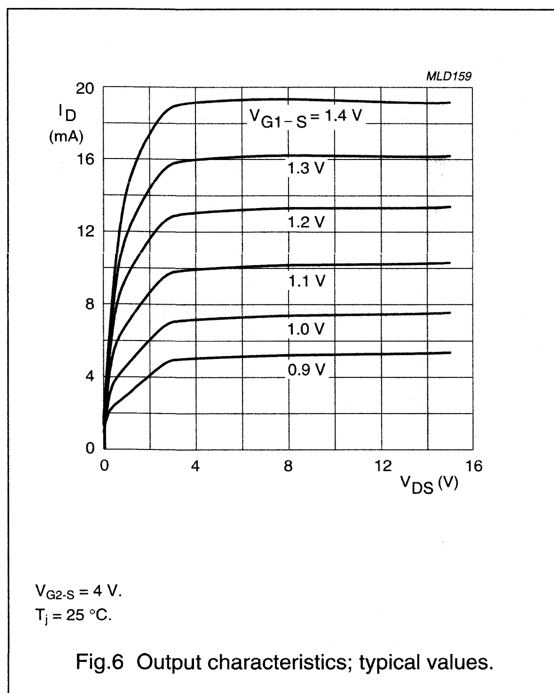
f = 50 MHz.
T_j = 25 °C.

Fig.4 Gain reduction as a function of the AGC voltage; typical values.



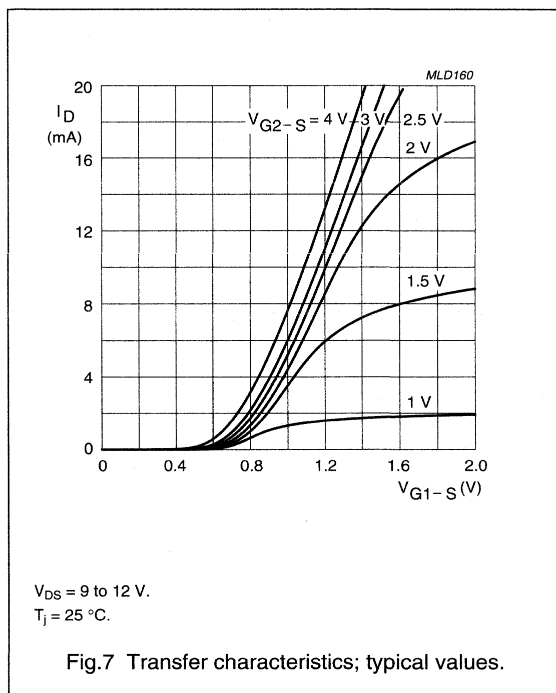
(1) R_G = 250 kΩ to V_{GG} = 12 V.
(2) R_G = 180 kΩ to V_{GG} = 9 V.
f_w = 50 MHz; f_{unw} = 60 MHz; T_{amb} = 25 °C.

Fig.5 Unwanted voltage for 1% cross-modulation as a function of gain reduction; typical values; see Fig.26.



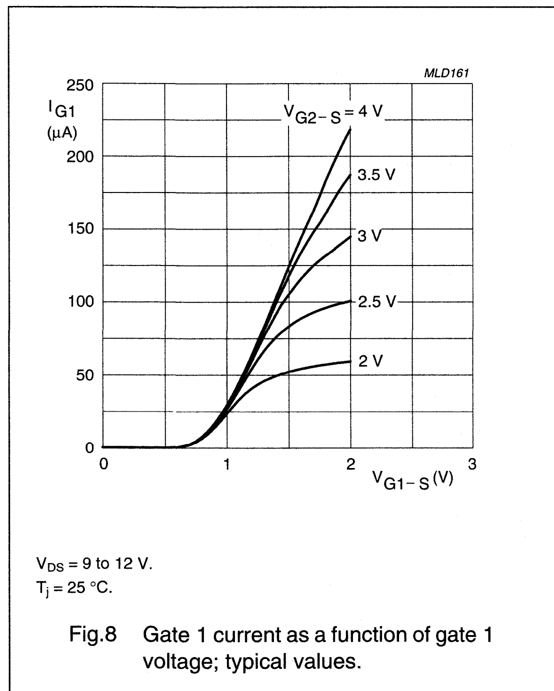
V_{G2-S} = 4 V.
T_j = 25 °C.

Fig.6 Output characteristics; typical values.



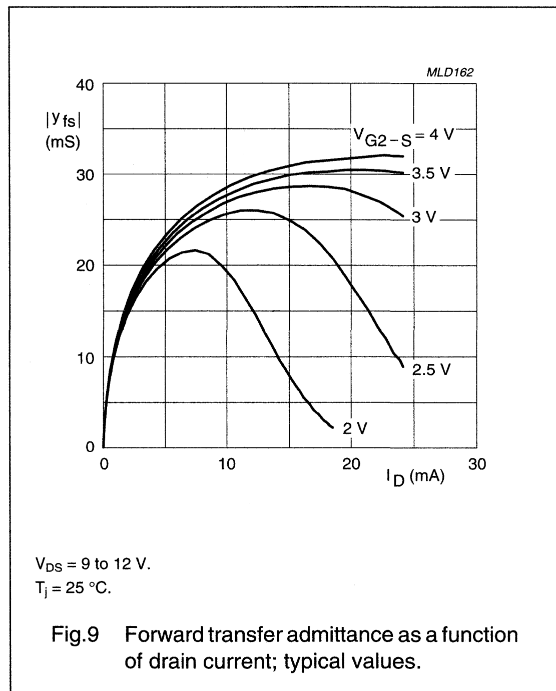
V_{DS} = 9 to 12 V.
T_j = 25 °C.

Fig.7 Transfer characteristics; typical values.



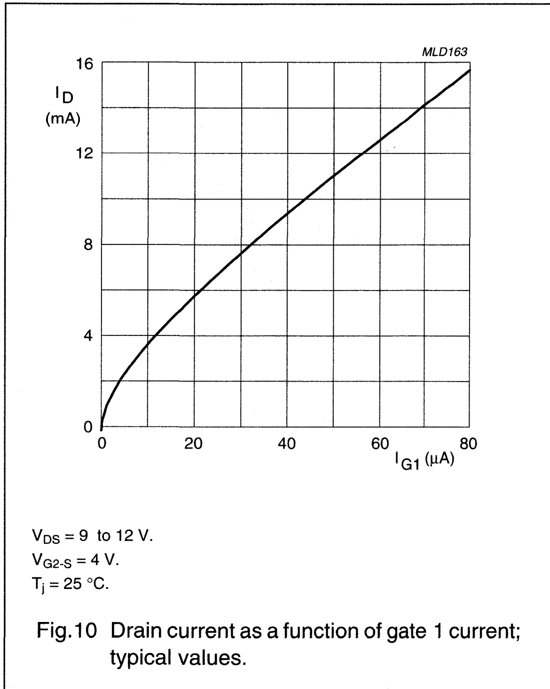
V_{DS} = 9 to 12 V.
T_j = 25 °C.

Fig.8 Gate 1 current as a function of gate 1 voltage; typical values.



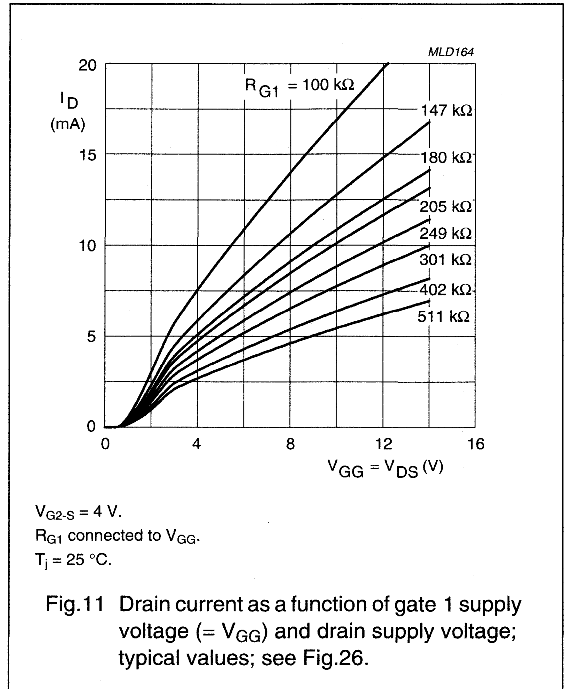
V_{DS} = 9 to 12 V.
T_j = 25 °C.

Fig.9 Forward transfer admittance as a function of drain current; typical values.



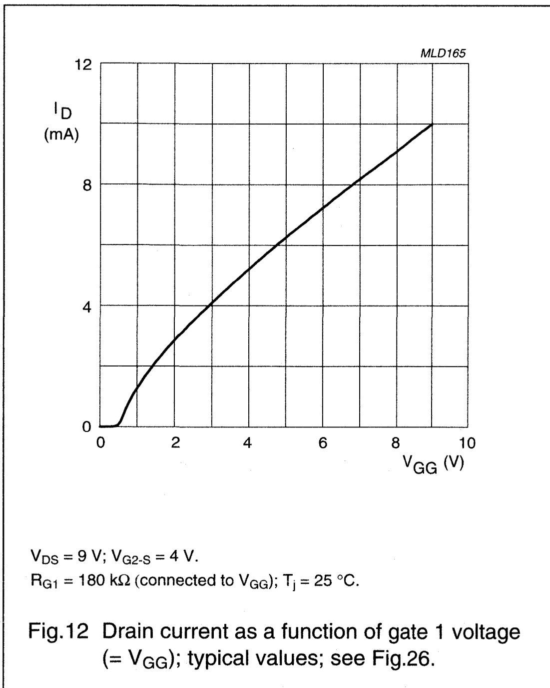
V_{DS} = 9 to 12 V.
V_{G2-S} = 4 V.
T_j = 25 °C.

Fig.10 Drain current as a function of gate 1 current; typical values.



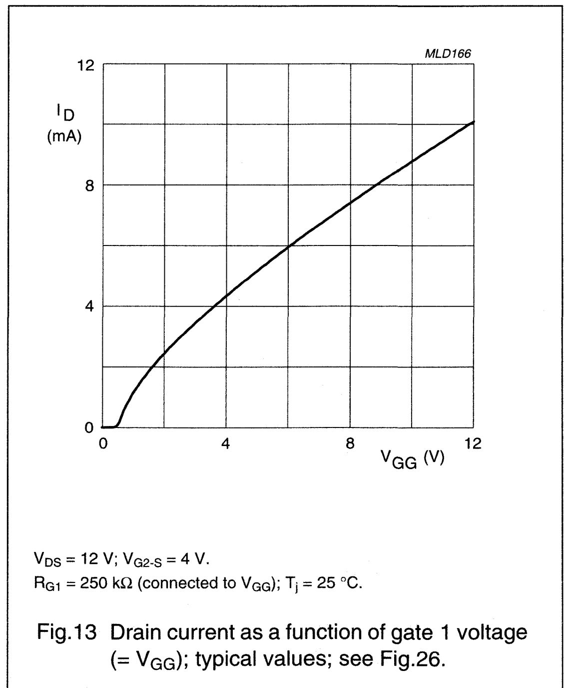
V_{G2-S} = 4 V.
R_{G1} connected to V_{GG}.
T_j = 25 °C.

Fig.11 Drain current as a function of gate 1 supply voltage (= V_{GG}) and drain supply voltage; typical values; see Fig.26.



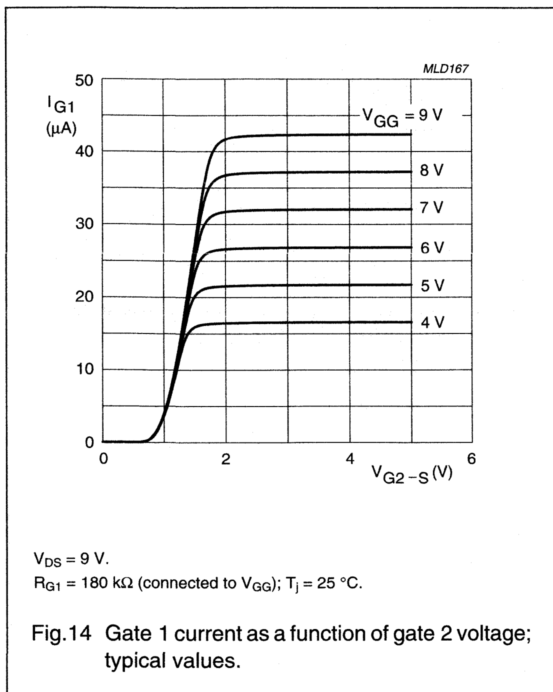
V_{DS} = 9 V; V_{G2-S} = 4 V.
R_{G1} = 180 kΩ (connected to V_{GG}); T_j = 25 °C.

Fig.12 Drain current as a function of gate 1 voltage (= V_{GG}); typical values; see Fig.26.



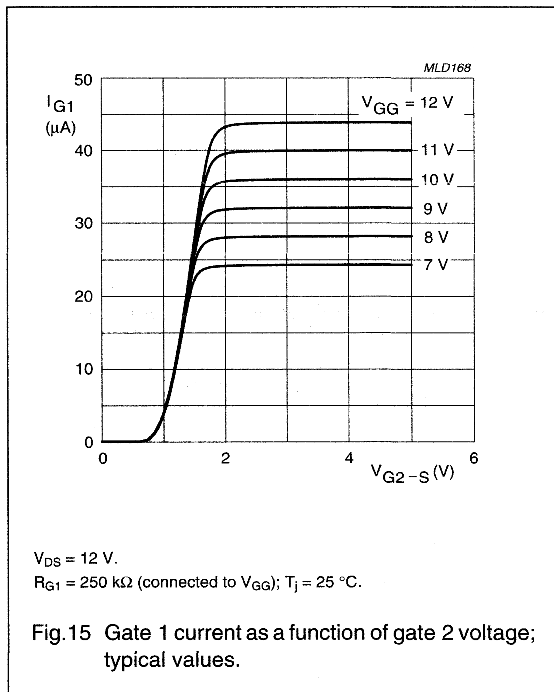
V_{DS} = 12 V; V_{G2-S} = 4 V.
R_{G1} = 250 kΩ (connected to V_{GG}); T_j = 25 °C.

Fig.13 Drain current as a function of gate 1 voltage (= V_{GG}); typical values; see Fig.26.



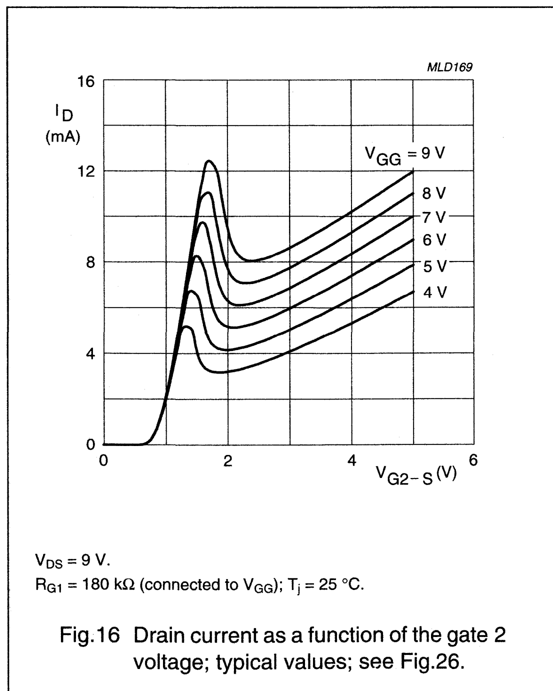
V_{DS} = 9 V.
R_{G1} = 180 kΩ (connected to V_{GG}); T_j = 25 °C.

Fig.14 Gate 1 current as a function of gate 2 voltage; typical values.



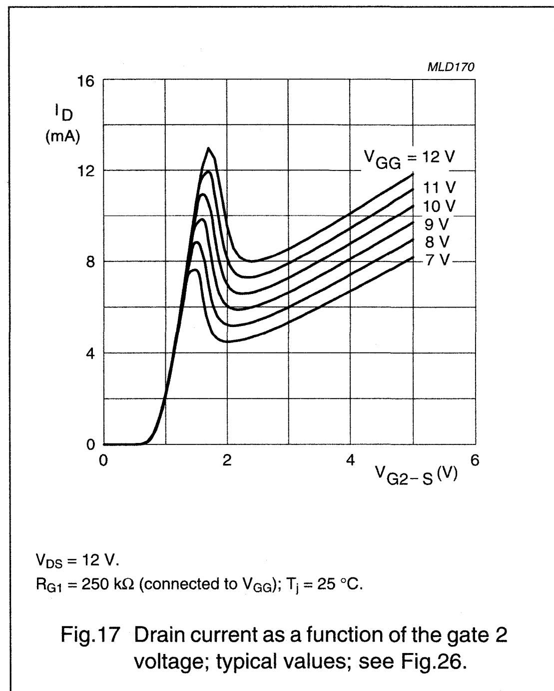
V_{DS} = 12 V.
R_{G1} = 250 kΩ (connected to V_{GG}); T_j = 25 °C.

Fig.15 Gate 1 current as a function of gate 2 voltage; typical values.



V_{DS} = 9 V.
R_{G1} = 180 kΩ (connected to V_{GG}); T_j = 25 °C.

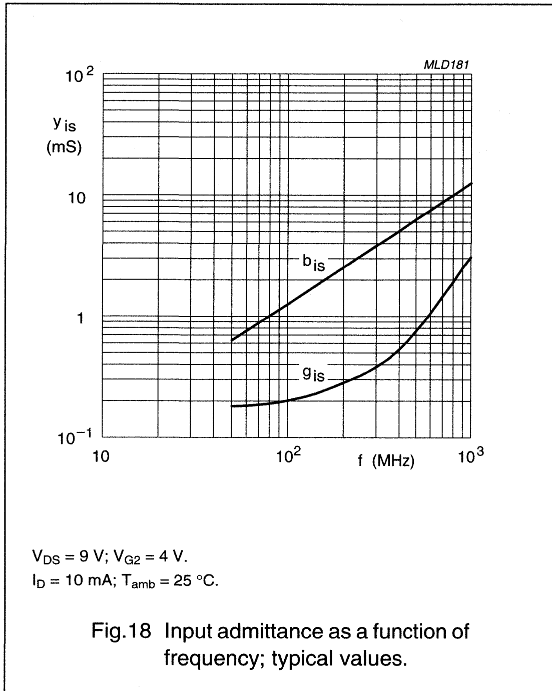
Fig.16 Drain current as a function of the gate 2 voltage; typical values; see Fig.26.



V_{DS} = 12 V.
R_{G1} = 250 kΩ (connected to V_{GG}); T_j = 25 °C.

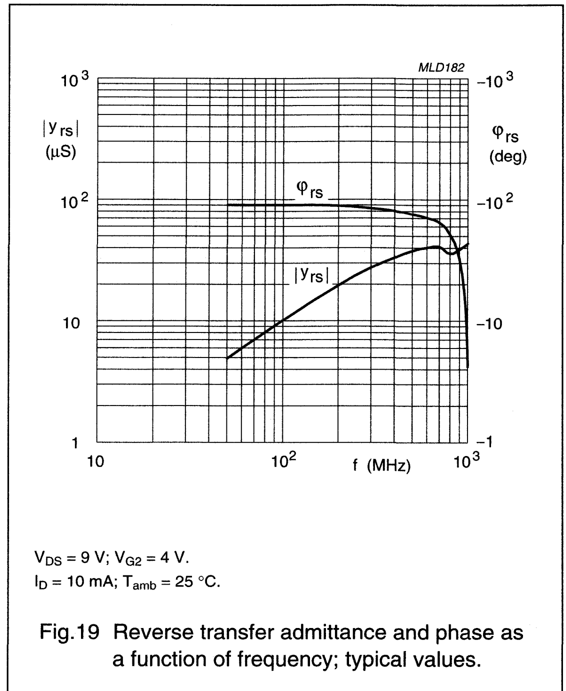
Fig.17 Drain current as a function of the gate 2 voltage; typical values; see Fig.26.

Dual-gate MOS-FET BF1100WR



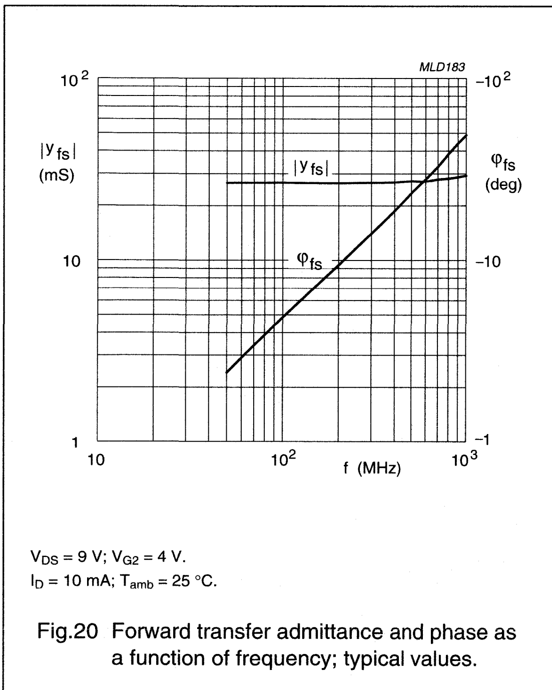
V_{DS} = 9 V; V_{G2} = 4 V.
I_D = 10 mA; T_{amb} = 25 °C.

Fig.18 Input admittance as a function of frequency; typical values.



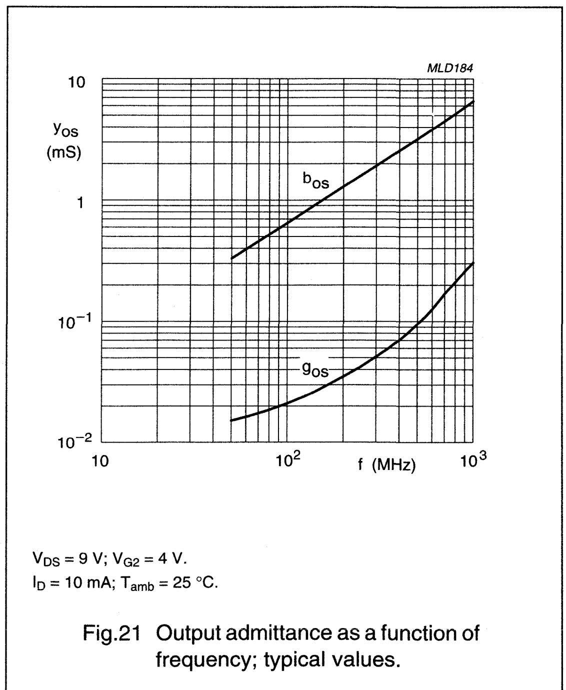
V_{DS} = 9 V; V_{G2} = 4 V.
I_D = 10 mA; T_{amb} = 25 °C.

Fig.19 Reverse transfer admittance and phase as a function of frequency; typical values.



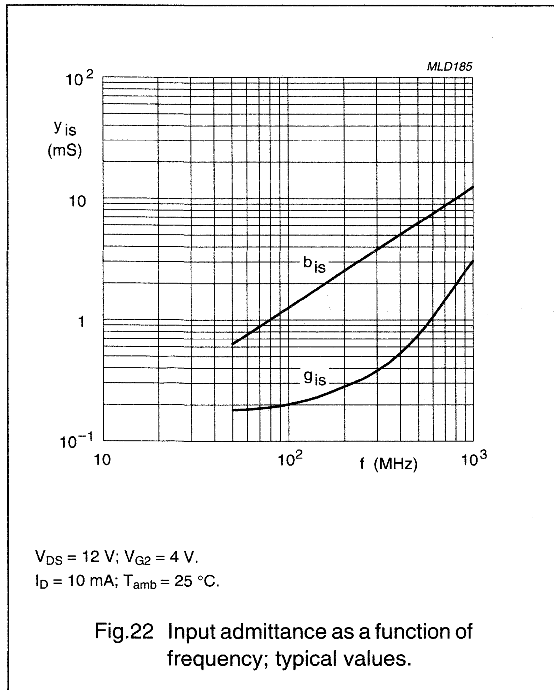
V_{DS} = 9 V; V_{G2} = 4 V.
I_D = 10 mA; T_{amb} = 25 °C.

Fig.20 Forward transfer admittance and phase as a function of frequency; typical values.



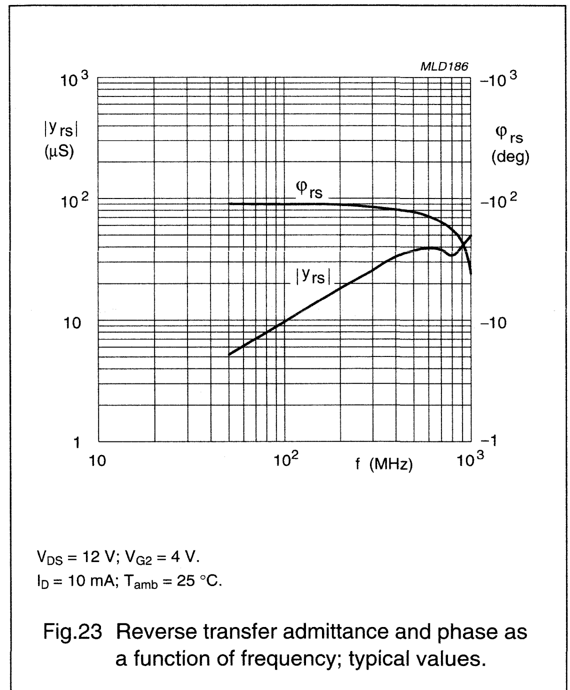
V_{DS} = 9 V; V_{G2} = 4 V.
I_D = 10 mA; T_{amb} = 25 °C.

Fig.21 Output admittance as a function of frequency; typical values.



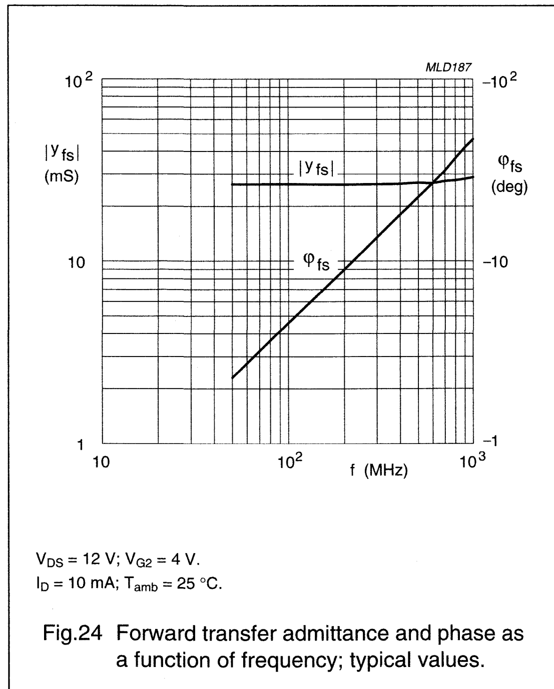
V_{DS} = 12 V; V_{G2} = 4 V.
I_D = 10 mA; T_{amb} = 25 °C.

Fig.22 Input admittance as a function of frequency; typical values.



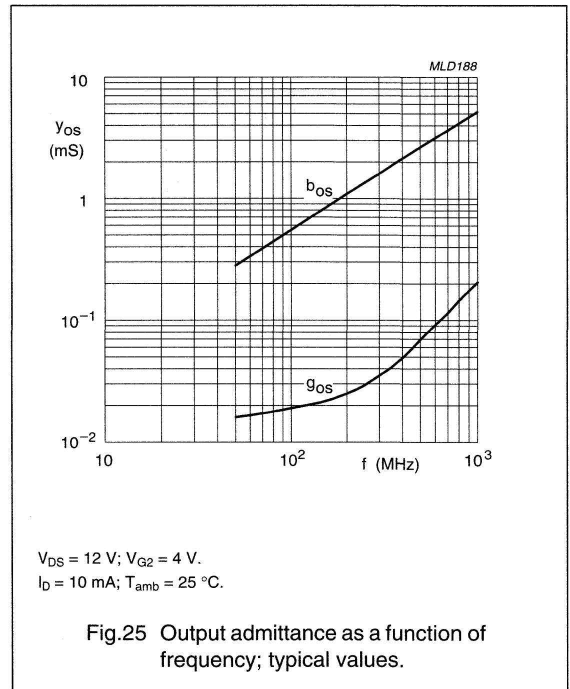
V_{DS} = 12 V; V_{G2} = 4 V.
I_D = 10 mA; T_{amb} = 25 °C.

Fig.23 Reverse transfer admittance and phase as a function of frequency; typical values.



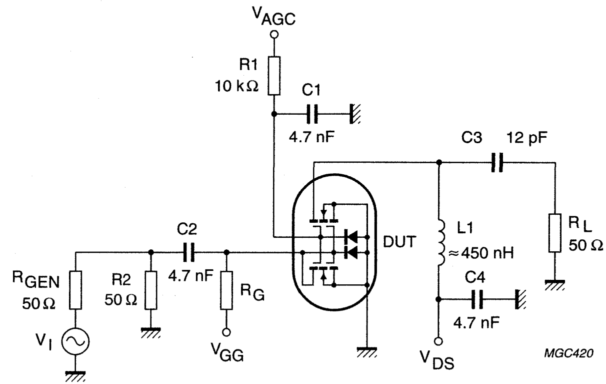
V_{DS} = 12 V; V_{G2} = 4 V.
I_D = 10 mA; T_{amb} = 25 °C.

Fig.24 Forward transfer admittance and phase as a function of frequency; typical values.



V_{DS} = 12 V; V_{G2} = 4 V.
I_D = 10 mA; T_{amb} = 25 °C.

Fig.25 Output admittance as a function of frequency; typical values.



For $V_{GG} = V_{DS} = 9$ V, $R_G = 180$ kΩ.
For $V_{GG} = V_{DS} = 12$ V, $R_G = 250$ kΩ.

Fig.26 Cross-modulation test circuit.

Table 1 Scattering parameters: V_{DS} = 9 V; $V_{G2\text{-}S}$ = 4 V; I_D = 10 mA

f (MHz)	s_{11}		s_{21}		s_{12}		s_{22}	
	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)
50	0.985	−3.9	2.618	175.1	0.001	137.9	1.000	−1.9
100	0.981	−7.3	2.602	170.5	0.001	80.4	0.999	−4.0
200	0.975	−14.4	2.577	160.7	0.002	74.0	0.995	−7.6
300	0.965	−21.6	2.555	151.6	0.002	79.3	0.994	−11.3
400	0.947	−28.3	2.513	141.8	0.003	80.5	0.992	−15.0
500	0.927	−34.9	2.449	133.4	0.003	82.8	0.988	−18.5
600	0.913	−41.7	2.339	124.6	0.003	78.9	0.984	−22.0
700	0.890	−47.9	2.361	115.4	0.003	80.6	0.982	−25.3
800	0.869	−54.0	2.302	106.4	0.003	93.9	0.979	−28.8
900	0.845	−59.7	2.228	97.6	0.003	104.8	0.976	−32.1
1000	0.823	−65.4	2.167	89.6	0.003	129.3	0.974	−35.5

Table 2 Noise data: V_{DS} = 9 V; $V_{G2\text{-}S}$ = 4 V; I_D = 10 mA

f (MHz)	F_{min} (dB)	Γ_{opt}		r_n
		(ratio)	(deg)	
800	2.00	0.67	43.9	0.89

Table 3 Scattering parameters: V_{DS} = 12 V; $V_{G2\text{-}S}$ = 4 V; I_D = 10 mA

f (MHz)	s_{11}		s_{21}		s_{12}		s_{22}	
	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)
50	0.985	−3.7	2.576	175.3	0.000	125.0	1.000	−1.6
100	0.980	−7.4	2.563	170.9	0.001	111.2	1.000	−3.3
200	0.973	−14.6	2.541	161.6	0.002	83.0	0.997	−6.4
300	0.962	−21.5	2.519	152.9	0.002	85.2	0.996	−9.3
400	0.946	−28.5	2.479	143.5	0.003	79.4	0.995	−12.4
500	0.929	−35.0	2.419	135.5	0.003	78.2	0.991	−15.3
600	0.912	−41.6	2.373	127.2	0.003	80.0	0.989	−18.1
700	0.895	−47.8	2.336	118.7	0.003	83.4	0.987	−20.9
800	0.868	−53.8	2.284	110.0	0.003	91.3	0.985	−23.7
900	0.845	−59.8	2.213	101.6	0.003	95.9	0.983	−26.5
1000	0.823	−65.7	2.160	94.1	0.003	112.2	0.981	−29.3

Table 4 Noise data: V_{DS} = 12 V; $V_{G2\text{-}S}$ = 4 V; I_D = 10 mA

f (MHz)	F_{min} (dB)	Γ_{opt}		r_n
		(ratio)	(deg)	
800	2.00	0.66	43.3	0.97

N-channel dual-gate MOS-FETs BF1105; BF1105R; BF1105WR

FEATURES

- Short channel transistor with high forward transfer admittance to input capacitance ratio
- Low noise gain controlled amplifier up to 1 GHz.
- Internal self-biasing circuit to ensure good cross-modulation performance during AGC and good DC stabilization.

APPLICATIONS

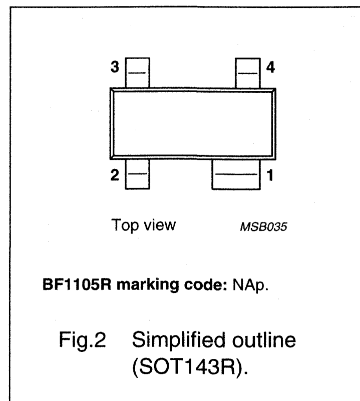
- VHF and UHF applications with 5 V supply voltage, such as television tuners and professional communications equipment.

DESCRIPTION

Enhancement type N-channel field-effect transistor with source and substrate interconnected. Integrated diodes between gates and source protect against excessive input voltage surges. The BF1105, BF1105R and BF1105WR are encapsulated in the SOT143B, SOT143R and SOT343R plastic packages respectively.

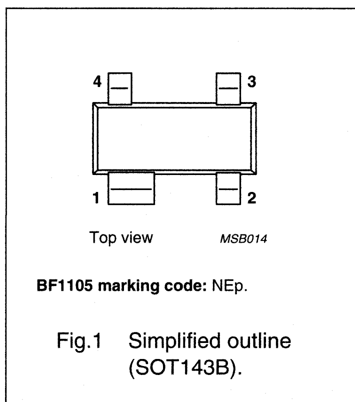
PINNING

PIN	DESCRIPTION
1	source
2	drain
3	gate 2
4	gate 1



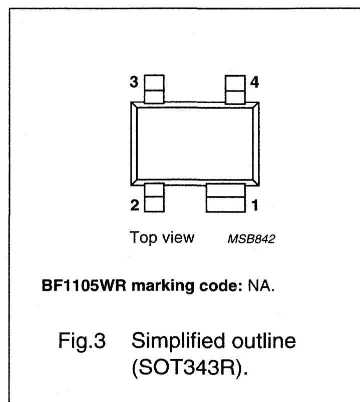
BF1105R marking code: NAp.

Fig.2 Simplified outline (SOT143R).



BF1105 marking code: NEp.

Fig.1 Simplified outline (SOT143B).



BF1105WR marking code: NA.

Fig.3 Simplified outline (SOT343R).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DS}	drain-source voltage		–	–	7	V
I_D	drain current		–	–	30	mA
P_{tot}	total power dissipation	$T_{amb} \leq 80$ °C	–	–	200	mW
$\|y_{fs}\|$	forward transfer admittance		25	31	–	mS
$C_{ig1\text{-}ss}$	input capacitance at gate 1		–	2.2	2.7	pF
C_{rss}	reverse transfer capacitance	f = 1 MHz	–	25	40	fF
F	noise figure	f = 800 MHz	–	1.7	2.5	dB
X_{mod}	cross-modulation	input level for k = 1% at 40 dB AGC	100	–	–	dBμV
T_j	operating junction temperature		–	–	150	°C

CAUTION
This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling. For further information, refer to Philips specs.: SNW-EQ-608, SNW-FQ-302A and SNW-FQ-302B.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	7	V
I_D	drain current		–	30	mA
I_{G1}	gate 1 current		–	±10	mA
I_{G2}	gate 2 current		–	±10	mA
P_{tot}	total power dissipation	$T_{amb} \leq 80$ °C; note 1; see Fig.4	–	200	mW
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–	+150	°C

Note

1. Device mounted on a printed-circuit board.

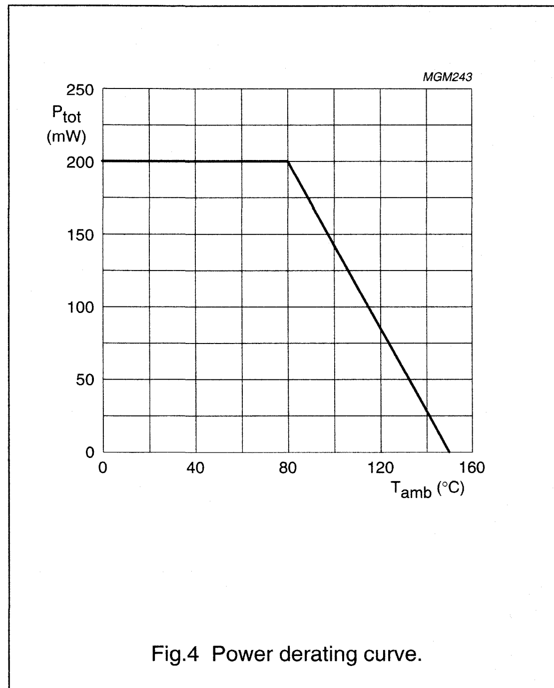


Fig.4 Power derating curve.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	note 1	350	K/W
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point		200	K/W

Note

1. Device mounted on a printed-circuit board.

STATIC CHARACTERISTICS

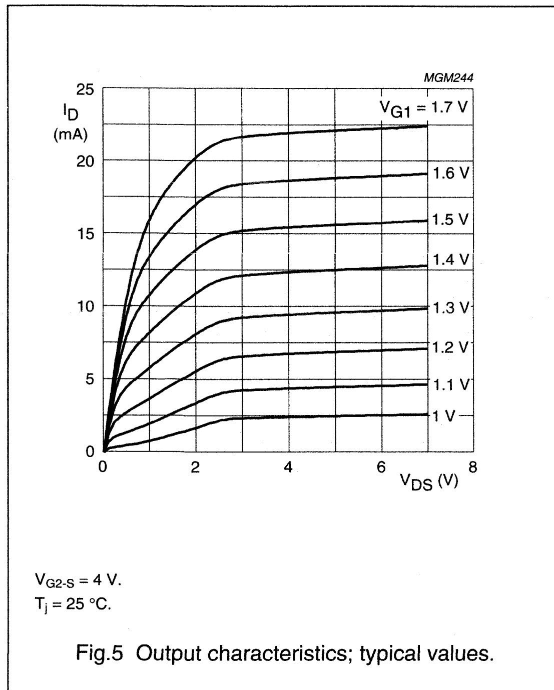
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{G1\text{-}S} = V_{G2\text{-}S} = 0$; $I_D = 10\ \mu A$	7	–	–	V
$V_{(BR)G1\text{-}SS}$	gate 1-source breakdown voltage	$V_{G2\text{-}S} = 0$; $I_D = 0$; $I_{G1\text{-}S} = 10\ \mu A$	7	–	–	V
$V_{(BR)G2\text{-}SS}$	gate 2-source breakdown voltage	$V_{G1\text{-}S} = V_{DS} = 0$; $I_{G2\text{-}S} = 10\ \mu A$	7	–	–	V
$V_{G2\text{-}S\ (th)}$	gate 2-source threshold voltage	$V_{G1\text{-}S} = 5$ V; $V_{DS} = 5$ V; $I_D = 20\ \mu A$	0.3	0.8	1.2	V
I_{DSX}	self-biasing drain current	$V_{G2\text{-}S} = 4$ V; $V_{DS} = 5$ V	8	–	16	mA
$I_{G1\text{-}SS}$	gate 1 cut-off current	$V_{G1\text{-}S} = 5$ V; $V_{G2\text{-}S} = 0$; $I_D = 0$	–	–	50	nA
$I_{G2\text{-}SS}$	gate 2 cut-off current	$V_{G1\text{-}S} = V_{DS} = 0$; $V_{G2\text{-}S} = 4$ V	–	–	20	nA

DYNAMIC CHARACTERISTICS

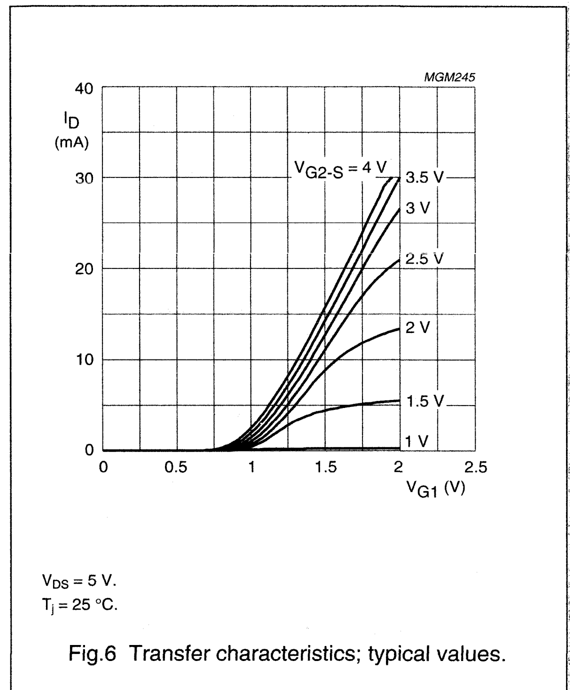
Common source; T_{amb} = 25 °C; $V_{G2\text{-}S}$ = 4 V; V_{DS} = 5 V; self-biasing current; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\lvert y_{fs} \rvert$	forward transfer admittance	pulsed; T_j = 25 °C	25	31	–	mS
$C_{ig1\text{-}ss}$	input capacitance at gate 1	f = 1 MHz	–	2.2	2.7	pF
$C_{ig2\text{-}ss}$	input capacitance at gate 2	f = 1 MHz	–	1.6	–	pF
C_{oss}	output capacitance	f = 1 MHz	–	1.2	–	pF
C_{rss}	reverse transfer capacitance	f = 1 MHz	–	25	40	fF
F	noise figure	f = 800 MHz; $Y_S = Y_{S\ opt}$	–	1.7	2.5	dB
G_p	power gain	G_S = 2 mS; $B_S = B_{S\ opt}$; G_L = 0.5 mS; $B_L = B_{L\ opt}$; f = 200 MHz; see Fig.16	–	38	–	dB
		G_S = 3.3 mS; $B_S = B_{S\ opt}$; G_L = 1 mS; $B_L = B_{L\ opt}$; f = 800 MHz; see Fig.17	–	20	–	dB
X_{mod}	cross-modulation	input level for k = 1% at 0 dB AGC; f_w = 50 MHz; f_{unw} = 60 MHz; see Fig.18	85	–	–	dBμV
		input level for k = 1% at 40 dB AGC; f_w = 50 MHz; f_{unw} = 60 MHz; see Fig.18	100	–	–	dBμV



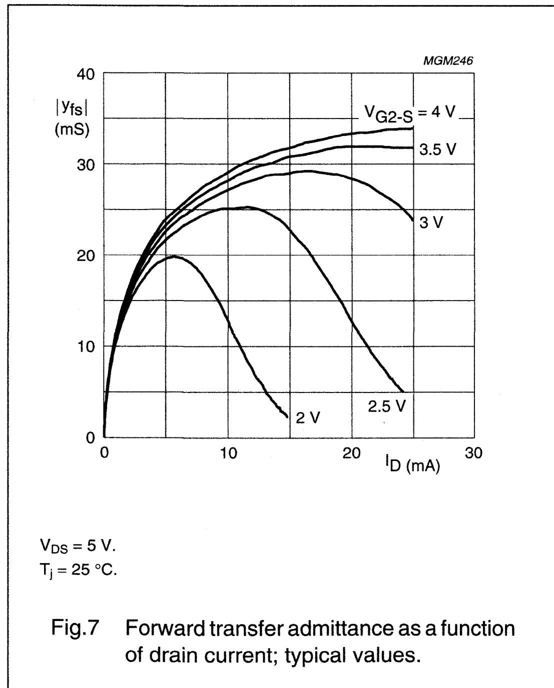
V_{G2-S} = 4 V.
T_j = 25 °C.

Fig.5 Output characteristics; typical values.



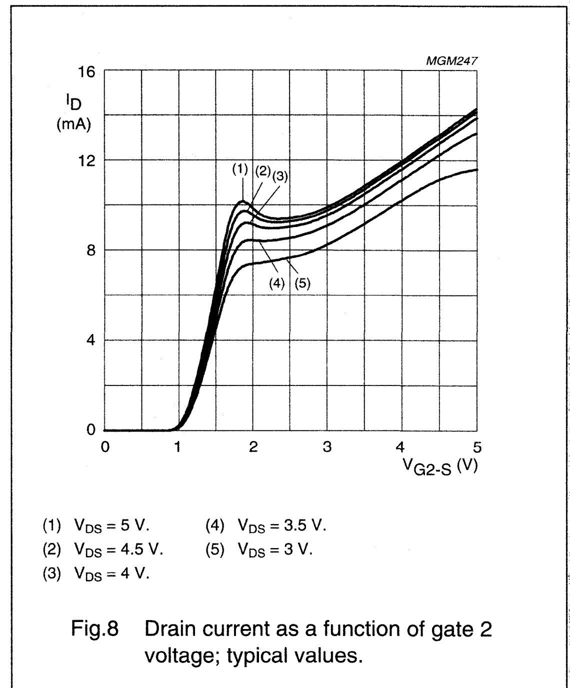
V_{DS} = 5 V.
T_j = 25 °C.

Fig.6 Transfer characteristics; typical values.



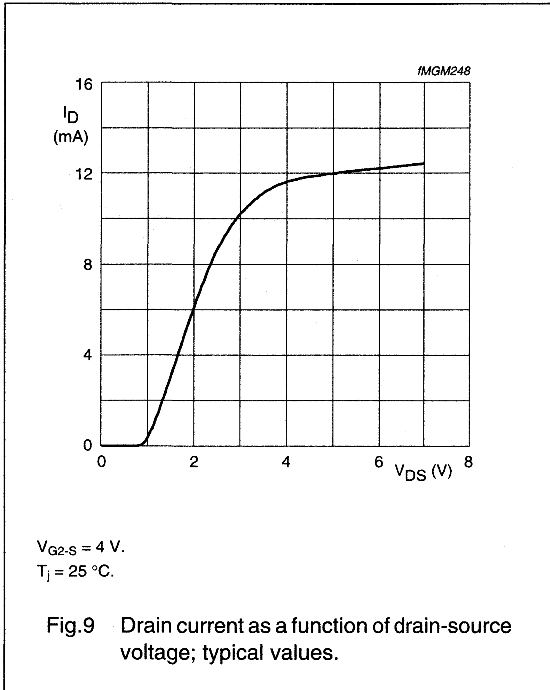
V_{DS} = 5 V.
T_j = 25 °C.

Fig.7 Forward transfer admittance as a function of drain current; typical values.



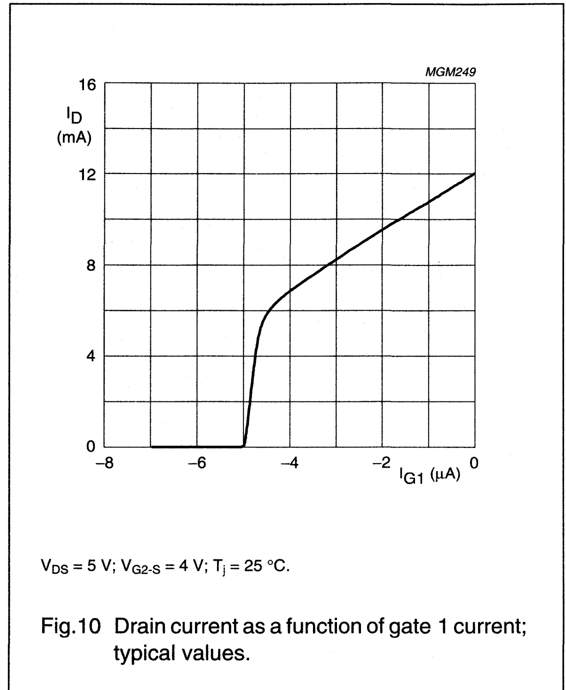
(1) V_{DS} = 5 V.
(2) V_{DS} = 4.5 V.
(3) V_{DS} = 4 V.
(4) V_{DS} = 3.5 V.
(5) V_{DS} = 3 V.

Fig.8 Drain current as a function of gate 2 voltage; typical values.



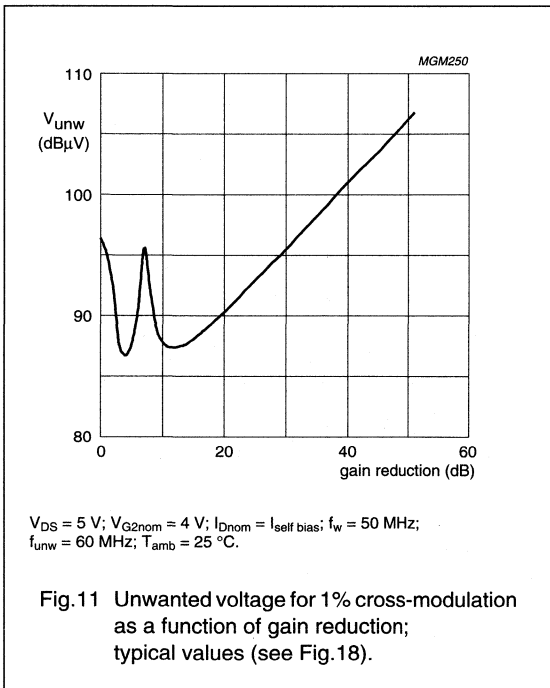
$V_{G2\text{-}S} = 4$ V.
$T_j = 25$ °C.

Fig.9 Drain current as a function of drain-source voltage; typical values.



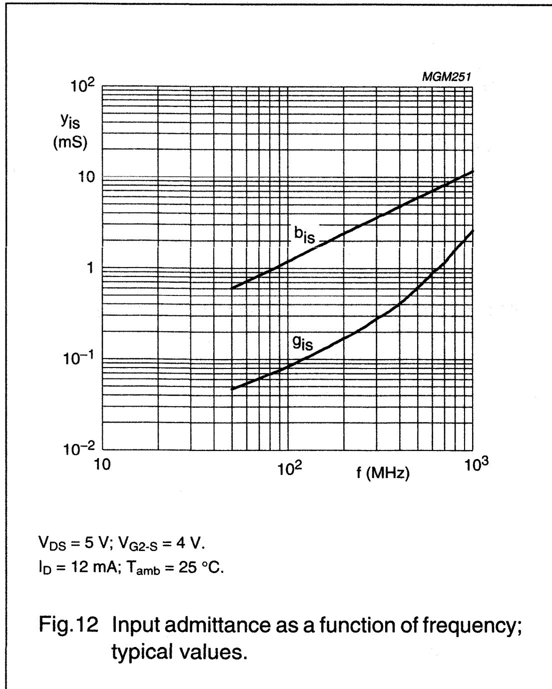
$V_{DS} = 5$ V; $V_{G2\text{-}S} = 4$ V; $T_j = 25$ °C.

Fig.10 Drain current as a function of gate 1 current; typical values.



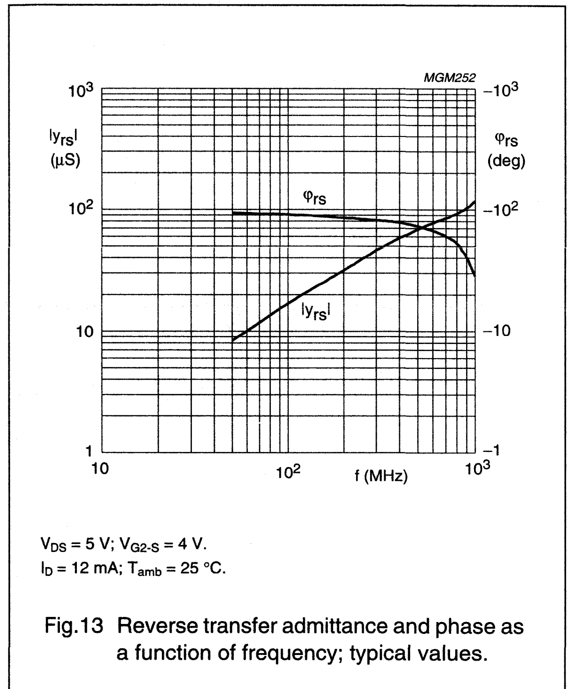
$V_{DS} = 5$ V; $V_{G2nom} = 4$ V; $I_{Dnom} = I_{self\ bias}$; $f_w = 50$ MHz; $f_{unw} = 60$ MHz; $T_{amb} = 25$ °C.

Fig.11 Unwanted voltage for 1% cross-modulation as a function of gain reduction; typical values (see Fig.18).



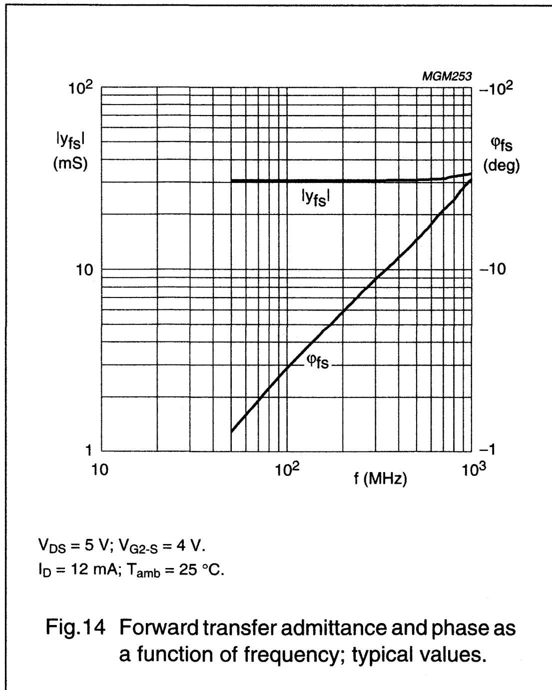
V_{DS} = 5 V; $V_{G2\text{-}S}$ = 4 V.
I_D = 12 mA; T_{amb} = 25 °C.

Fig.12 Input admittance as a function of frequency; typical values.



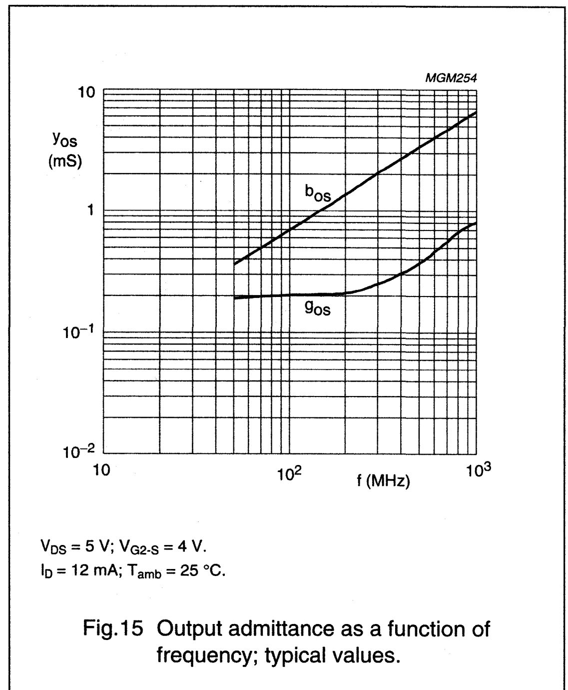
V_{DS} = 5 V; $V_{G2\text{-}S}$ = 4 V.
I_D = 12 mA; T_{amb} = 25 °C.

Fig.13 Reverse transfer admittance and phase as a function of frequency; typical values.



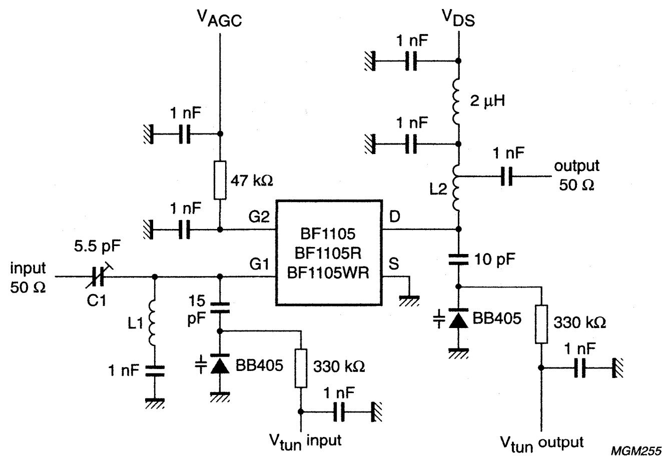
V_{DS} = 5 V; $V_{G2\text{-}S}$ = 4 V.
I_D = 12 mA; T_{amb} = 25 °C.

Fig.14 Forward transfer admittance and phase as a function of frequency; typical values.



V_{DS} = 5 V; $V_{G2\text{-}S}$ = 4 V.
I_D = 12 mA; T_{amb} = 25 °C.

Fig.15 Output admittance as a function of frequency; typical values.



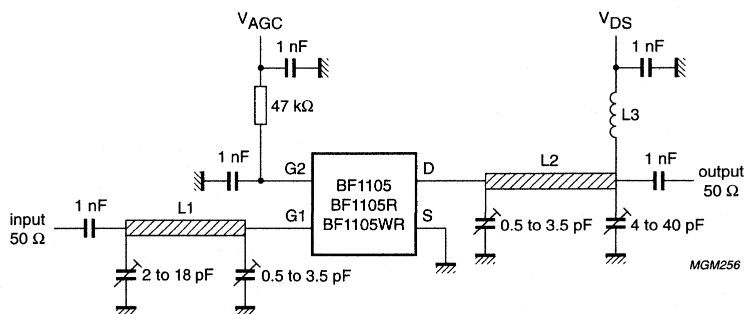
V_{DS} = 5 V, G_S= 2 mS, G_L = 0.5 mS, f = 200 MHz.

L1 = 45 nH, 4 turns, internal diameter = 4 mm, 0.8 mm copper wire.

L2 = 160 nH, 3 turns, internal diameter = 8 mm, 0.8 mm copper wire; tapped at approximately half a turn from the cold side, to set G_L = 0.5 mS.

C1 adjusted for G_S = 2 mS.

Fig.16 Gain test circuit.



V_{DS} = 5 V, G_S= 3.3 mS, G_L = 1 mS, f = 800 MHz.

L1 = 2 cm, silvered 0.8 mm copper wire 4 mm above ground plane.

L2 = 2 cm, silvered 0.8 mm copper wire 4 mm above ground plane.

L3 = 11 turns 0.5 mm copper wire without spacing, internal diameter = 3 mm, L = approx. 200 nH.

Fig.17 Gain test circuit.

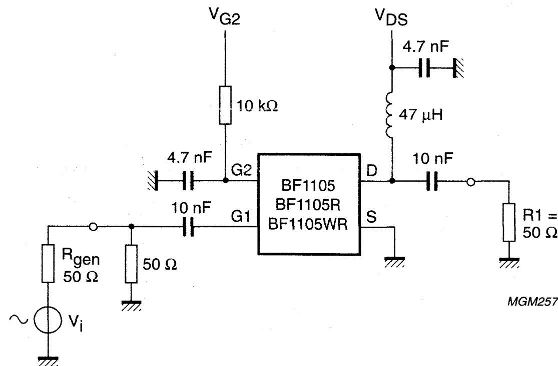


Fig.18 Cross-modulation test set-up.

Table 1 Scattering parameters: V_{DS} = 5 V; $V_{G2\text{-}S}$ = 4 V; I_D = 12 mA

f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)
50	0.994	−3.8	3.060	175.4	0.000	86.9	0.985	−2.1
100	0.991	−7.5	3.047	170.9	0.002	86.1	0.983	−4.2
200	0.982	−14.7	3.004	162.1	0.003	82.7	0.980	−8.3
300	0.968	−21.7	2.932	153.4	0.004	79.7	0.976	−12.1
400	0.956	−28.8	2.896	145.3	0.006	77.8	0.972	−16.2
500	0.937	−35.4	2.815	137.1	0.007	76.7	0.967	−20.0
600	0.918	−41.8	2.735	129.2	0.007	76.3	0.961	−23.7
700	0.897	−48.1	2.651	121.5	0.008	76.7	0.955	−27.3
800	0.878	−54.0	2.575	114.0	0.008	79.7	0.948	−30.9
900	0.858	−59.9	2.482	106.5	0.008	82.2	0.941	−34.4
1000	0.840	−65.5	2.396	99.5	0.008	88.0	0.935	−37.9

Table 2 Noise data: V_{DS} = 5 V; $V_{G2\text{-}S}$ = 4 V; I_D = 12 mA

f (MHz)	F_{min} (dB)	Γ_{opt}		R_n (Ω)
		(ratio)	(deg)	
800	1.5	0.674	39.7	37.15

FEATURES

- Short channel transistor with high forward transfer admittance to input capacitance ratio
- Low noise gain controlled amplifier up to 1 GHz
- Internal self-biasing circuit to ensure good cross-modulation performance during AGC and good DC stabilization.

APPLICATIONS

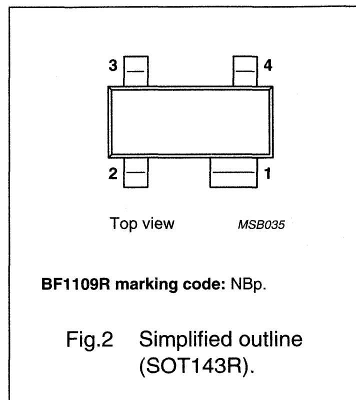
- VHF and UHF applications with 9 V supply voltage, such as television tuners and professional communications equipment.

DESCRIPTION

Enhancement type N-channel field-effect transistor with source and substrate interconnected. Integrated diodes between gates and source protect against excessive input voltage surges. The BF1109, BF1109R and BF1109WR are encapsulated in the SOT143B, SOT143R and SOT343R plastic packages respectively.

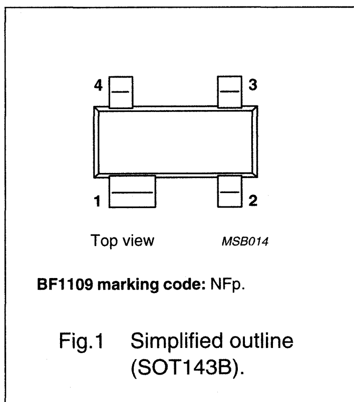
PINNING

PIN	DESCRIPTION
1	source
2	drain
3	gate 2
4	gate 1



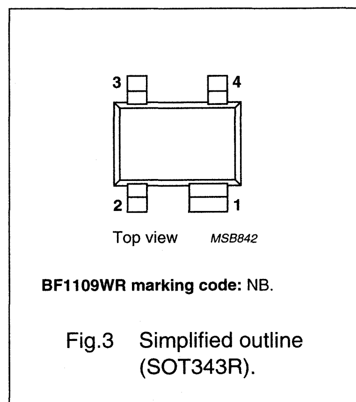
BF1109R marking code: NBp.

Fig.2 Simplified outline (SOT143R).



BF1109 marking code: NFp.

Fig.1 Simplified outline (SOT143B).



BF1109WR marking code: NB.

Fig.3 Simplified outline (SOT343R).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DS}	drain-source voltage		–	–	11	V
I_D	drain current (DC)		–	–	30	mA
P_{tot}	total power dissipation	$T_{amb} \leq 80$ °C	–	–	200	mW
$\|y_{fs}\|$	forward transfer admittance		–	30	–	mS
$C_{ig1\text{-}ss}$	input capacitance at gate 1		–	2.2	2.7	pF
C_{rss}	reverse transfer capacitance	f = 1 MHz	–	25	40	fF
F	noise figure	f = 800 MHz	–	1.5	2.5	dB
X_{mod}	cross-modulation	input level for k = 1% at 40 dB AGC	100	–	–	dBμV
T_j	operating junction temperature		–	–	150	°C

CAUTION
This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling. For further information, refer to Philips specs.: SNW-EQ-608, SNW-FQ-302A and SNW-FQ-302B.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	11	V
I_D	drain current (DC)		–	30	mA
I_{G1}	gate 1 current		–	±10	mA
I_{G2}	gate 2 current		–	±10	mA
P_{tot}	total power dissipation	$T_{amb} \leq 80$ °C; note 1	–	200	mW
T_{stg}	storage temperature		−65	+150	°C
T_j	operating junction temperature		–	+150	°C

Note

1. Device mounted on a printed-circuit board.

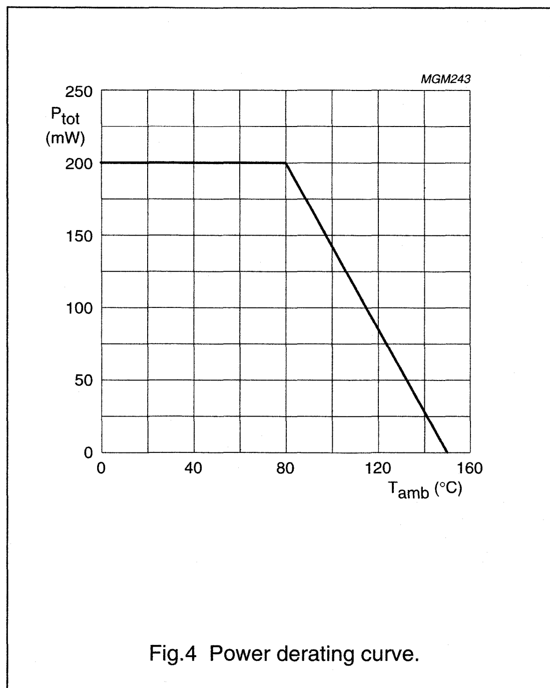


Fig.4 Power derating curve.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient in free air	note 1	350	K/W
$R_{th\ j-s}$	thermal resistance from junction to soldering point		200	K/W

Note

1. Device mounted on a printed-circuit board.

STATIC CHARACTERISTICS

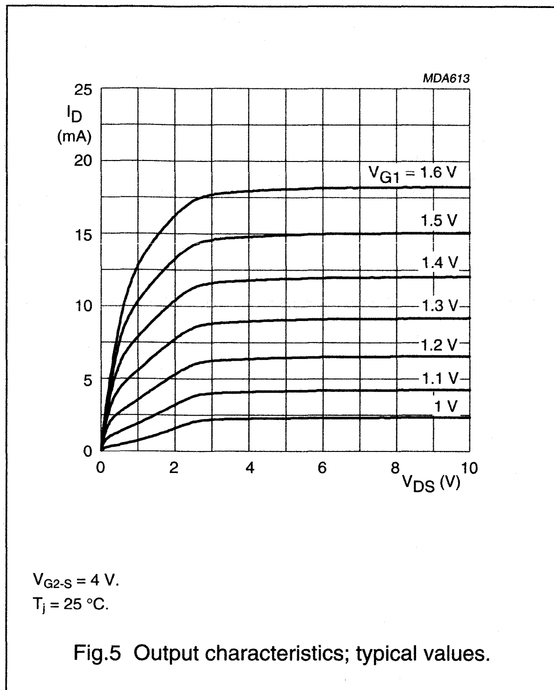
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{G1-S} = V_{G2-S} = 0$; $I_D = 10\ \mu A$	11	–	V
$V_{(BR)G1-SS}$	gate 1-source breakdown voltage	$V_{G2-S} = 0$; $I_{G1-S} = 10\ \mu A$; $I_D = 0$	11	–	V
$V_{(BR)G2-SS}$	gate 2-source breakdown voltage	$V_{G1-S} = V_{DS} = 0$; $I_{G2-S} = 10\ \mu A$	11	–	V
$V_{G2-S\ (th)}$	gate 2-source threshold voltage	$V_{G1-S} = 9$ V; $V_{DS} = 9$ V; $I_D = 20\ \mu A$	0.3	1.2	V
I_{DSX}	self-biasing drain current	$V_{G2-S} = 4$ V; $V_{DS} = 9$ V	8	16	mA
I_{G1-SS}	gate 1 cut-off current	$V_{G1-S} = 9$ V; $V_{G2-S} = 0$; $I_D = 0$	–	20	nA
I_{G2-SS}	gate 2 cut-off current	$V_{G1-S} = V_{DS} = 0$; $V_{G2-S} = 9$ V	–	20	nA

DYNAMIC CHARACTERISTICS

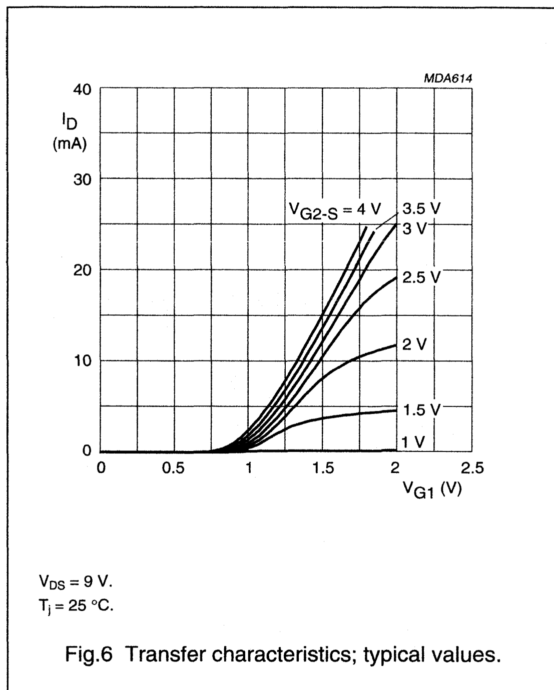
Common source; T_{amb} = 25 °C; V_{G2-S} = 4 V; V_{DS} = 9 V; self-biasing current; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\lvert y_{fs} \rvert$	forward transfer admittance	pulsed; T_j = 25 °C	24	30	–	mS
C_{ig1-ss}	input capacitance at gate 1	f = 1 MHz	–	2.2	2.7	pF
C_{ig2-ss}	input capacitance at gate 2	f = 1 MHz	–	1.5	–	pF
C_{oss}	output capacitance	f = 1 MHz	–	1.3	–	pF
C_{rss}	reverse transfer capacitance	f = 1 MHz	–	25	40	fF
F	noise figure	f = 800 MHz; $Y_S = Y_{S\ opt}$	–	1.5	2.5	dB
G_p	power gain	G_S = 2 mS; $B_S = B_{S\ opt}$; G_L = 0.5 mS; $B_L = B_{L\ opt}$; f = 200 MHz; see Fig.16	–	38	–	dB
		G_S = 3.3 mS; $B_S = B_{S\ opt}$; G_L = 1 mS; $B_L = B_{L\ opt}$; f = 800 MHz; see Fig.17	–	20	–	dB
X_{mod}	cross-modulation	input level for k = 1% at 0 dB AGC; f_w = 50 MHz; f_{unw} = 60 MHz; see Fig.18	85	–	–	dBμV
		input level for k = 1% at 40 dB AGC; f_w = 50 MHz; f_{unw} = 60 MHz; see Fig.18	100	–	–	dBμV



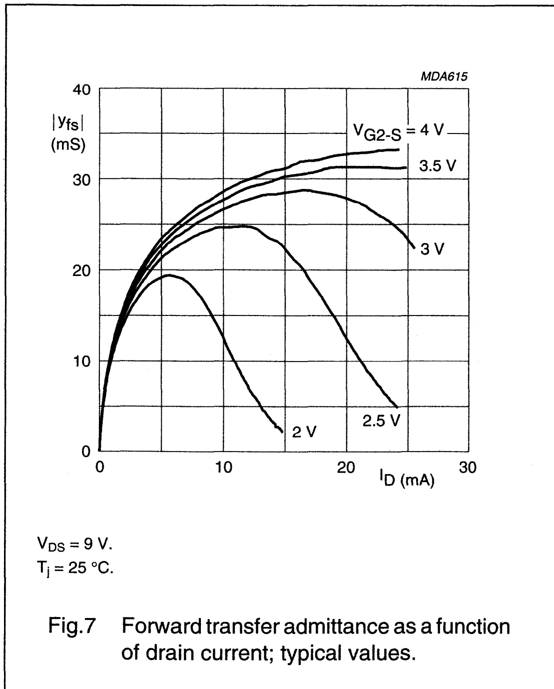
V_{G2-S} = 4 V.
T_j = 25 °C.

Fig.5 Output characteristics; typical values.



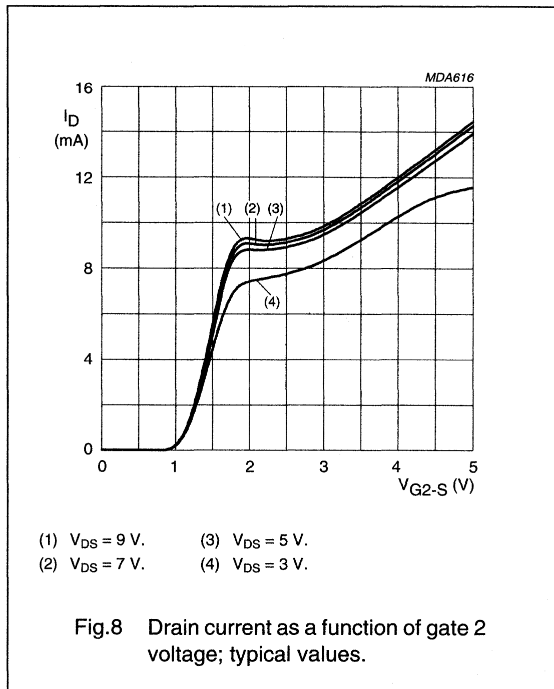
V_{DS} = 9 V.
T_j = 25 °C.

Fig.6 Transfer characteristics; typical values.



V_{DS} = 9 V.
T_j = 25 °C.

Fig.7 Forward transfer admittance as a function of drain current; typical values.



(1) V_{DS} = 9 V.
(2) V_{DS} = 7 V.
(3) V_{DS} = 5 V.
(4) V_{DS} = 3 V.

Fig.8 Drain current as a function of gate 2 voltage; typical values.

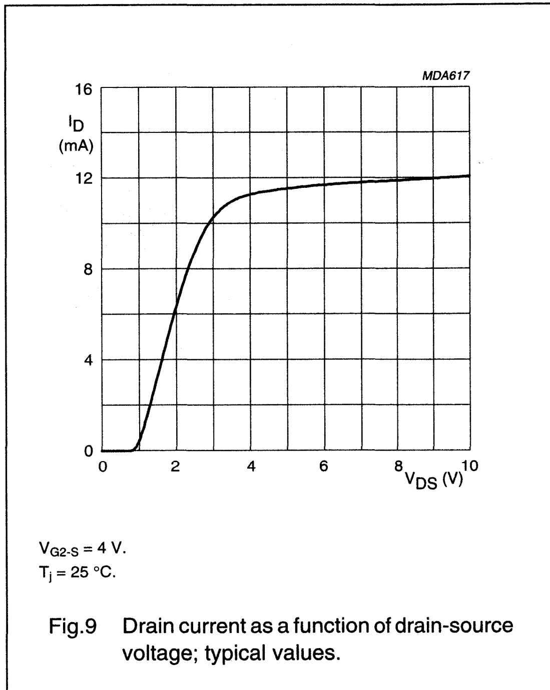


Fig.9 Drain current as a function of drain-source voltage; typical values.

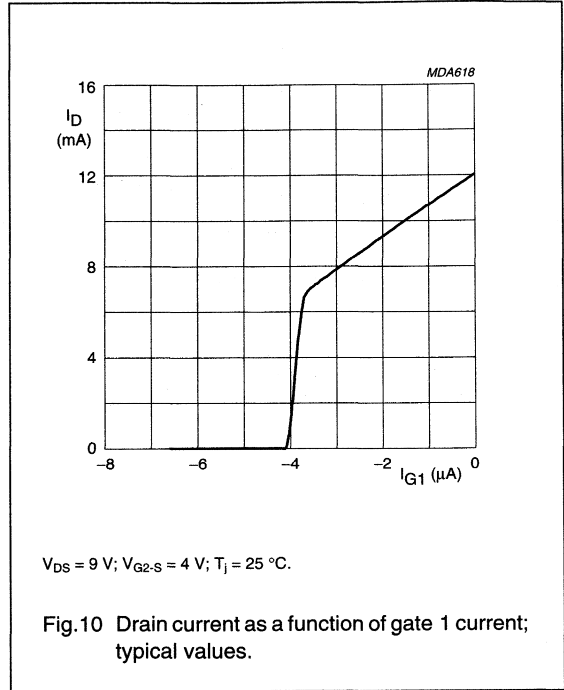


Fig.10 Drain current as a function of gate 1 current; typical values.

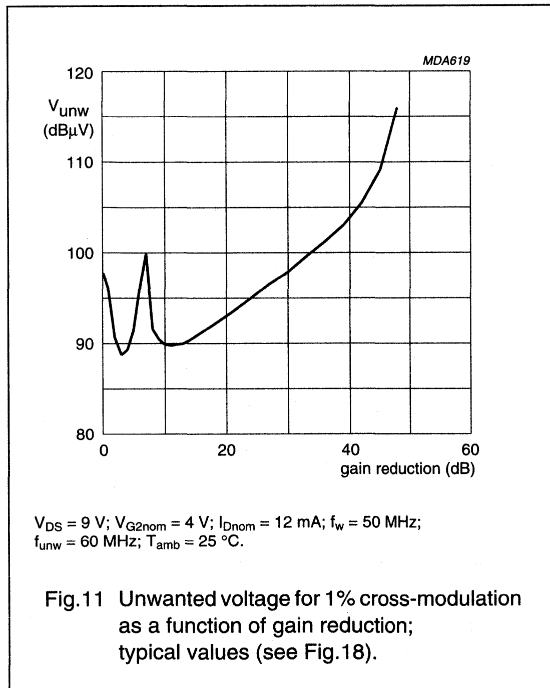
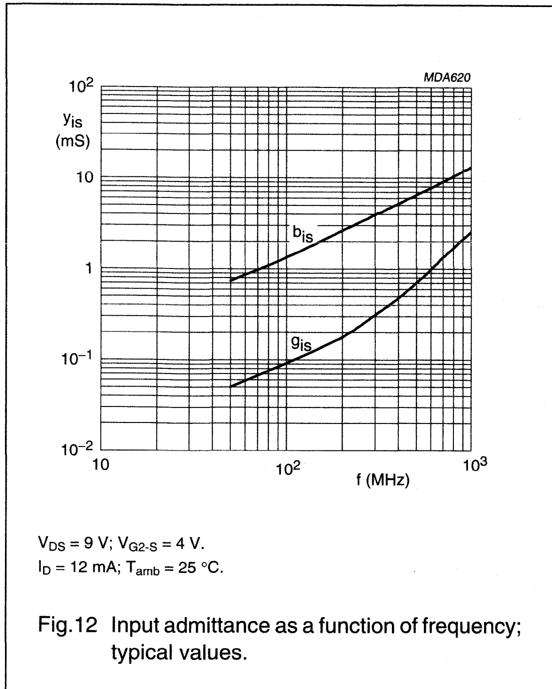
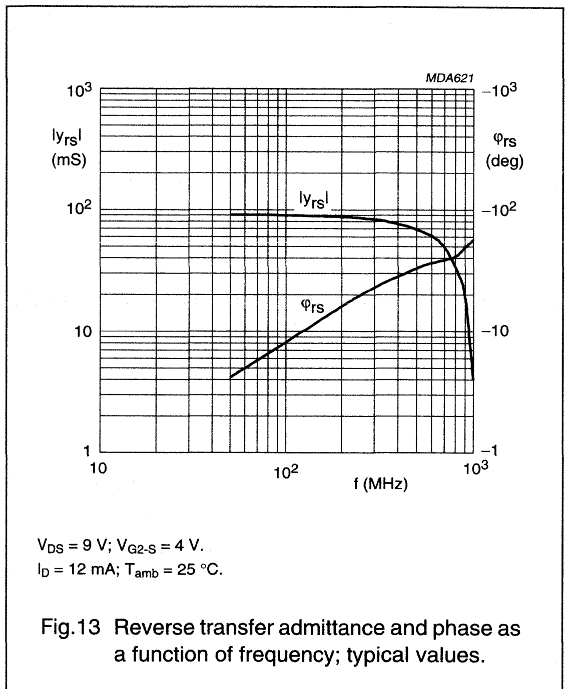


Fig.11 Unwanted voltage for 1% cross-modulation as a function of gain reduction; typical values (see Fig.18).



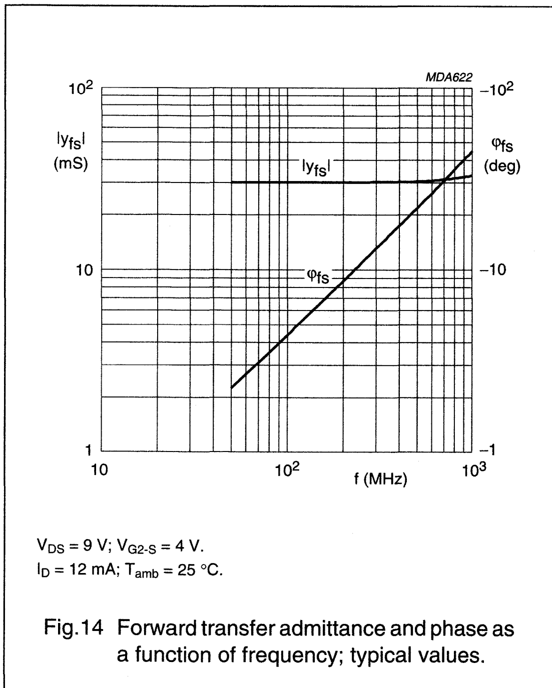
V_{DS} = 9 V; $V_{G2\text{-}S}$ = 4 V.
I_D = 12 mA; T_{amb} = 25 °C.

Fig.12 Input admittance as a function of frequency; typical values.



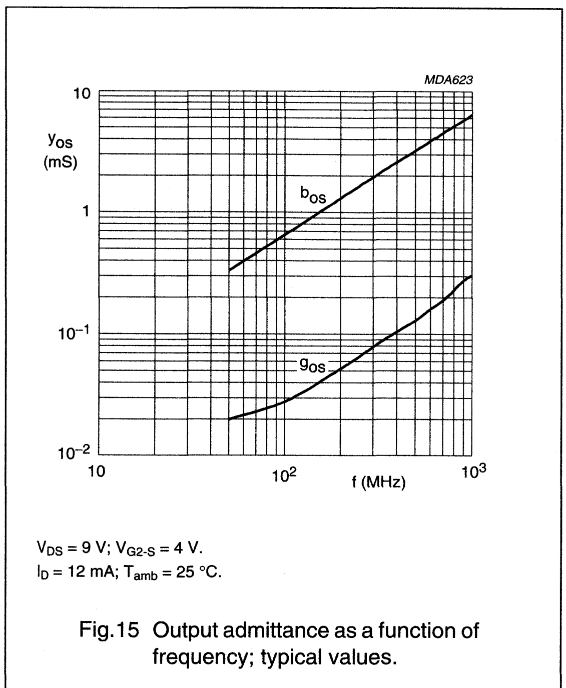
V_{DS} = 9 V; $V_{G2\text{-}S}$ = 4 V.
I_D = 12 mA; T_{amb} = 25 °C.

Fig.13 Reverse transfer admittance and phase as a function of frequency; typical values.



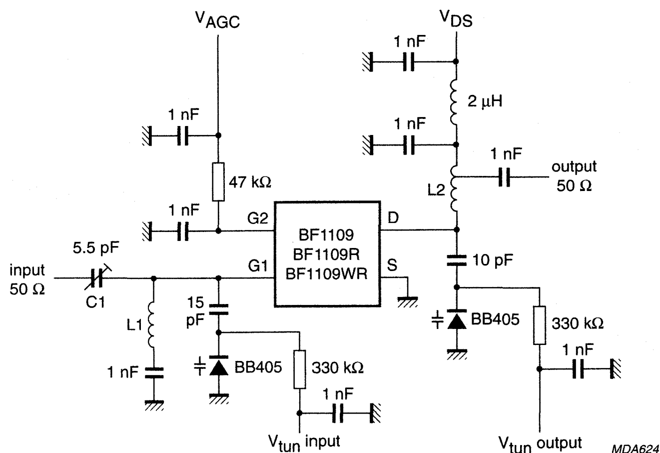
V_{DS} = 9 V; $V_{G2\text{-}S}$ = 4 V.
I_D = 12 mA; T_{amb} = 25 °C.

Fig.14 Forward transfer admittance and phase as a function of frequency; typical values.



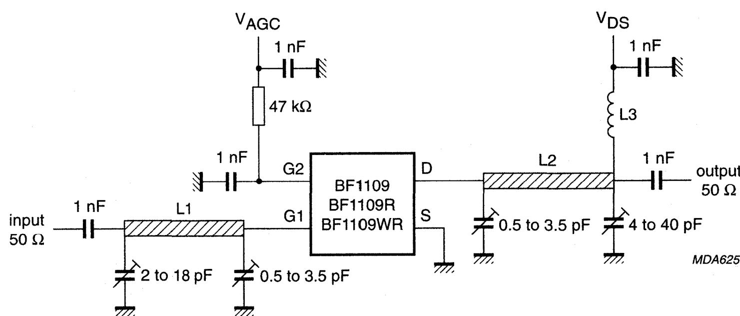
V_{DS} = 9 V; $V_{G2\text{-}S}$ = 4 V.
I_D = 12 mA; T_{amb} = 25 °C.

Fig.15 Output admittance as a function of frequency; typical values.



V_{DS} = 9 V, G_S = 2 mS, G_L = 0.5 mS, f = 200 MHz.
L1 = 45 nH, 4 turns, internal diameter = 4 mm, 0.8 mm copper wire.
L2 = 160 nH, 3 turns, internal diameter = 8 mm, 0.8 mm copper wire; tapped at approximately half a turn from the cold side, to set G_L = 0.5 mS.
C1 adjusted for G_S = 2 mS.

Fig.16 Gain test circuit.



V_{DS} = 9 V, G_S = 3.3 mS, G_L = 1 mS, f = 800 MHz.
L1 = 2 cm, silvered 0.8 mm copper wire 4 mm above ground plane.
L2 = 2 cm, silvered 0.8 mm copper wire 4 mm above ground plane.
L3 = 11 turns 0.5 mm copper wire without spacing, internal diameter = 3 mm, L = approx. 200 nH.

Fig.17 Gain test circuit.

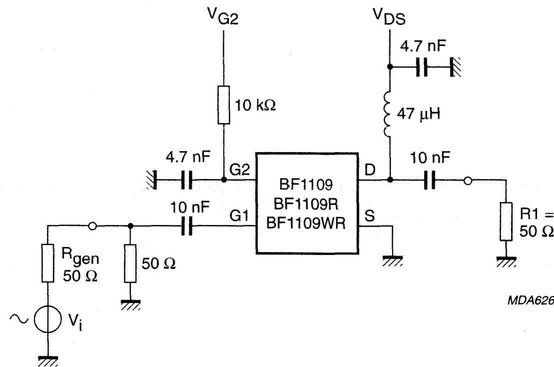


Fig.18 Cross-modulation test set-up.

Table 1 Scattering parameters: V_{DS} = 9 V; $V_{G2\text{-}S}$ = 4 V; I_D = 12 mA

f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
	MAGNITUDE (ratio)	**ANGLE (deg)**	**MAGNITUDE (ratio)**	**ANGLE (deg)**	**MAGNITUDE (ratio)**	**ANGLE (deg)**	**MAGNITUDE (ratio)**	**ANGLE (deg)**
50	0.995	−3.71	3.013	175.0	0.000	88.2	0.998	−1.8
100	0.992	−7.29	3.002	170.2	0.001	83.7	0.997	−3.5
200	0.984	−14.3	2.967	160.7	0.002	86.2	0.995	−7.0
300	0.973	−21.2	2.922	151.3	0.002	83.2	0.992	−10.5
400	0.961	−27.9	2.869	142.0	0.003	84.1	0.990	−13.9
500	0.944	−34.4	2.793	132.9	0.003	85.7	0.987	−17.2
600	0.926	−40.8	2.730	124.1	0.003	88.4	0.985	−20.5
700	0.906	−46.9	2.660	1115.3	0.003	94.6	0.983	−23.7
800	0.887	−52.9	2.605	106.5	0.004	107.2	0.981	−26.8
900	0.868	−58.8	2.527	97.8	0.004	114.9	0.977	−30.0
1000	0.852	−64.3	2.457	89.6	0.004	129.7	0.9377	−33.1

Table 2 Noise data: V_{DS} = 9 V; $V_{G2\text{-}S}$ = 4 V; I_D = 12 mA

f (MHz)	F_{min} (dB)	Γ_{opt}		R_n (Ω)
		(ratio)	**(deg)**	
800	1.5	0.684	40.94	40.4

DESCRIPTION

Planar epitaxial symmetrical junction N-channel field-effect transistor in a plastic SOT23 package.

APPLICATIONS

- Low level general purpose amplifiers in thick and thin-film circuits.

PINNING - SOT23

PIN	SYMBOL	DESCRIPTION
1	d	drain(1)
2	s	source(1)
3	g	gate

Note

1. Drain and source are interchangeable.

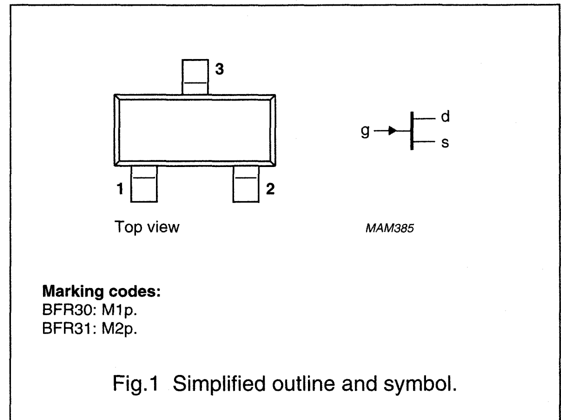


Fig.1 Simplified outline and symbol.

CAUTION

This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling. For further information, refer to Philips specs.: SNW-EQ-608, SNW-FQ-302A and SNW-FQ-302B.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	±25	V
V_{GSO}	gate-source voltage	open drain	–	–25	V
P_{tot}	total power dissipation	$T_{amb} \leq 40$ °C	–	250	mW
I_{DSS}	drain current	$V_{GS} = 0$; $V_{DS} = 10$ V			
	BFR30		4	10	mA
	BFR31		1	5	mA
$\lvert y_{fs} \rvert$	common-source transfer admittance	$I_D = 1$ mA; $V_{DS} = 10$ V; f = 1 kHz			
	BFR30		1	4	mS
	BFR31		1.5	4.5	mS

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	±25	V
V_{DGO}	drain-gate voltage	open source	–	–25	V
V_{GSO}	gate-source voltage	open drain	–	–25	V
I_D	drain current		–	10	mA
I_G	forward gate current (DC)		–	5	mA
P_{tot}	total power dissipation	$T_{amb} \leq 40$ °C; note 1; see Fig.2	–	250	mW
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–	150	°C

Note

1. Mounted on a ceramic substrate of 8 × 10 × 0.7 mm.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	note 1	430	K/W

Note

1. Mounted on a ceramic substrate of 8 × 10 × 0.7 mm.

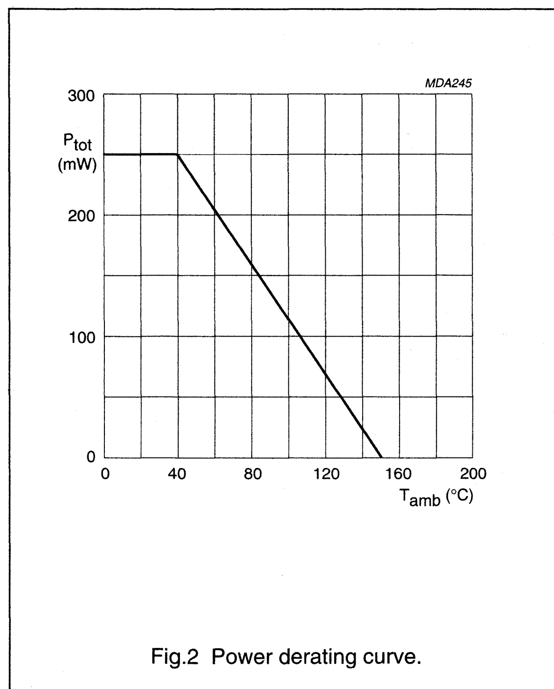
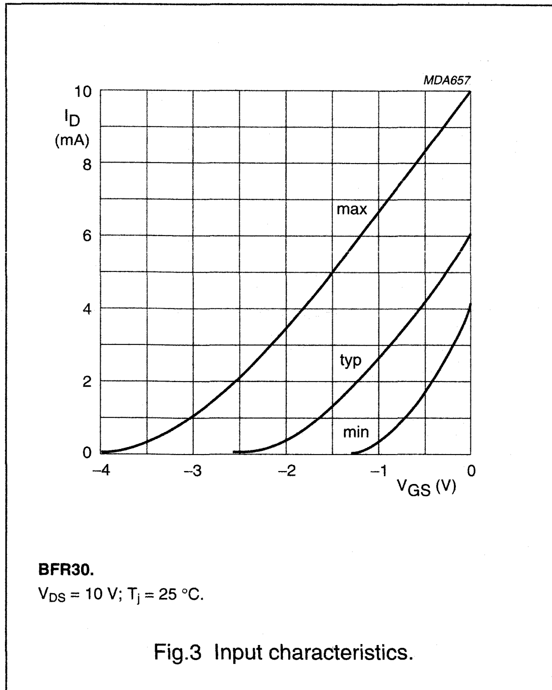


Fig.2 Power derating curve.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

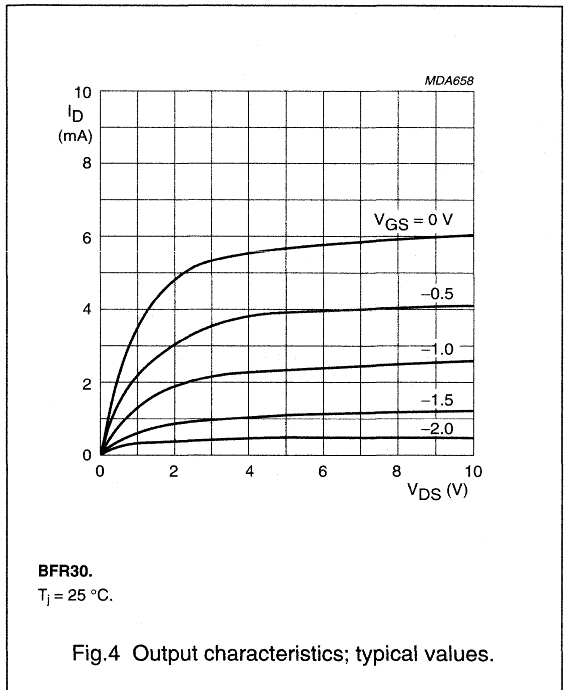
SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{GSS}	gate cut-off current	V_{DS} = 0; V_{GS} = −10 V	–	−0.2	nA
I_{DSS}	drain current	V_{GS} = 0; V_{DS} = 10 V			
	BFR30		4	10	mA
	BFR31		1	5	mA
V_{GS}	gate-source voltage	I_D = 1 mA; V_{DS} = 10 V			
	BFR30		−0.7	−3	V
	BFR31		0	−1.3	V
V_{GS}	gate-source voltage	I_D = 50 μA; V_{DS} = 10 V			
	BFR30		–	−4	V
	BFR31		–	−2	V
V_{GSoff}	gate-source cut-off voltage	I_D = 0.5 nA; V_{DS} = 10 V			
	BFR30		–	−5	V
	BFR31		–	−2.5	V
$\|y_{fs}\|$	common-source transfer admittance	I_D = 1 mA; V_{DS} = 10 V; f = 1 kHz; T_{amb} = 25 °C			
	BFR30		1	4	mS
	BFR31		1.5	4.5	mS
$\|y_{fs}\|$	common-source transfer admittance	I_D = 200 μA; V_{DS} = 10 V; f = 1 kHz; T_{amb} = 25 °C			
	BFR30		0.5	–	mS
	BFR31		0.75	–	mS
$\|y_{os}\|$	common source output admittance	I_D = 1 mA; V_{DS} = 10 V; f = 1 kHz			
	BFR30		–	40	μS
	BFR31		–	25	μS
$\|y_{os}\|$	common source output admittance	I_D = 200 μA; V_{DS} = 10 V; f = 1 kHz			
	BFR30		–	20	μS
	BFR31		–	15	μS
C_{is}	input capacitance	V_{DS} = 10 V; f = 1 MHz			
		I_D = 1 mA	–	4	pF
		I_D = 0.2 nA	–	4	pF
C_{rs}	feedback capacitance	V_{DS} = 10 V; f = 1 MHz; T_{amb} = 25 °C			
		I_D = 1 mA	–	1.5	pF
		I_D = 200 μA	–	1.5	pF
V_n	equivalent input noise voltage	I_D = 200 μA; V_{DS} = 10 V; B = 0.6 to 100 Hz	–	0.5	μV



BFR30.

V_{DS} = 10 V; T_j = 25 °C.

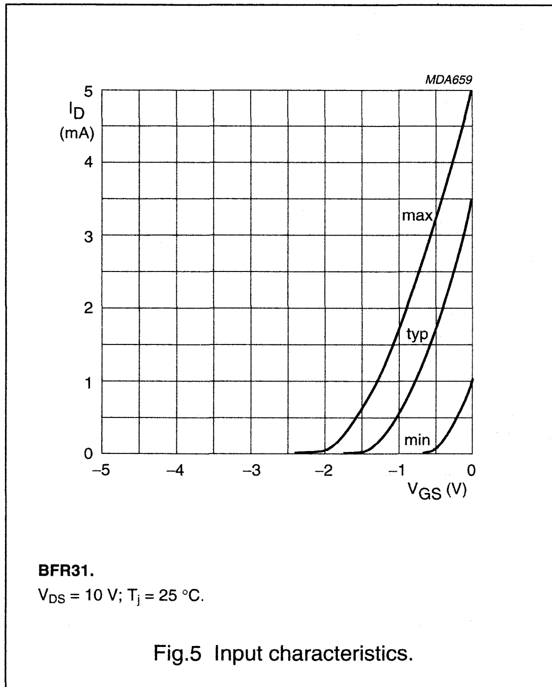
Fig.3 Input characteristics.



BFR30.

T_j = 25 °C.

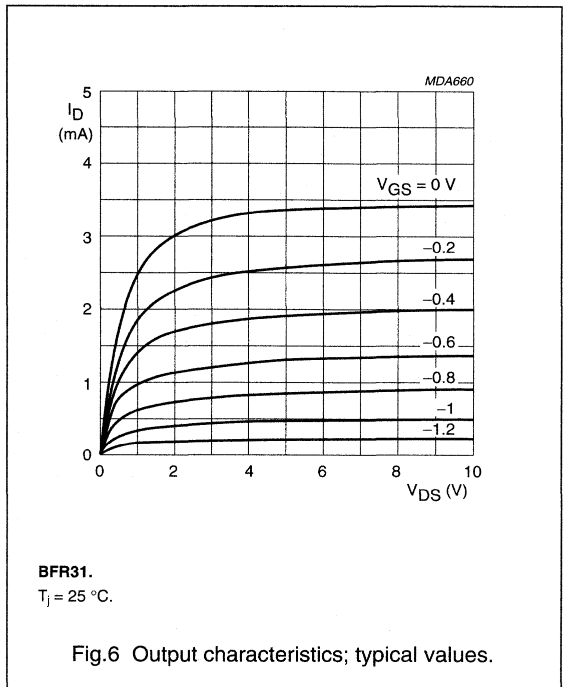
Fig.4 Output characteristics; typical values.



BFR31.

V_{DS} = 10 V; T_j = 25 °C.

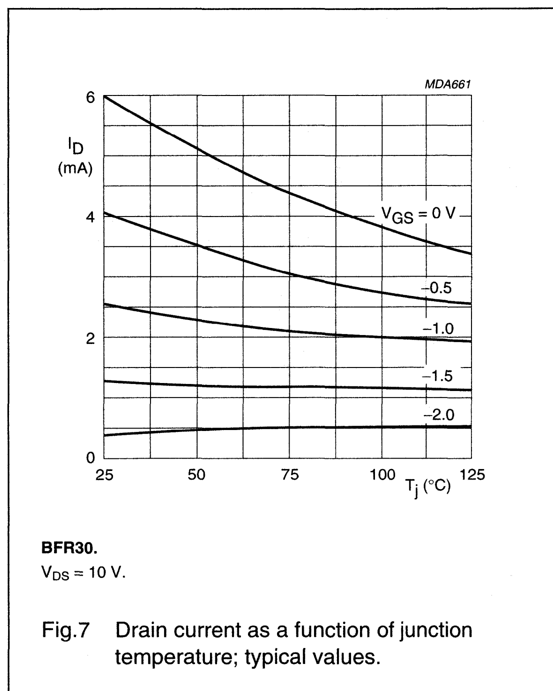
Fig.5 Input characteristics.



BFR31.

T_j = 25 °C.

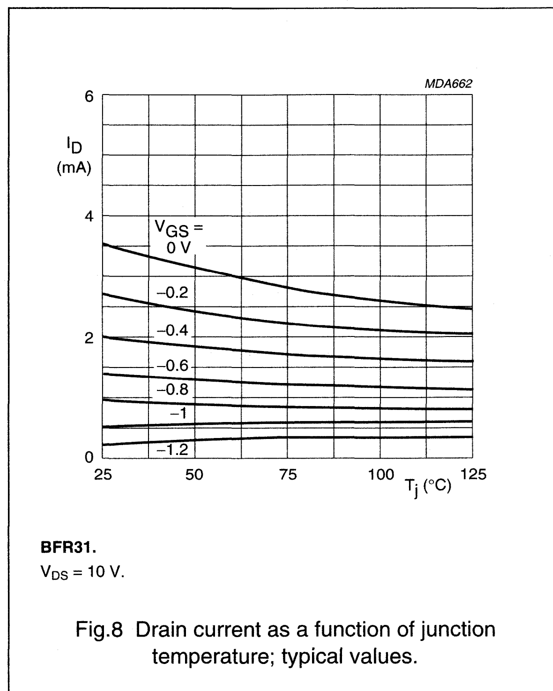
Fig.6 Output characteristics; typical values.



BFR30.

V_{DS} = 10 V.

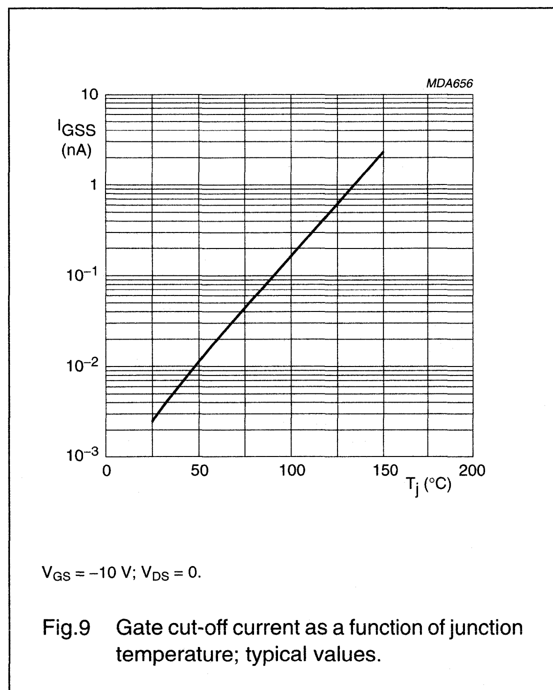
Fig.7 Drain current as a function of junction temperature; typical values.



BFR31.

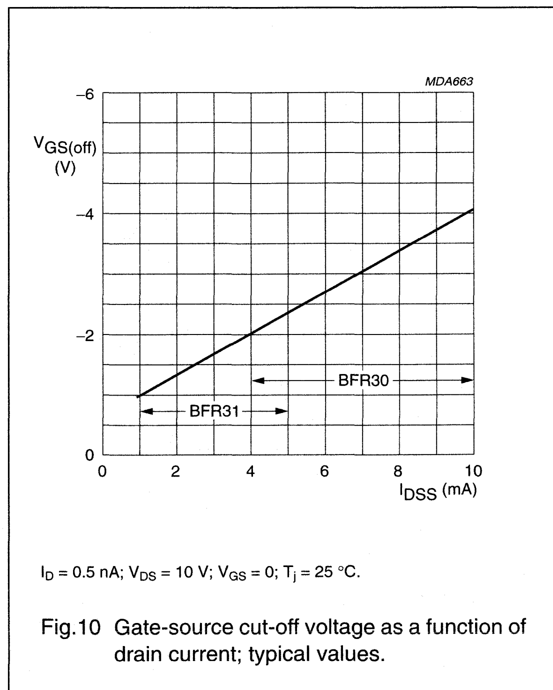
V_{DS} = 10 V.

Fig.8 Drain current as a function of junction temperature; typical values.



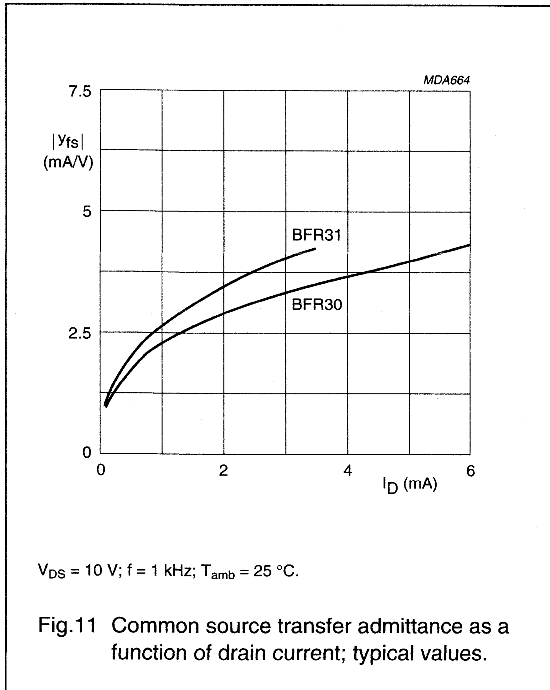
V_{GS} = −10 V; V_{DS} = 0.

Fig.9 Gate cut-off current as a function of junction temperature; typical values.



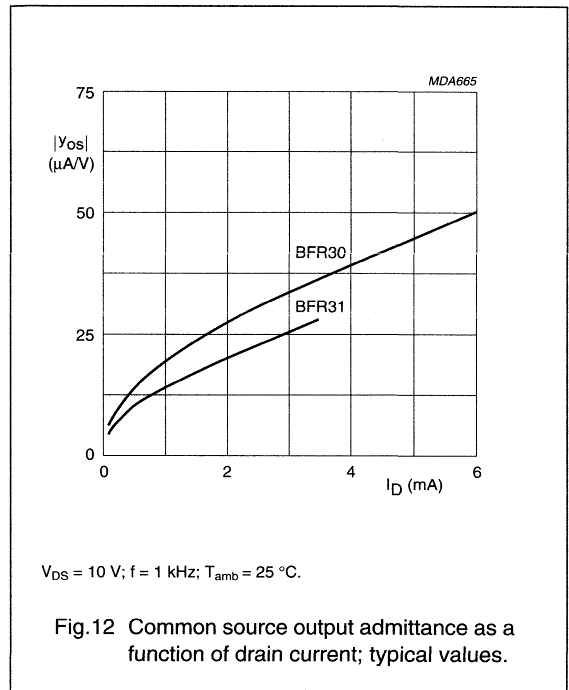
I_D = 0.5 nA; V_{DS} = 10 V; V_{GS} = 0; T_j = 25 °C.

Fig.10 Gate-source cut-off voltage as a function of drain current; typical values.



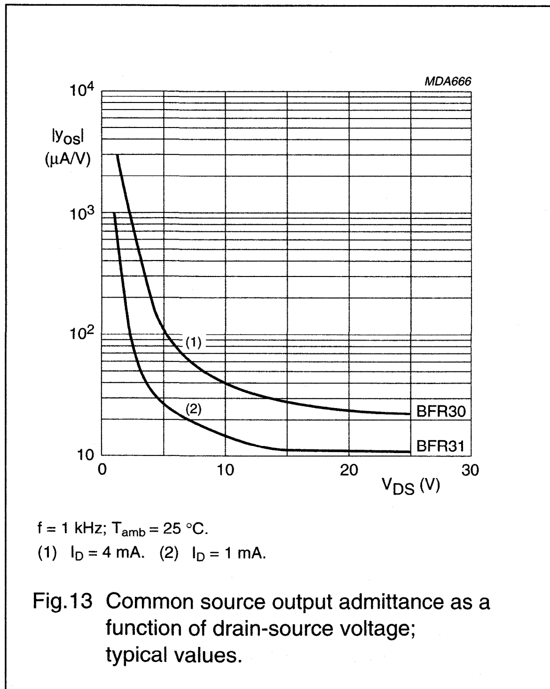
V_{DS} = 10 V; f = 1 kHz; T_{amb} = 25 °C.

Fig.11 Common source transfer admittance as a function of drain current; typical values.



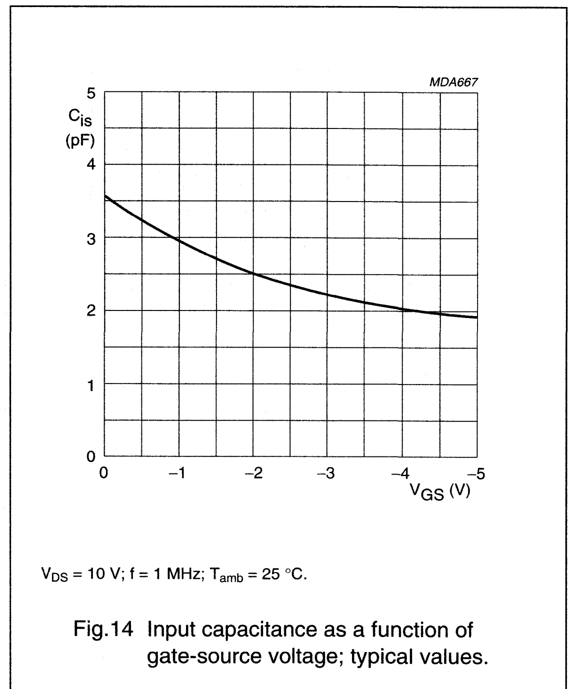
V_{DS} = 10 V; f = 1 kHz; T_{amb} = 25 °C.

Fig.12 Common source output admittance as a function of drain current; typical values.



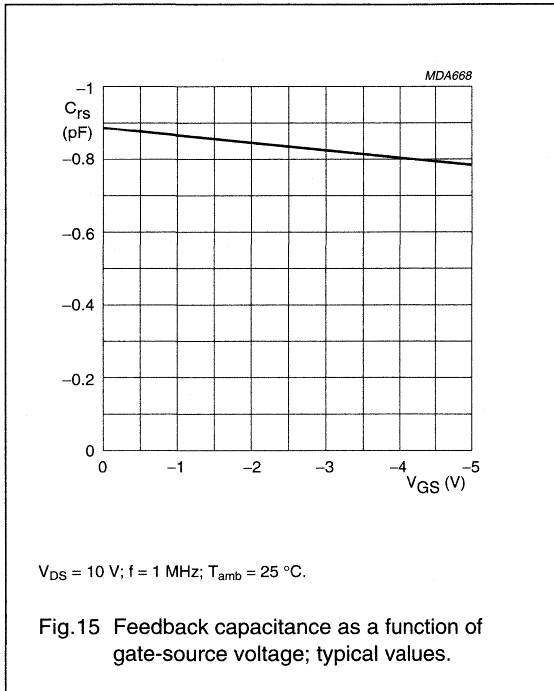
f = 1 kHz; T_{amb} = 25 °C.
(1) I_D = 4 mA. (2) I_D = 1 mA.

Fig.13 Common source output admittance as a function of drain-source voltage; typical values.



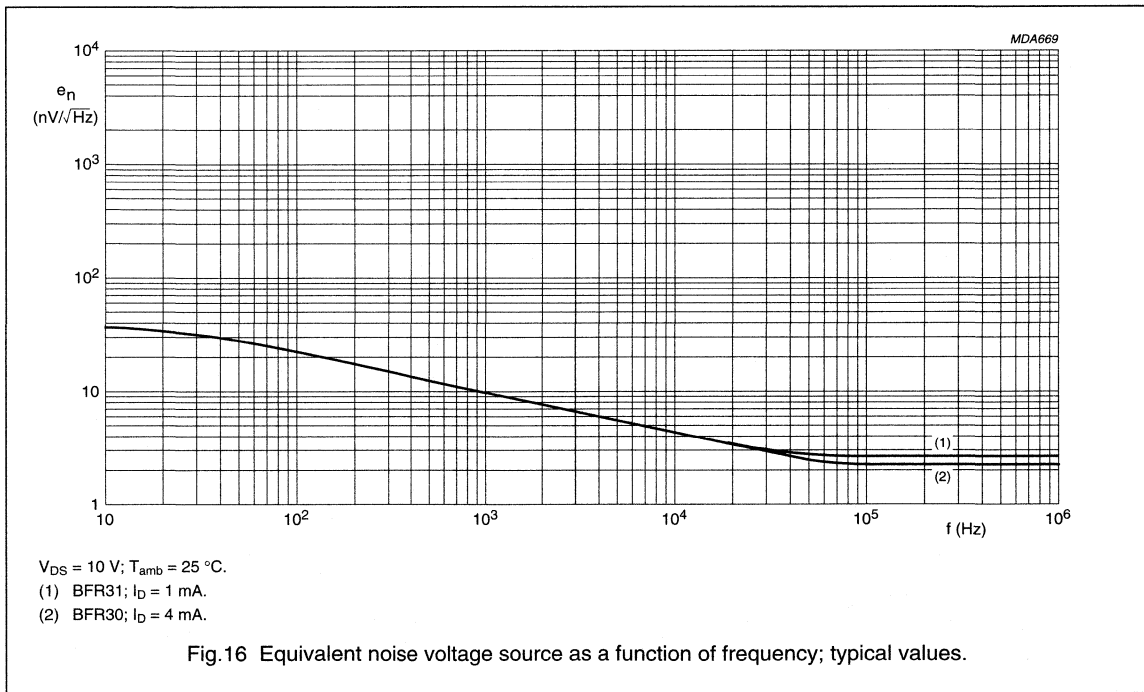
V_{DS} = 10 V; f = 1 MHz; T_{amb} = 25 °C.

Fig.14 Input capacitance as a function of gate-source voltage; typical values.



V_{DS} = 10 V; f = 1 MHz; T_{amb} = 25 °C.

Fig.15 Feedback capacitance as a function of gate-source voltage; typical values.

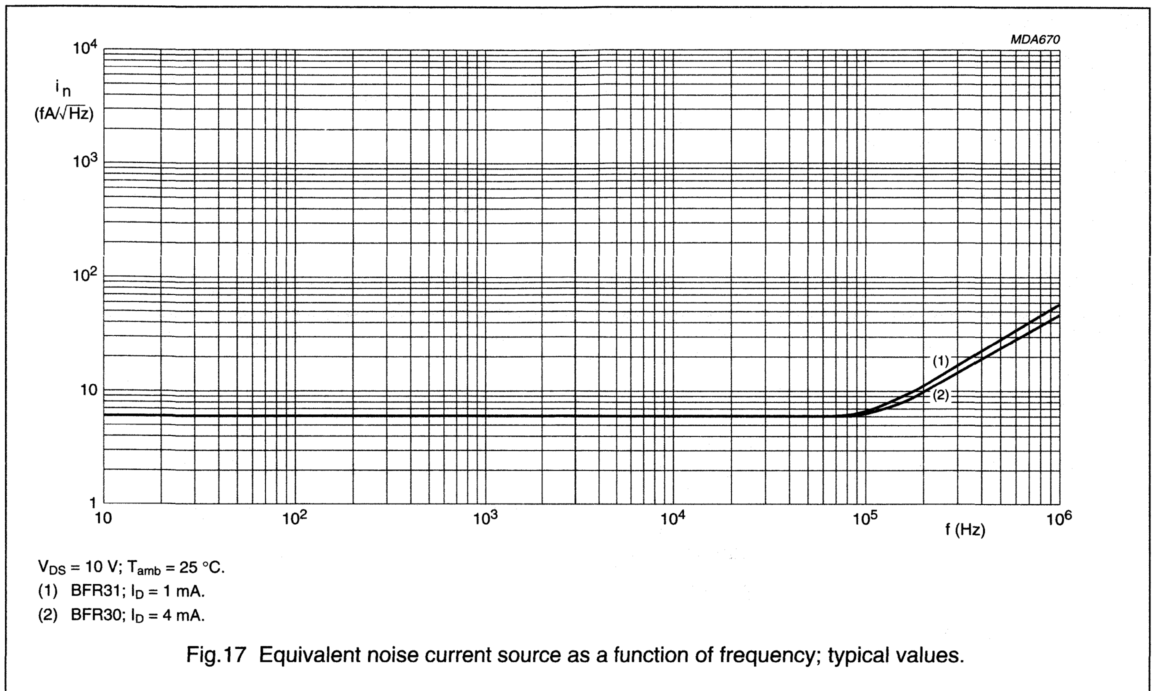


V_{DS} = 10 V; T_{amb} = 25 °C.

(1) BFR31; I_D = 1 mA.

(2) BFR30; I_D = 4 mA.

Fig.16 Equivalent noise voltage source as a function of frequency; typical values.



V_{DS} = 10 V; T_{amb} = 25 °C.
(1) BFR31; I_D = 1 mA.
(2) BFR30; I_D = 4 mA.

Fig.17 Equivalent noise current source as a function of frequency; typical values.

N-channel silicon FET

BFT46

DESCRIPTION

Symmetrical n-channel silicon epitaxial planar junction field-effect transistor in a microminiature plastic envelope. The transistor is intended for low level general purpose amplifiers in thick and thin-film circuits.

PINNING

1 = drain

2 = source

3 = gate

Note : Drain and source are interchangeable.

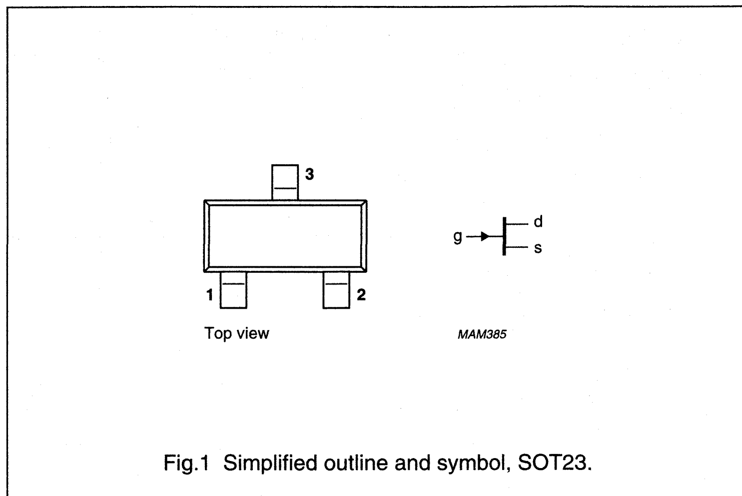


Fig.1 Simplified outline and symbol, SOT23.

Marking code

BFT46 = M3p

QUICK REFERENCE DATA

Drain-source voltage	$\pm V_{DS}$	max.	25	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	25	V
Total power dissipation up to T_{amb} = 40 °C	P_{tot}	max.	250	mW
Drain current				
V_{DS} = 10 V; V_{GS} = 0	I_{DSS}	>	0,2	mA
		<	1,5	mA
Transfer admittance (common source)				
I_D = 0,2 mA; V_{DS} = 10 V; f = 1 kHz	$\lvert y_{fs} \rvert$	>	0,5	mS
Equivalent noise voltage				
V_{DS} = 10 V; I_D = 200 μA; B = 0,6 to 100 Hz	V_n	<	0,5	μV

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	25	V
Drain-gate voltage (open source)	V_{DGO}	max.	25	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	25	V
Drain current	I_D	max.	10	mA
Gate current	I_G	max.	5	mA
Total power dissipation up to T_{amb} = 40 °C[1]	P_{tot}	max.	250	mW
Storage temperature range	T_{stg}		−65 to +150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient[1]	$R_{th\ j\text{-}a}$	=	430	K/W

Note

1. Mounted on a ceramic substrate of 8 mm × 10 mm × 0,7 mm.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Gate cut-off current				
$-V_{GS}$ = 10 V; V_{DS} = 0	$-I_{GSS}$	<	0,2	nA
Drain current				
V_{DS} = 10 V; V_{GS} = 0	I_{DSS}	>	0,2	mA
		<	1,5	mA
Gate-source voltage				
I_D = 50 μA; V_{DS} = 10 V	$-V_{GS}$	>	0,1	V
		<	1,0	V
Gate-source cut-off voltage				
I_D = 0,5 nA; V_{DS} = 10 V	$-V_{(P)GS}$	<	1,2	V
y-parameters at f = 1 kHz;				
V_{DS} = 10 V; V_{GS} = 0; T_{amb} = 25 °C				
Transfer admittance	$\lvert y_{fs} \rvert$	>	1,0	mS
Output admittance	$\lvert y_{os} \rvert$	<	10	μS
V_{DS} = 10 V; I_D = 200 μA; T_{amb} = 25 °C				
Transfer admittance	$\lvert y_{fs} \rvert$	>	0,5	mS
Output admittance	$\lvert y_{os} \rvert$	<	5	μS
Input capacitance at f = 1 MHz;				
V_{DS} = 10 V; V_{GS} = 0; T_{amb} = 25 °C	C_{is}	<	5	pF
Feedback capacitance at f = 1 MHz;				
V_{DS} = 10 V; V_{GS} = 0; T_{amb} = 25 °C	C_{rs}	<	1,5	pF
Equivalent noise voltage				
V_{DS} = 10 V; I_D = 200 μA; T_{amb} = 25 °C				
B = 0,6 to 100 Hz	V_n	<	0,5	μV

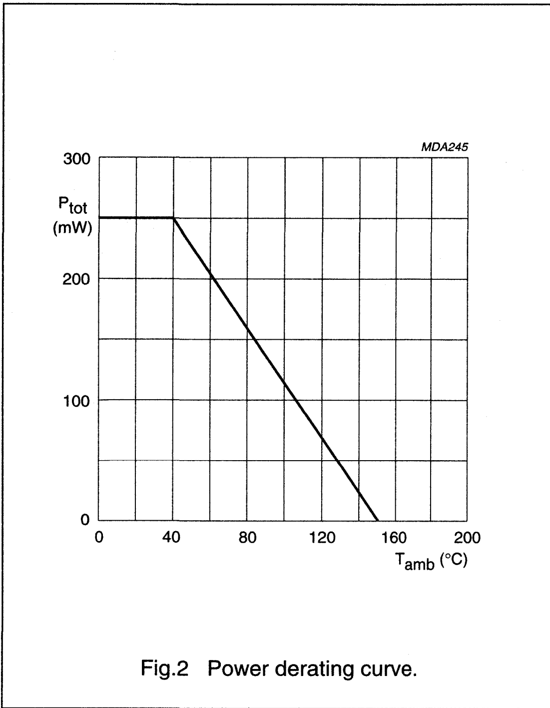


Fig.2 Power derating curve.

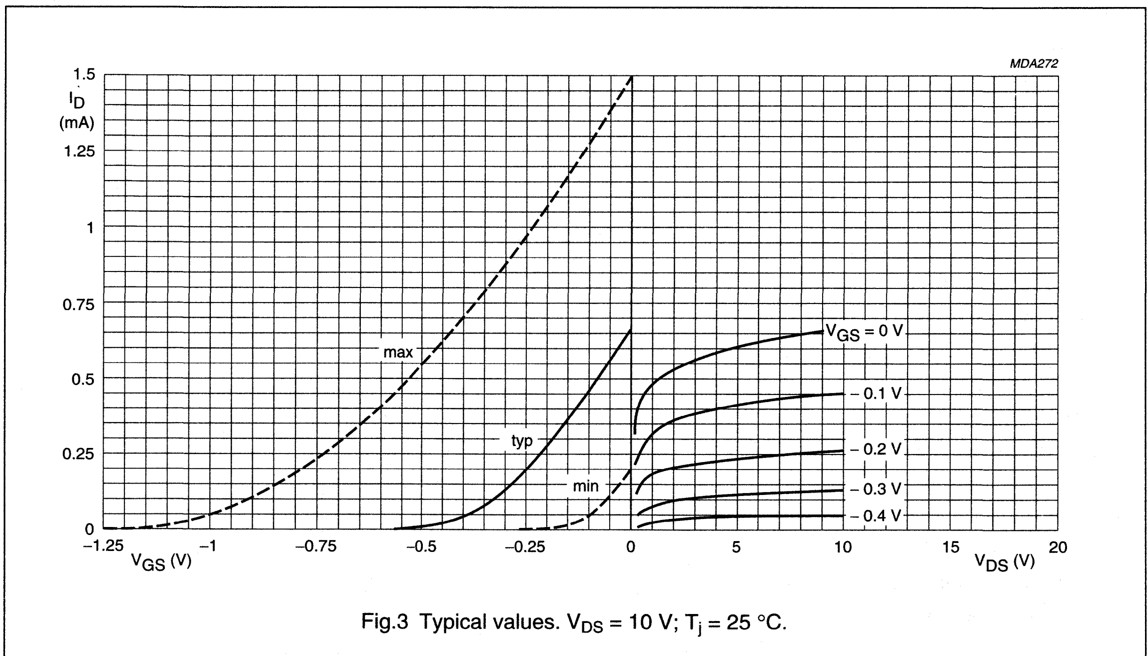


Fig.3 Typical values. V_{DS} = 10 V; T_j = 25 °C.

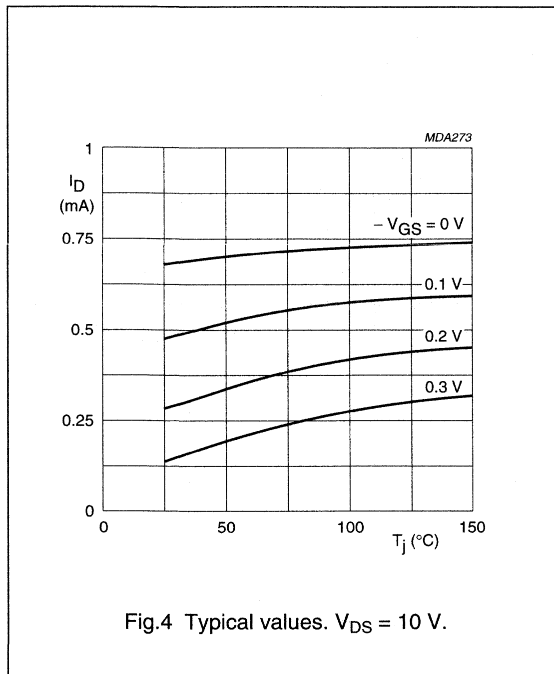


Fig.4 Typical values. V_{DS} = 10 V.

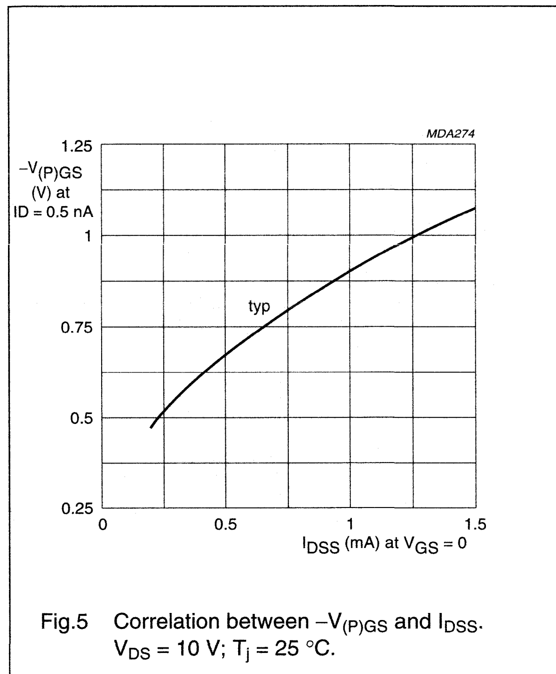


Fig.5 Correlation between $-V_{(P)GS}$ and I_{DSS}. V_{DS} = 10 V; T_j = 25 °C.

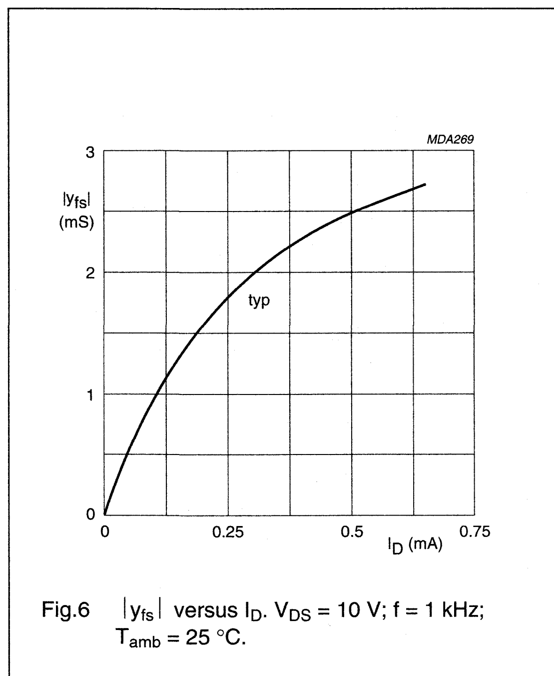


Fig.6 $|y_{fs}|$ versus I_D. V_{DS} = 10 V; f = 1 kHz; T_{amb} = 25 °C.

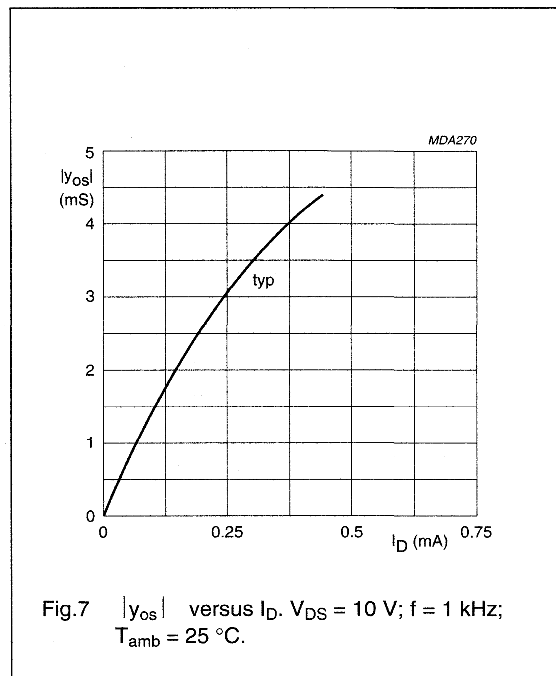


Fig.7 $|y_{os}|$ versus I_D. V_{DS} = 10 V; f = 1 kHz; T_{amb} = 25 °C.

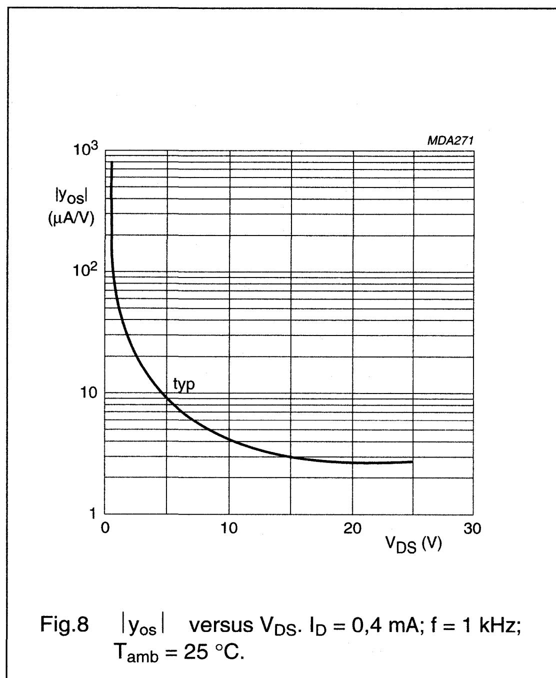


Fig.8 $|y_{os}|$ versus V_{DS}. I_D = 0,4 mA; f = 1 kHz; T_{amb} = 25 °C.

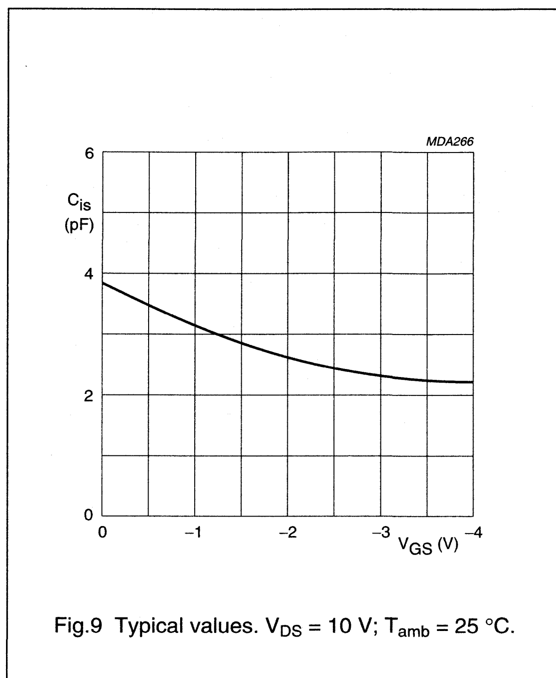


Fig.9 Typical values. V_{DS} = 10 V; T_{amb} = 25 °C.

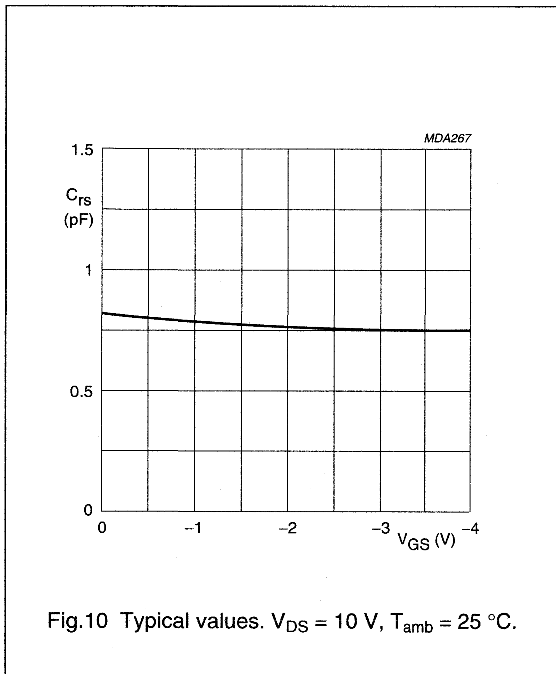


Fig.10 Typical values. V_{DS} = 10 V, T_{amb} = 25 °C.

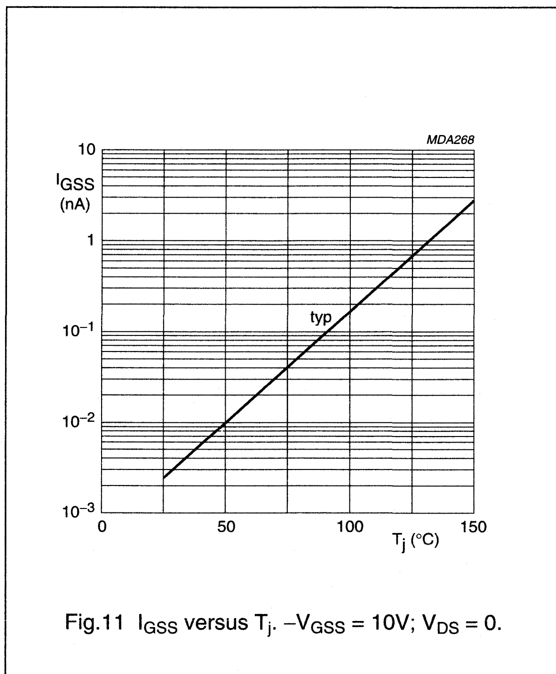


Fig.11 I_{GSS} versus T_j. $-V_{GSS}$ = 10V; V_{DS} = 0.

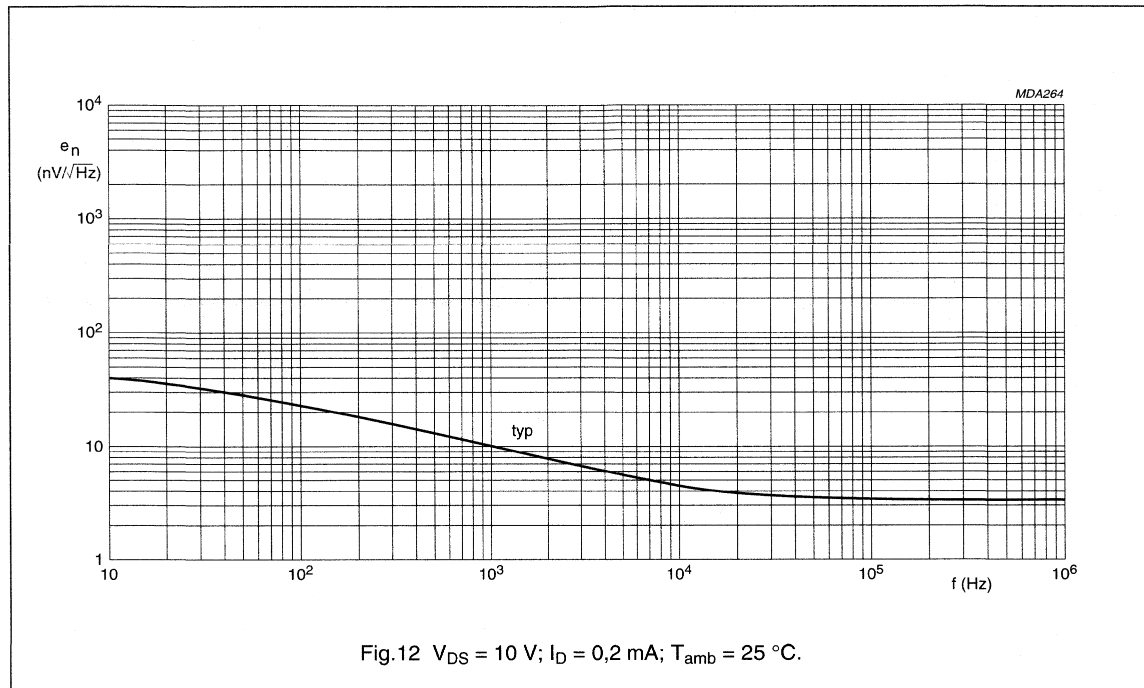


Fig.12 V_{DS} = 10 V; I_D = 0,2 mA; T_{amb} = 25 °C.

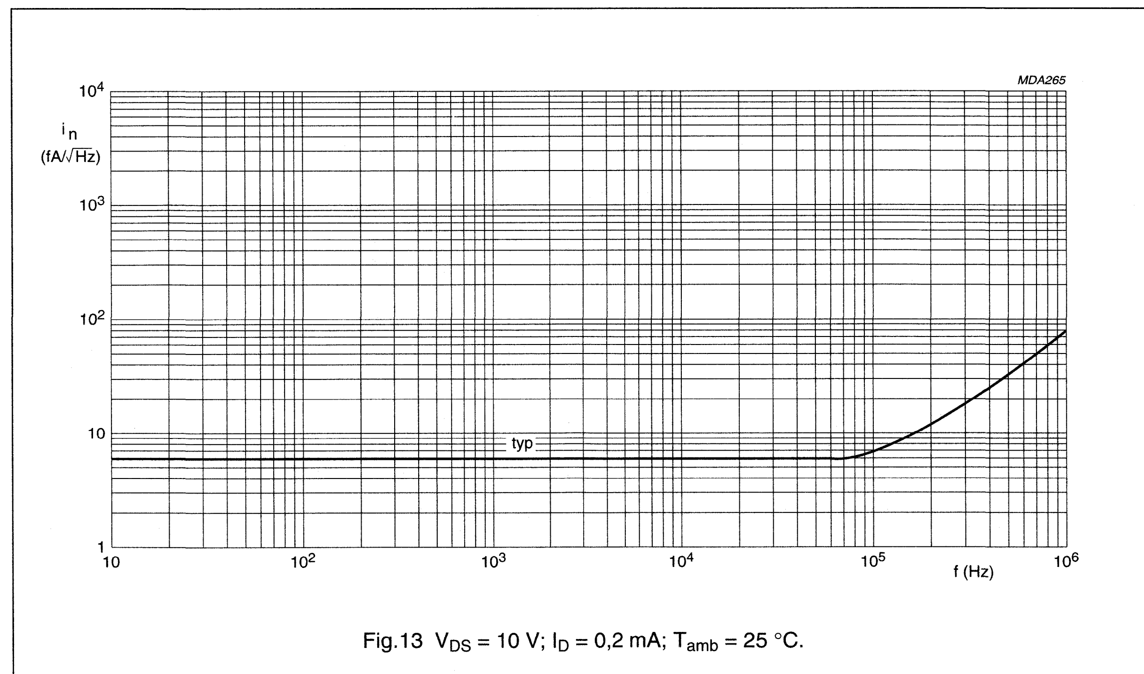


Fig.13 V_{DS} = 10 V; I_D = 0,2 mA; T_{amb} = 25 °C.

MOSFET N-channel depletion switching transistor BSD22

DESCRIPTION

Symmetrical insulated-gate silicon MOS field-effect transistor of the n-channel depletion mode type.The transistor is sealed in a SOT143 envelope and features a low ON-resistance and low capacitances.The transistor is protected against excessive input voltages by integrated back-to-back diodes between gate and substrate.

Applications:

- analog and/or digital switch
- switch driver
- convertor
- chopper

PINNING

1 = substrate (b)
2 = source
3 = drain
4 = gate

Note

1. Drain and source are interchangeable

Marking code: M32

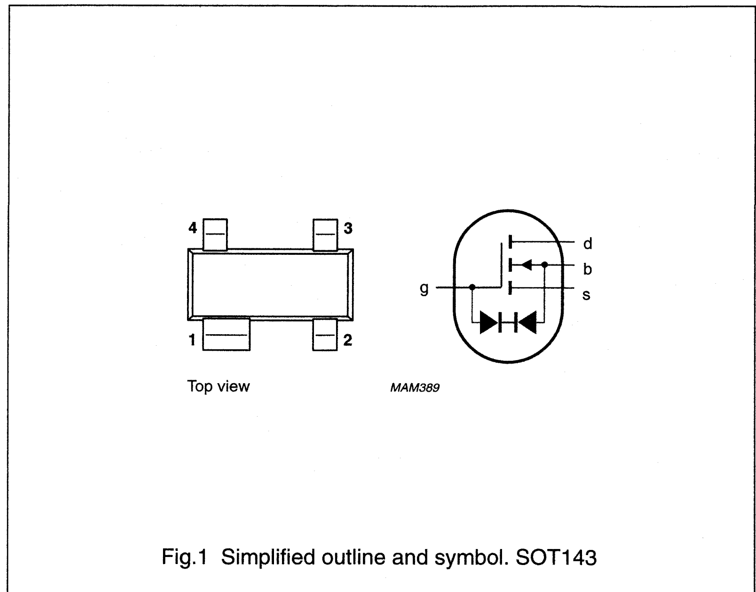


Fig.1 Simplified outline and symbol. SOT143

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	20	V
Gate-source voltage	V_{GS}	max.	+ 15	V
			− 40	V
Drain current (DC)	I_D	max.	50	mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	230	mW
Junction temperature	T_j	max.	125	°C
Drain-source ON-resistance				
V_{GS} = 10 V; V_{SB} = 0; I_D = 1 mA	R_{DSon}	max.	30	Ω
Feed-back capacitance				
V_{GS} = V_{BS} = −5 V; V_{DS} = 10 V; f = 1 MHz	C_{rss}	typ.	0.6	pF

MOSFET N-channel depletion switching transistor BSD22

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20	V
Source-drain voltage	V_{SD}	max.	20	V
Drain-substrate voltage	V_{DB}	max.	25	V
Source-substrate voltage	V_{SB}	max.	25	V
Gate-substrate voltage	V_{GB}	max.	± 15	V
Gate-source voltage	V_{GS}	max.	+ 15	V
			− 40	V
Drain current (DC)	I_D	max.	50	mA
Total power dissipation up to T_{amb} = 25 °C[1]	P_{tot}	max.	230	mW
Storage temperature range	T_{stg}		−65 to + 150	°C
Junction temperature	T_j	max.	125	°C

THERMAL RESISTANCE

From junction to ambient in free air[1]	$R_{th\ j\text{-}a}$	=	430	K/W

Note

1. Device mounted on a ceramic subtrate of 8 mm × 10 mm × 0.7 mm.

CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified

Drain-source breakdown voltage				
$V_{GS} = V_{BS} = -5$ V; I_S = 10 nA	$V_{(BR)DSX}$	min.	20	V
Source-drain breakdown voltage				
$V_{GD} = V_{BD} = -5$ V; I_D = 10 nA	$V_{(BR)SDX}$	min.	20	V
Drain-substrate breakdown voltage				
$V_{GB} = 0$; I_D = 10 nA; open source	$V_{(BR)DBO}$	min.	25	V
Source-substrate breakdown voltage				
$V_{GB} = 0$; I_S = 10 nA; open drain	$V_{(BR)SBO}$	min.	25	V
Drain-source leakage current				
$V_{GS} = V_{BS} = -5$ V; V_{DS} = 10 V	I_{DSoff}	typ.	1.0	nA
Source-drain leakage current				
$V_{GD} = V_{BD} = 5$ V; V_{SD} = 10 V	I_{SDoff}	typ.	1.0	nA
Gate-substrate leakage current				
$V_{DB} = V_{SB} = 0$; $V_{GB} = \pm 15$ V	I_{GBS}	max.	10	nA
Forward transconductance at f = 1 kHz				
V_{DS} = 10 V; V_{SB} = 0; I_D = 20 mA	g_{fs}	min.	10	mS
		typ.	15	mS
Gate-source cut-off voltage				
V_{DS} = 10 V; V_{SB} = 0; I_D = 10 μA	$-V_{(P)GS}$	max.	2.0	V

Drain-source ON-resistance				
I_D = 1 mA; V_{SB} = 0;				
V_{GS} = 5 V	R_{DSon}	typ.	25	Ω
		max.	50	Ω
V_{GS} = 10 V	R_{DSon}	typ.	15	Ω
		max.	30	Ω
Capacitances at f = 1 MHz				
V_{GS} = V_{BS} = −5 V; V_{DS} = 10 V				
Feed-back capacitance	C_{rss}	typ.	0.6	pF
Input capacitance	C_{iss}	typ.	1.5	pF
Output capacitance	C_{oss}	typ.	1.0	pF
Switching times (see Fig.3)				
V_{DD} = 10 V; V_i = −5 V to + 5 V	t_{on}	typ.	1.0	ns
	t_{off}	typ.	5.0	ns

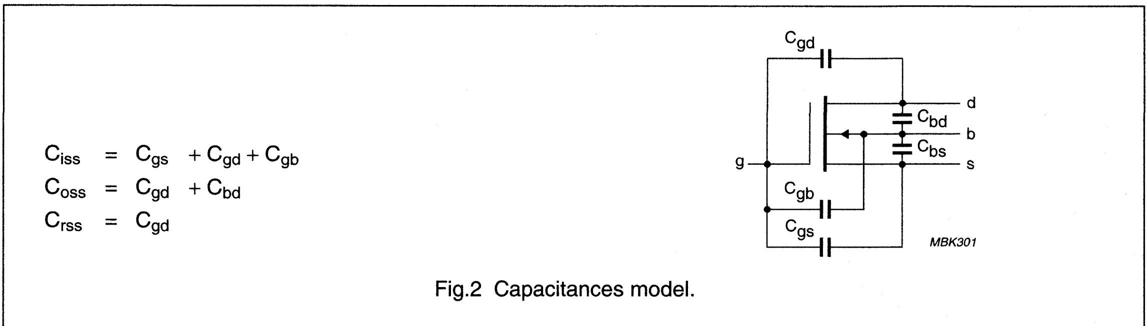


Fig.2 Capacitances model.

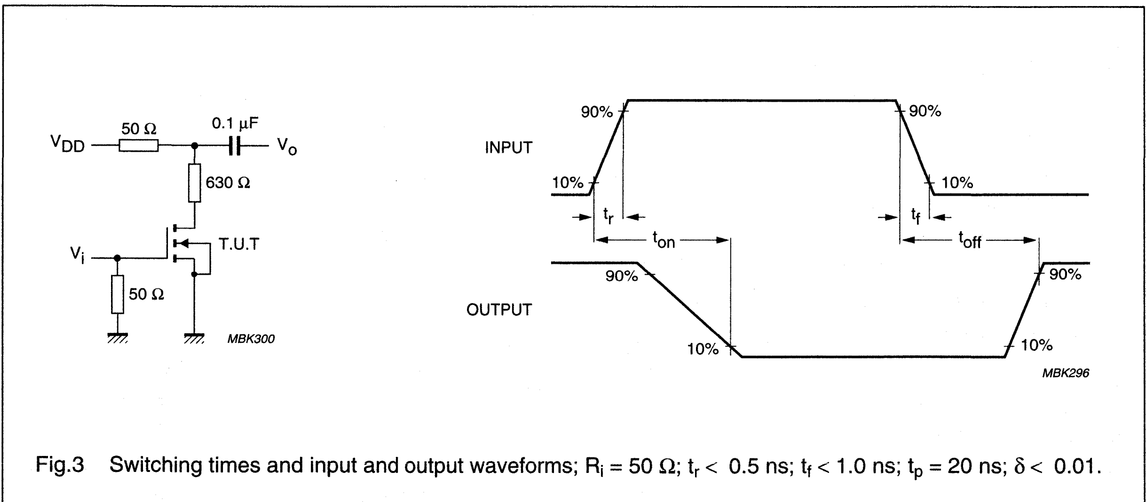


Fig.3 Switching times and input and output waveforms; R_i = 50 Ω; t_r < 0.5 ns; t_f < 1.0 ns; t_p = 20 ns; δ < 0.01.

N-channel FETs BSR56; BSR57; BSR58

DESCRIPTION

Symmetrical silicon n-channel depletion type junction field-effect transistors in a plastic microminiature envelope intended for application in thick and thin-film circuits. The transistors are intended for low-power, chopper or switching applications in industrial service.

PINNING

1 = drain
2 = source
3 = gate

Note

1. Drain and source are interchangeable.

Marking code

BSR56 = M4P
BSR57 = M5P
BSR58 = M6P

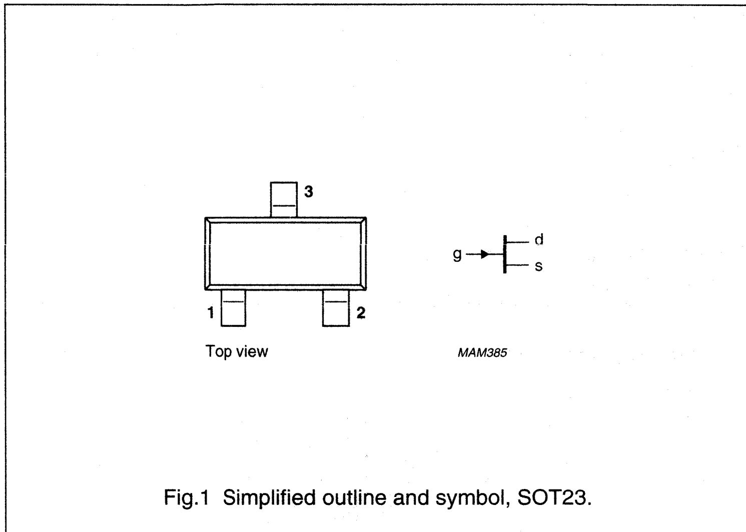


Fig.1 Simplified outline and symbol, SOT23.

QUICK REFERENCE DATA

			BSR56	BSR57	BSR58	
Drain-source voltage	$\pm V_{DS}$	max.	40	40	40	V
Total power dissipation up to T_{amb} = 40 °C	P_{tot}	max.	250	250	250	mW
Drain current						
V_{DS} = 15 V; V_{GS} = 0	I_{DSS}	>	50	20	8	mA
		<	–	100	80	mA
Gate-source cut-off voltage						
V_{DS} = 15 V; I_D = 0.5 nA	$-V_{(P)GS}$	>	4	2	0.8	V
		<	10	6	4	V
Drain-source resistance (on) at f = 1 kHz						
I_D = 0; V_{GS} = 0	$r_{ds\ on}$	<	25	40	60	Ω
Feedback capacitance at f = 1 MHz						
$-V_{GS}$ = 10 V; V_{DS} = 0	C_{rs}	<	5	5	5	pF
Turn-off time						
V_{DD} = 10 V; V_{GS} = 0						
I_D = 20 mA; $-V_{GSM}$ = 10 V	t_{off}	<	25	–	–	ns
I_D = 10 mA; $-V_{GSM}$ = 6 V	t_{off}	<	–	50	–	ns
I_D = 5 mA; $-V_{GSM}$ = 4 V	t_{off}	<	–	–	100	ns

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	40	V
Drain-gate voltage	V_{DGO}	max.	40	V
Gate-source voltage	$-V_{GSO}$	max.	40	V
Forward gate current	I_{GF}	max.	50	mA
Total power dissipation up to T_{amb} = 40 °C (note 1)	P_{tot}	max.	250	mW
Storage temperature range	T_{stg}		−65 to +150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	430	K/W

Notes

1. Mounted on a ceramic substrate of 8 mm × 10 mm × 0.7 mm.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Gate-source cut-off current				
V_{DS} = 0 V; $-V_{GS}$ = 20 V	$-I_{GSS}$	max.	1.0	nA
Drain cut-off current				
V_{DS} = 15 V; $-V_{GS}$ = 10 V	I_{DSX}	max.	1.0	nA

			BSR56	BSR57	BSR58	
Drain current						
V_{DS} = 15 V; V_{GS} = 0	I_{DSS}	>	50	20	8	mA
	I_{DSS}	<	–	100	80	mA
Gate-source breakdown voltage						
$-I_G$ = 1 μA; V_{DS} = 0	$-V_{(BR)GSS}$	>	40	40	40	V
Gate-source cut-off voltage						
I_D = 0,5 nA; V_{DS} = 15 V	$-V_{(P)GS}$	>	4	2	0.8	V
	$-V_{(P)GS}$	<	10	6	4	V
Drain-source voltage (on)						
I_D = 20 mA; V_{GS} = 0	V_{DSon}	<	750	–	–	mV
I_D = 10 mA; V_{GS} = 0	V_{DSon}	<	–	500	–	mV
I_D = 5 mA; V_{GS} = 0	V_{DSon}	<	–	–	400	mV
Drain-source resistance (on) at f = 1 kHz						
I_D = 0; V_{GS} = 0; T_a = 25 °C	$r_{ds\ on}$	<	25	40	60	Ω
Feedback capacitance at f = 1 MHz						
$-V_{GS}$ = 10 V; V_{DS} = 0	C_{rss}	<	5	5	5	pF

			BSR56	BSR57	BSR58	
Switching times						
V_{DD} = 10 V; V_{GS} = 0 Conditions I_D and $-V_{GSM}$	I_D	=	20	10	5	mA
	$-V_{GSM}$	=	10	6	4	V
Delay time	t_d	<	6	6	10	ns
Rise time	t_r	<	3	4	10	ns
Turn-off time	t_{off}	<	25	50	100	ns

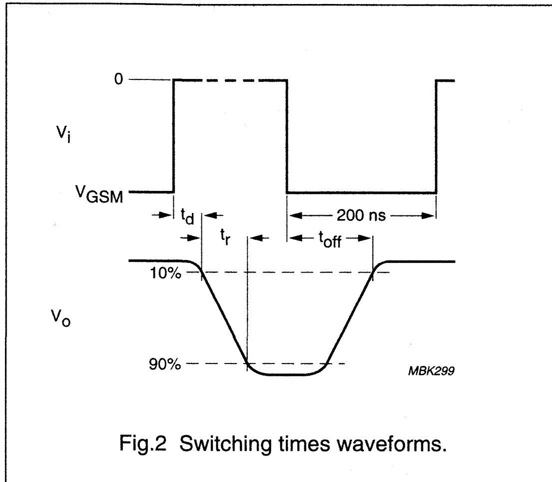


Fig.2 Switching times waveforms.

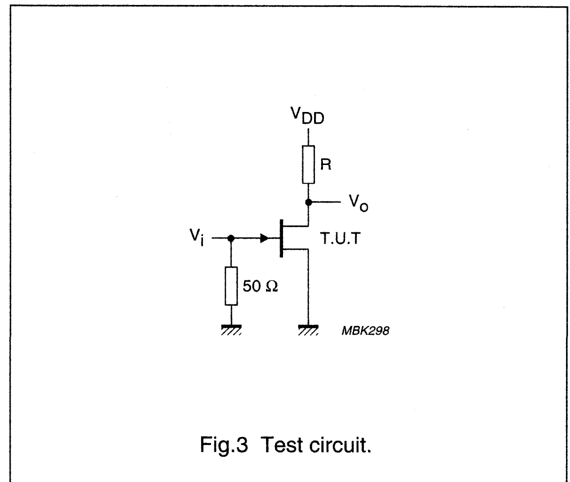


Fig.3 Test circuit.

BSR56; R = 464 Ω
BSR57; R = 953 Ω
BSR58; R = 1910 Ω

Pulse generator

$t_r = t_f \leq 1$ ns
δ = 0.02
Z_o = 50 Ω

Oscilloscope

$t_r \leq$ 0.75 ns
$R_i \geq$ 1 MΩ
$C_i \leq$ 2.5 pF

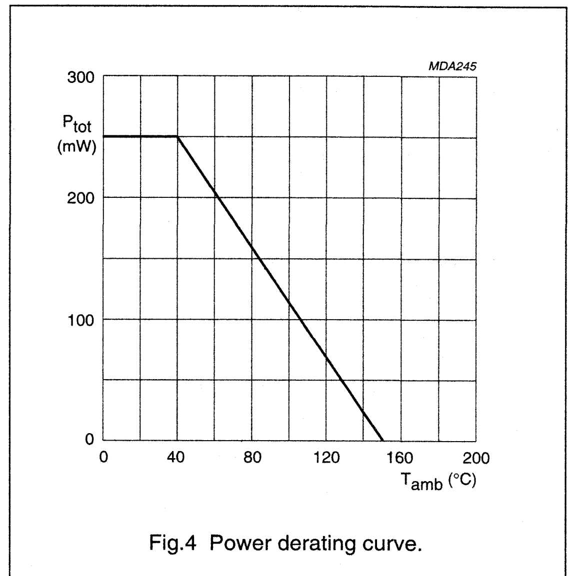


Fig.4 Power derating curve.

MOSFET N-channel enhancement switching transistor — BSS83

DESCRIPTION

Symmetrical insulated-gate silicon MOS field-effect transistor of the N-channel enhancement mode type. The transistor is sealed in a SOT143 envelope and features a low ON resistance and low capacitances. The transistor is protected against excessive input voltages by integrated back-to-back diodes between gate and substrate.

APPLICATIONS

- analog and/or digital switch
- switch driver

PINNING

1 = substrate (b)
2 = source
3 = drain
4 = gate

Note

1. Drain and source are interchangeable.

Marking code:

BSS83 = M74

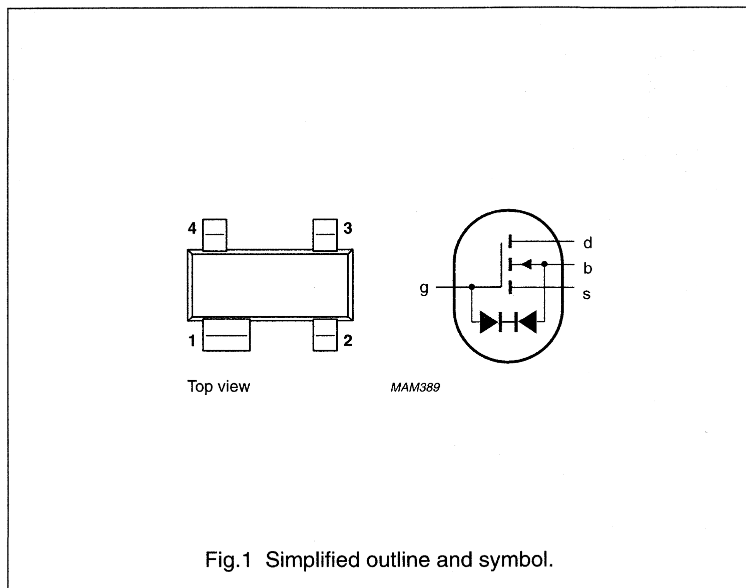


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

Parameter	Symbol		Value	Unit
Drain-source voltage	V_{DS}	max.	10	V
Source-drain voltage	V_{SD}	max.	10	V
Drain-substrate voltage	V_{DB}	max.	15	V
Source-substrate voltage	V_{SB}	max.	15	V
Drain current (DC)	I_D	max.	50	mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	230	mW
Gate-source threshold voltage				
$V_{DS} = V_{GS}$; $V_{SB} = 0$;	$V_{GS(th)}$	>	0.1	V
$I_D = 1\ \mu A$		<	2.0	V
Drain-source ON-resistance				
$V_{GS} = 10$ V; $V_{SB} = 0$; $I_D = 0.1$ mA	R_{DSon}	<	45	Ω
Feed-back capacitance				
$V_{GS} = V_{BS} = -15$ V;				
$V_{DS} = 10$ V; f = 1 MHz	C_{rss}	typ.	0.6	pF

MOSFET N-channel enhancement switching transistor BSS83

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	10	V
Source-drain voltage	V_{SD}	max.	10	V
Drain-substrate voltage	V_{DB}	max.	15	V
Source-substrate voltage	V_{SB}	max.	15	V
Drain current (DC)	I_D	max.	50	mA
Total power dissipation up to T_{amb} = 25 °C[1]	P_{tot}	max.	230	mW
Storage temperature range	T_{stg}		−65 to + 150	°C
Junction temperature	T_j	max.	125	°C

THERMAL RESISTANCE

From junction to ambient in free air[1]	$R_{th\ j\text{-}a}$	=	430	K/W

CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified

Parameter	Symbol		Value	Unit
Drain-source breakdown voltage				
$V_{GS} = V_{BS} = -5$ V; $I_D = 10$ nA	$V_{(BR)DSX}$	>	10	V
Source-drain breakdown voltage				
$V_{GD} = V_{BD} = -5$ V; $I_D = 10$ nA	$V_{(BR)SDX}$	>	10	V
Drain-substrate breakdown voltage				
$V_{GB} = 0$; $I_D = 10$ nA; open source	$V_{(BR)DBO}$	>	15	V
Source-substrate breakdown voltage				
$V_{GB} = 0$; $I_D = 10$ nA; open drain	$V_{(BR)SBO}$	>	15	V
Drain-source leakage current				
$V_{GS} = V_{BS} = -2$ V; $V_{DS} = 6,6$ V	I_{DSoff}	<	10	nA
Source-drain leakage current				
$V_{GD} = V_{BD} = -2$ V; $V_{SD} = 6,6$ V	I_{SDoff}	<	10	nA
Forward transconductance at f = 1 kHz				
$V_{DS} = 10$ V; $V_{SB} = 0$; $I_D = 20$ mA	g_{fs}	>	10	mS
		typ.	15	mS
Gate-source threshold voltage				
$V_{DS} = V_{GS}$; $V_{SB} = 0$; $I_D = 1$ µA	$V_{GS(th)}$	>	0,1	V
		<	2,0	V
Drain-source ON-resistance				
$I_D = 0,1$ mA;				
$V_{GS} = 5$ V; $V_{SB} = 0$	R_{DSon}	<	70	Ω
$V_{GS} = 10$ V; $V_{SB} = 0$	R_{DSon}	<	45	Ω
$V_{GS} = 3,2$ V; $V_{SB} = 6,8$ V (see Fig.4)	R_{DSon}	typ.	80	Ω
		<	120	Ω
Gate-substrate zener voltages				
$V_{DB} = V_{SB} = 0$; $-I_G = 10$ µA	$V_{Z(1)}$	>	12,5	V
$V_{DB} = V_{SB} = 0$; $+I_G = 10$ µA	$V_{Z(2)}$	>	12,5	V
Capacitances at f = 1 MHz				
$V_{GS} = V_{BS} = -15$ V; $V_{DS} = 10$ V				
Feed-back capacitance	C_{rss}	typ.	0,6	pF
Input capacitance	C_{iss}	typ.	1,5	pF
Output capacitance	C_{oss}	typ.	1,0	pF
Switching times (see Fig.2)				
$V_{DD} = 10$ V; $V_i = 5$ V	t_{on}	typ.	1,0	ns
	t_{off}	typ.	5,0	ns

Note

1. Device mounted on a ceramic substrate of 8 mm × 10 mm × 0,7 mm.

Pulse generator:

R_i	=	50 Ω
t_r	<	0,5 ns
t_f	<	1,0 ns
t_p	=	20 ns
δ	<	0,01

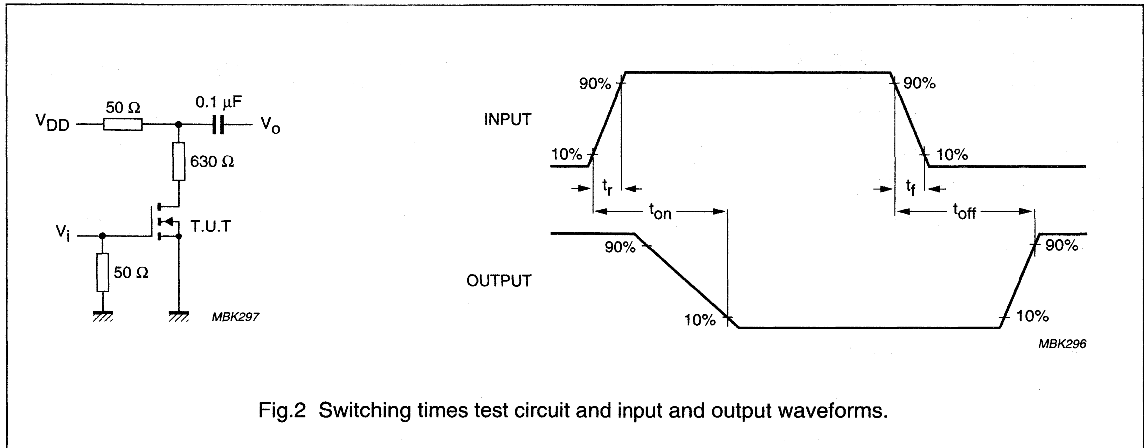
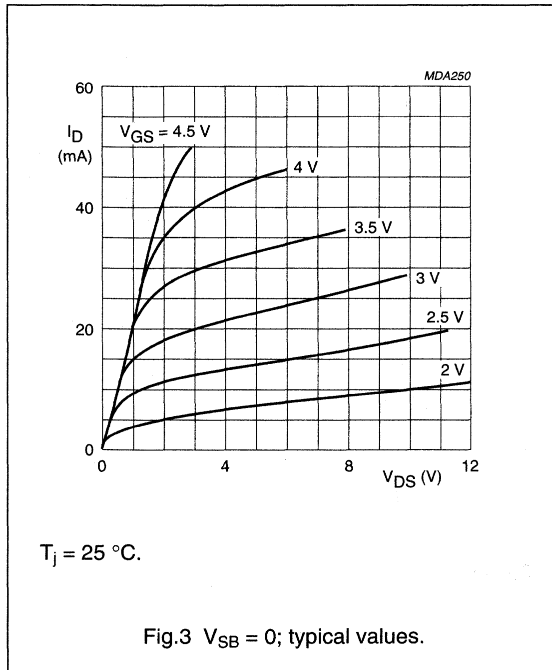
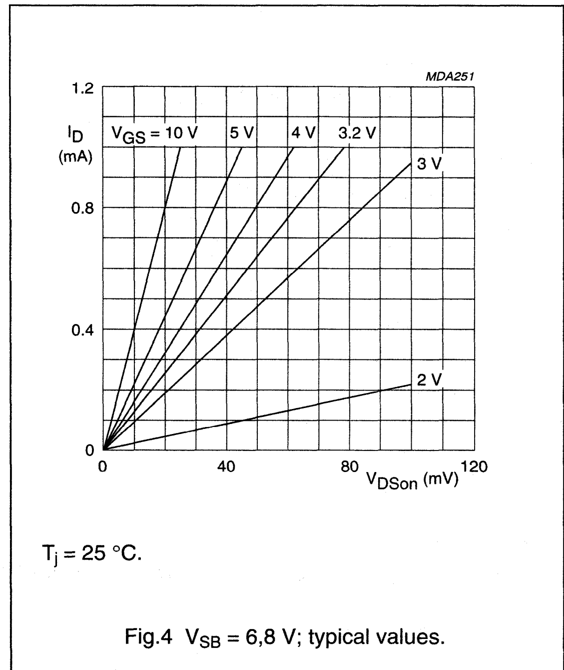


Fig.2 Switching times test circuit and input and output waveforms.



T_j = 25 °C.

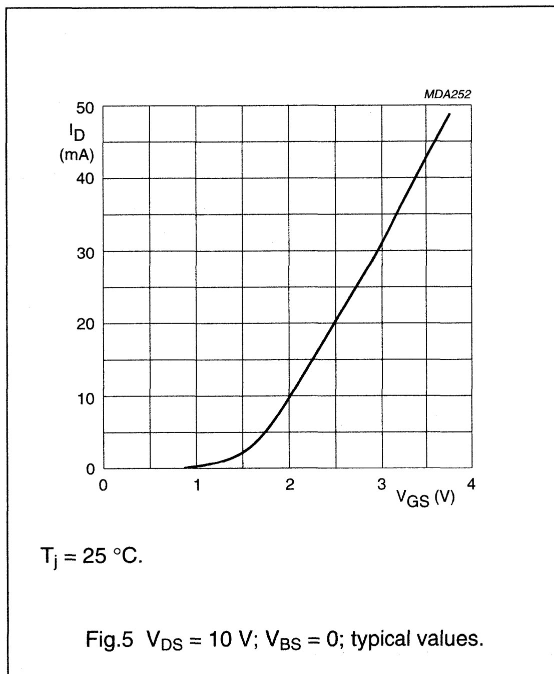
Fig.3 V_{SB} = 0; typical values.



T_j = 25 °C.

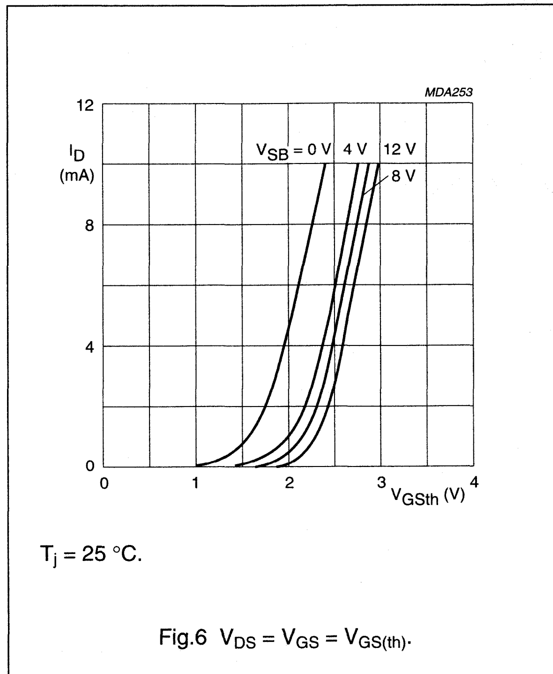
Fig.4 V_{SB} = 6,8 V; typical values.

MOSFET N-channel enhancement switching transistor BSS83



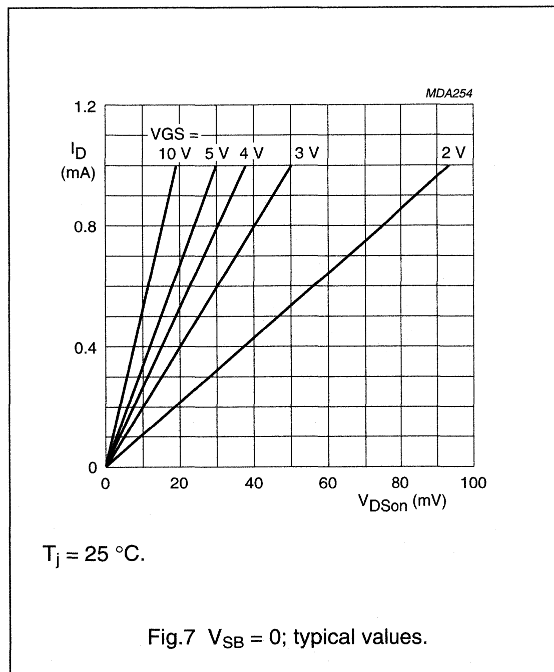
T_j = 25 °C.

Fig.5 V_{DS} = 10 V; V_{BS} = 0; typical values.



T_j = 25 °C.

Fig.6 V_{DS} = V_{GS} = $V_{GS(th)}$.



T_j = 25 °C.

Fig.7 V_{SB} = 0; typical values.

N-channel silicon junction FETs — J108; J109; J110

FEATURES

- High speed switching
- Interchangeability of drain and source connections
- Low R_{DSon} at zero gate voltage (<8 Ω for J108).

APPLICATIONS

- Analog switches
- Choppers and commutators.

DESCRIPTION

N-channel symmetrical silicon junction field-effect transistors in a TO-92 package.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING - TO-92

PIN	SYMBOL	DESCRIPTION
1	g	gate
2	s	source
3	d	drain

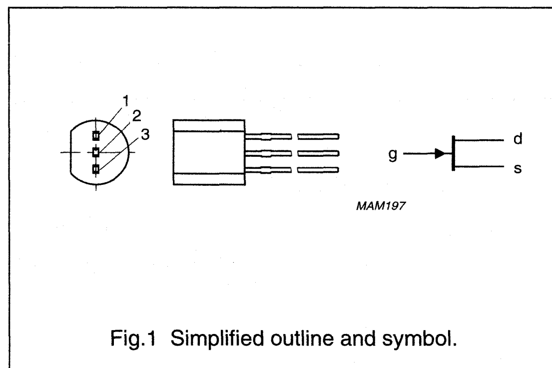


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	±25	V
V_{GSoff}	gate-source cut-off voltage	I_D = 1 μA; V_{DS} = 5 V			
	J108		−3	−10	V
	J109		−2	−6	V
	J110		−0.5	−4	V
I_{DSS}	drain current	V_{GS} = 0; V_{DS} = 5 V			
	J108		80	–	mA
	J109		40	–	mA
	J110		10	–	mA
P_{tot}	total power dissipation	up to T_{amb} = 50 °C	–	400	mW

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	±25	V
V_{GSO}	gate-source voltage	open drain	–	–25	V
V_{GDO}	gate-drain voltage	open source	–	–25	V
I_G	forward gate current (DC)		–	50	mA
P_{tot}	total power dissipation	up to T_{amb} = 50 °C	–	400	mW
T_{stg}	storage temperature		–65	150	°C
T_j	operating junction temperature		–	150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient	250	K/W

STATIC CHARACTERISTICS

T_j = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)GSS}$	gate-source breakdown voltage	I_G = –1 μA; V_{DS} = 0	–	–	–25	V
V_{GSoff}	gate-source cut-off voltage	I_D = 1 μA; V_{DS} = 5 V				V
	J108		–3	–	–10	V
	J109		–2	–	–6	V
	J110		–0.5	–	–4	V
I_{DSS}	drain current	V_{GS} = 0; V_{DS} = 15 V				
	J108		80	–	–	mA
	J109		40	–	–	mA
	J110		10	–	–	mA
I_{GSS}	gate leakage current	V_{GS} = –15 V; V_{DS} = 0	–	–	–3	nA
I_{DSX}	drain-source cut-off current	V_{GS} = –10 V; V_{DS} = 5 V	–	–	3	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 0; V_{DS} = 100 mV				
	J108		–	–	8	Ω
	J109		–	–	12	Ω
	J110		–	–	18	Ω

DYNAMIC CHARACTERISTICS

T_j = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
C_{is}	input capacitance	V_{DS} = 0; V_{GS} = −10 V; f = 1 MHz	15	30	pF
		V_{DS} = 0; V_{GS} = 0; f = 1 MHz; T_{amb} = 25 °C	50	85	pF
C_{rs}	reverse transfer capacitance	V_{DS} = 0; V_{GS} = −10 V; f = 1 MHz	8	15	pF
Switching times; see Fig.2					
t_d	delay time	note 1	2	–	ns
t_{on}	turn-on time		4	–	ns
t_s	storage time		4	–	ns
t_{off}	turn-off time		6	–	ns

Note

1. Test conditions for switching times are as follows:

   V_{DD} = 1.5 V; V_{GS} = 0 to V_{GSoff} (all types)

   V_{GSoff} = −12 V; R_L = 100 Ω (J108)

   V_{GSoff} = −7 V; R_L = 100 Ω (J109)

   V_{GSoff} = −5 V; R_L = 100 Ω (J110).

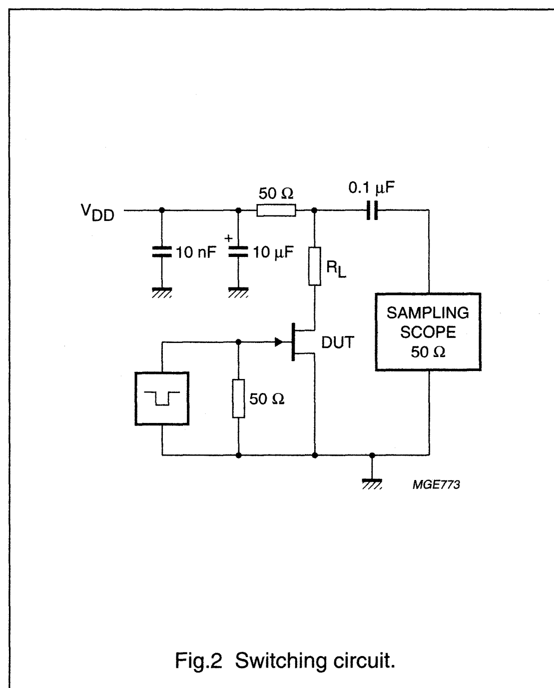


Fig.2 Switching circuit.

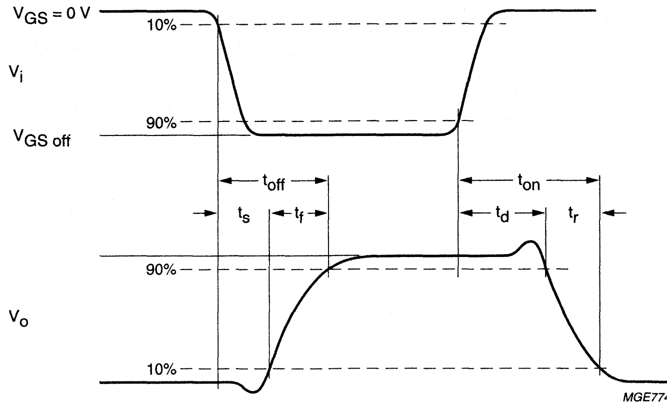


Fig.3 Input and output waveforms.

N-channel silicon field-effect transistors J111; J112; J113

DESCRIPTION

Symmetrical silicon n-channel junction FETs in plastic TO-92 envelopes. They are intended for applications such as analog switches, choppers, commutators etc.

FEATURES

- High speed switching
- Interchangeability of drain and source connections
- Low $R_{DS\ on}$ at zero gate voltage

PINNING

1 = gate

2 = source

3 = drain

Note: Drain and source are interchangeable.

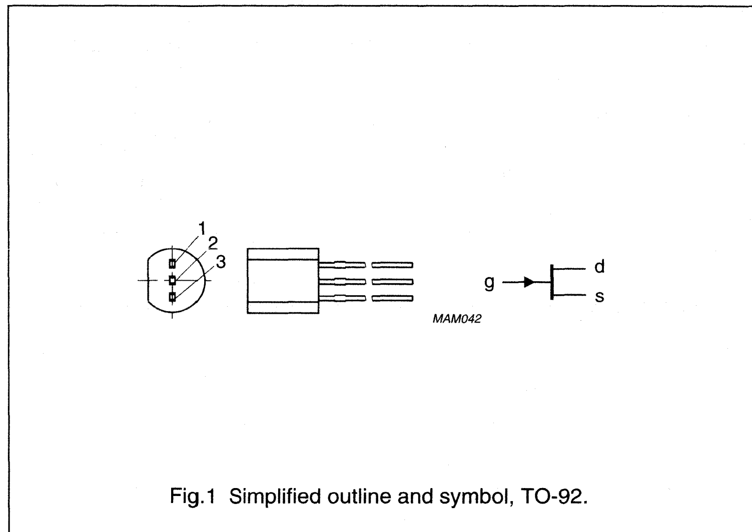


Fig.1 Simplified outline and symbol, TO-92.

QUICK REFERENCE DATA

			J111	J112	J113	
Drain-source voltage	$\pm V_{DS}$	max.	40	40	40	V
Drain current $V_{DS} = 15$ V; $V_{GS} = 0$	I_{DSS}	min.	20	5	2	mA
Total power dissipation up to $T_{amb} = 50$ °C	P_{tot}	max.	400	400	400	mW
Gate-source cut-off voltage $V_{DS} = 5$ V; $I_D = 1$ µA	$-V_{GS\ off}$	min.	3	1	0.5	V
		max.	10	5	3	V
Drain-source on-state resistance $V_{DS} = 0.1$ V; $V_{GS} = 0$	$R_{DS\ on}$	max.	30	50	100	Ω

N-channel silicon field-effect transistors J111; J112; J113

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	40	V
Gate-source voltage	$-V_{GSO}$	max.	40	V
Gate-drain voltage	$-V_{GDO}$	max.	40	V
Gate forward current (DC)	I_G	max.	50	mA
Total power dissipation up to T_{amb} = 50 °C	P_{tot}	max.	400	mW
Storage temperature range	T_{stg}		−65 to + 150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j\text{-}a}$	=	250	K/W

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

			J111	J112	J113	
Gate reverse current $-V_{GS}$ = 15 V; V_{DS} = 0	$-I_{GSS}$	max.	1	1	1	nA
Drain cut-off current V_{DS} = 5 V; $-V_{GS}$ = 10 V	$-I_{DSX}$	max.	1	1	1	nA
Drain saturation current V_{DS} = 15 V; V_{GS} = 0	I_{DSS}	min.	20	5	2	mA
Gate-source breakdown voltage $-I_G$ = 1 μA; V_{DS} = 0	$-V_{(BR)GSS}$	min.	40	40	40	V
Gate-source cut-off voltage V_{DS} = 5 V; I_D = 1 μA	$-V_{GS\ off}$	min.	3	1	0.5	V
		max.	10	5	3	V
Drain-source on-state resistance V_{DS} = 0.1 V; V_{GS} = 0	R_{DSon}	max.	30	50	100	Ω

DYNAMIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Input capacitance				
V_{DS} = 0; $-V_{GS}$ = 10 V; f = 1 MHz	C_{is}	typ.	6	pF
V_{DS} = $-V_{GS}$ = 0; f = 1 MHz	C_{is}	typ.	22	pF
		max.	28	pF
Feedback capacitance				
V_{DS} = 0; $-V_{GS}$ = 10 V; f = 1 MHz	C_{rs}	typ.	3	pF
Switching times				
test conditions				
V_{DD} = 10 V; V_{GS} = 0 to V_{GSoff}				
$-V_{GS\,off}$ = 12 V; R_L = 750 Ω for J111				
$-V_{GS\,off}$ = 7 V; R_L = 1550 Ω for J112				
$-V_{GS\,off}$ = 5 V; R_L = 3150 Ω for J113				
Rise time	t_r	typ.	6	ns
Turn-on time	t_{on}	typ.	13	ns
Fall time	t_f	typ.	15	ns
Turn-off time	t_{off}	typ.	35	ns

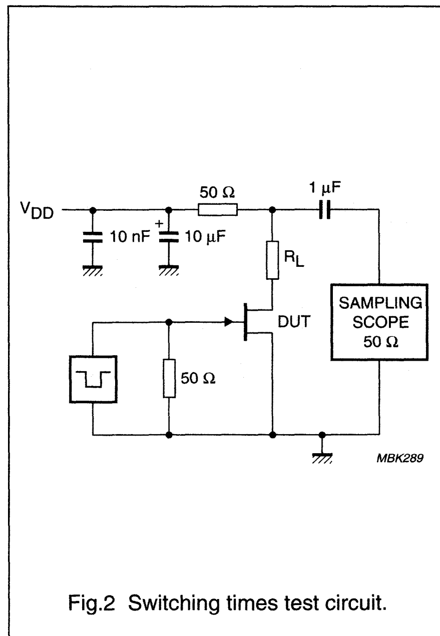


Fig.2 Switching times test circuit.

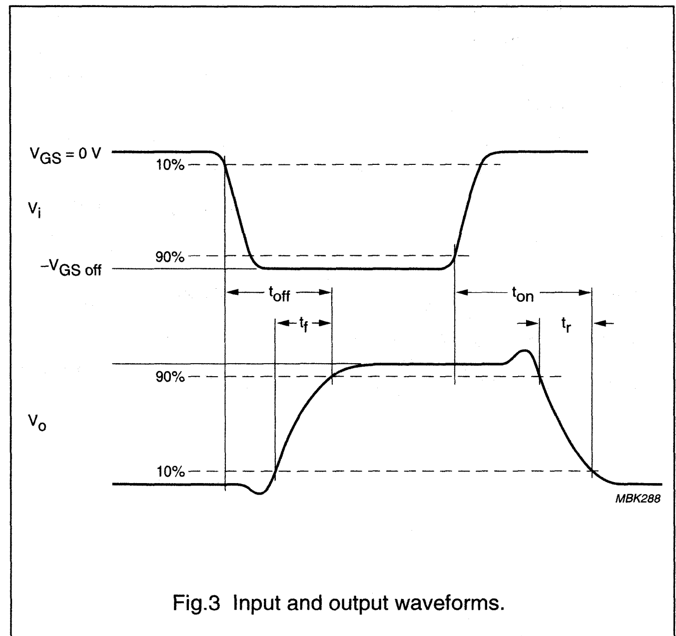


Fig.3 Input and output waveforms.

P-channel silicon field-effect transistors

J174; J175; J176; J177

DESCRIPTION

Silicon symmetrical p-channel junction FETs in a plastic TO-92 envelope and intended for application with analog switches, choppers, commutators etc.

A special feature is the interchangeability of the drain and source connections.

PINNING

1 = source

2 = gate

3 = drain

Note: Drain and source are interchangeable.

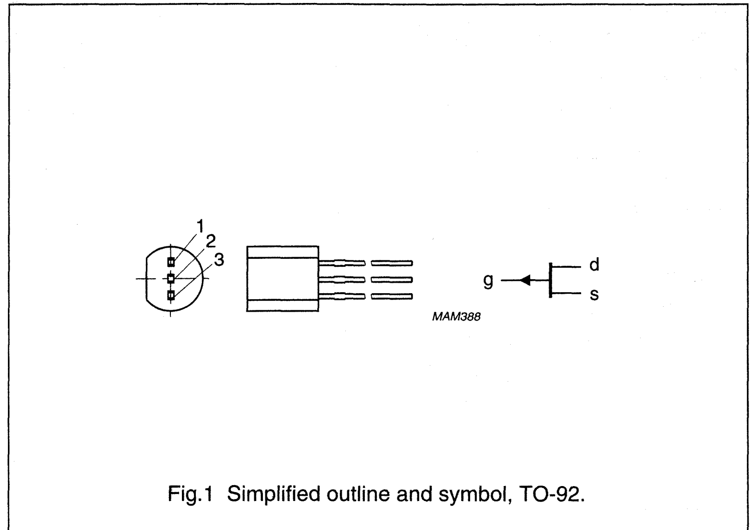


Fig.1 Simplified outline and symbol, TO-92.

QUICK REFERENCE DATA

Parameter	Symbol		Value	Unit
Drain-source voltage	$\pm V_{DS}$	max.	30	V
Gate-source voltage	V_{GSO}	max.	30	V
Gate current	$-I_G$	max.	50	mA
Total power dissipation up to T_{amb} = 50 °C	P_{tot}	max.	400	mW

Parameter	Symbol		J174	J175	J176	J177	Unit
Drain current $-V_{DS}$ = 15 V; V_{GS} = 0	$-I_{DSS}$	min.	20	7	2	1.5	mA
		max.	135	70	35	20	mA
Drain-source ON-resistance $-V_{DS}$ = 0.1 V; V_{GS} = 0	$R_{DS\,on}$	max.	85	125	250	300	Ω

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Parameter	Symbol		Value	Unit
Drain-source voltage	$\pm V_{DS}$	max.	30	V
Gate-source voltage	V_{GSO}	max.	30	V
Gate-drain voltage	V_{GDO}	max.	30	V
Gate current (DC)	$-I_G$	max.	50	mA
Total power dissipation up to T_{amb} = 50 °C	P_{tot}	max.	400	mW
Storage temperature range	T_{stg}		−65 to +150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

Parameter	Symbol		Value	Unit
From junction to ambient in free air	$R_{th\ j\text{-}a}$	=	250	K/W

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Parameter	Symbol		J174	J175	J176	J177	Unit
Gate cut-off current V_{GS} = 20 V; V_{DS} = 0	I_{GSS}	max.	1	1	1	1	nA
Drain cut-off current $-V_{DS}$ = 15 V; V_{GS} = 10 V	$-I_{DSX}$	max.	1	1	1	1	nA
Drain current $-V_{DS}$ = 15 V; V_{GS} = 10 V	$-I_{DSS}$	min.	20	7	2	1.5	mA
		max.	135	70	35	20	mA
Gate-source breakdown voltage I_G = 1 μA; V_{DS} = 0	$V_{(BR)GSS}$	min.	30	30	30	30	V
Gate-source cut-off voltage $-I_D$ = 10 nA; V_{DS} = −15 V	$V_{GS\ off}$	min.	5	3	1	0.8	V
		max.	10	6	4	2.25	V
Drain-source ON-resistance $-V_{DS}$ = 0.1 V; V_{GS} = 0	R_{DSon}	max.	85	125	250	300	Ω

DYNAMIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Input capacitance, f = 1 MHz							
V_{GS} = 10 V; V_{DS} = 0 V	C_{is}	typ.	8				pF
$V_{GS} = V_{DS}$ = 0	C_{is}	typ.	30				pF
Feedback capacitance, f = 1 MHz							
V_{GS} = 10 V; V_{DS} = 0 V	C_{rs}	typ.	4				pF
Switching times (see Fig.2 + 3)			**J174**	**J175**	**J176**	**J177**	
Delay time	t_d	typ.	2	5	15	20	ns
Rise time	t_r	typ.	5	10	20	25	ns
Turn-on time	t_{on}	typ.	7	15	35	45	ns
Storage time	t_s	typ.	5	10	15	20	ns
Fall time	t_f	typ.	10	20	20	25	ns
Turn-off time	t_{off}	typ.	15	30	35	45	ns
Test conditions:	$-V_{DD}$		10	6	6	6	V
	$V_{GS\,off}$		12	8	6	3	V
	R_L		560	1200	2000	2900	Ω
	$V_{GS\,on}$		0	0	0	0	V

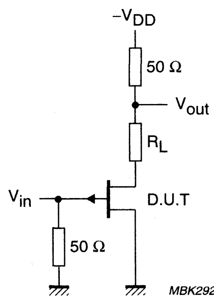


Fig.2 Switching times test circuit.

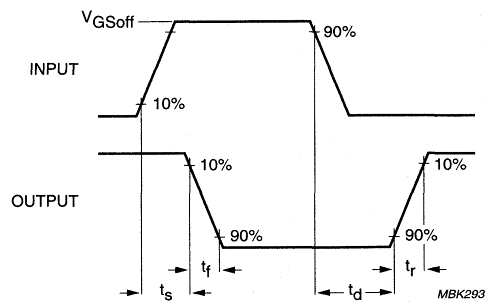


Fig.3 Input and output waveforms; $t_d + t_r = t_{on}$; $t_s + t_f = t_{off}$.

N-channel field-effect transistors J210; J211; J212

FEATURES

- High speed switching
- Interchangeability of drain and source connections
- High impedance.

APPLICATIONS

- Analog switches
- Choppers, multiplexers and commutators
- Audio amplifiers.

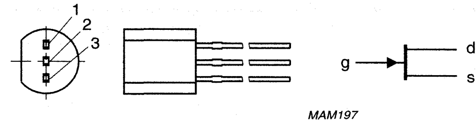
DESCRIPTION

N-channel symmetrical junction field-effect transistor in a TO-92 (SOT54) package.

CAUTION
This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling. For further information, refer to Philips specs.: SNW-EQ-608, SNW-FQ-302A and SNW-FQ-302B.

PINNING - TO-92 (SOT54)

PIN	SYMBOL	DESCRIPTION
1	g	gate
2	s	source
3	d	drain



Marking codes:
J210: J210.
J211: J211.
J212: J212.

Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	±25	V
V_{GSoff}	gate-source cut-off voltage	I_D = 1 nA; V_{DS} = 15 V			
	J210		−1	−3	V
	J211		−2.5	−4.5	V
	J212		−4	−6	V
I_{DSS}	drain current	V_{GS} = 0; V_{DS} = 15 V			
	J210		2	15	mA
	J211		7	20	mA
	J212		15	40	mA
P_{tot}	total power dissipation	$T_{amb} \leq 50$ °C	–	400	mW
$\|y_{fs}\|$	common-source transfer admittance	V_{GS} = 0; V_{DS} = 15 V			
	J210		4	12	mS
	J211		6	12	mS
	J212		7	12	mS

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	±25	V
V_{GSO}	gate-source voltage	open drain	–	–25	V
V_{DGO}	drain-gate voltage	open source	–	–25	V
I_G	forward gate current (DC)		–	10	mA
P_{tot}	total power dissipation	$T_{amb} \leq 50$ °C; note 1; see Fig.13	–	400	mW
T_{stg}	storage temperature		–65	150	°C
T_j	operating junction temperature		–	150	°C

Note

1. Device mounted on a printed-circuit board, maximum lead length 4 mm; mounting pad for the drain lead 10 mm^2.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient; note 1	250	K/W

Note

1. Device mounted on a printed-circuit board, maximum lead length 4 mm; mounting pad for the drain lead 10 mm^2.

STATIC CHARACTERISTICS

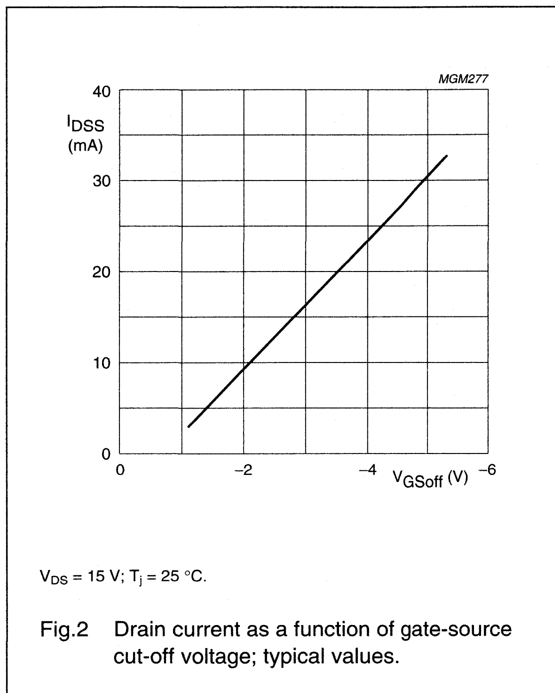
T_j = 25 °C.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{(BR)GSS}$	gate-source breakdown voltage	I_G = −1 μA; V_{DS} = 0	–	−25	V
V_{GSoff}	gate-source cut-off voltage	I_D = 1 nA; V_{DS} = 15 V			
	J210		−1	−3	V
	J211		−2.5	−4.5	V
	J212		−4	−6	V
V_{GSS}	gate-source forward voltage	I_G = 0; V_{DS} = 0	–	1	V
I_{DSS}	drain current	V_{GS} = 0; V_{DS} = 15 V			
	J10		2	15	mA
	J11		7	20	mA
	J12		15	40	mA
I_{GSS}	reverse gate leakage current	V_{GS} = −15 V; V_{DS} = 0	–	−100	pA
$\|y_{fs}\|$	common-source transfer admittance	V_{GS} = 0; V_{DS} = 15 V			
	J210		4	12	mS
	J211		6	12	mS
	J212		7	12	mS
$\|y_{os}\|$	common source output admittance	V_{GS} = 0; V_{DS} = 15 V			
	J210		–	150	μS
	J211		–	200	μS
	J212		–	200	μS

DYNAMIC CHARACTERISTICS

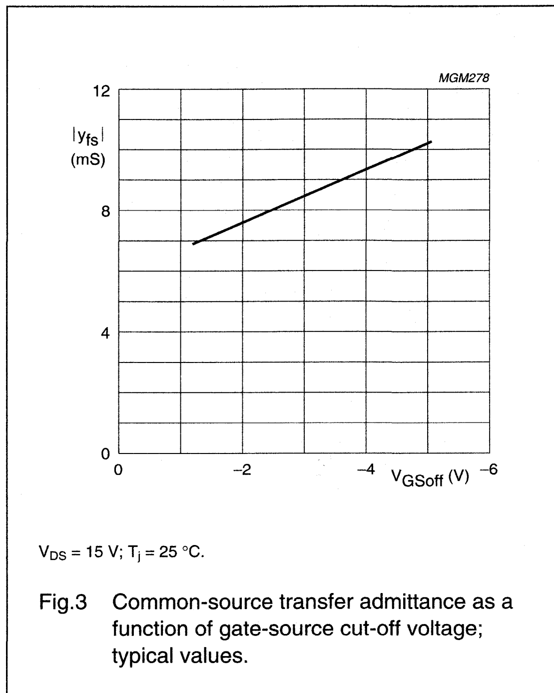
T_{amb} = 25 °C.

SYMBOL	PARAMETER	CONDITIONS	TYP.	UNIT
C_{is}	input capacitance	V_{DS} = 15 V; V_{GS} = −10 V; f = 1 MHz	2	pF
		V_{DS} = 15 V; V_{GS} = 0; f = 1 MHz	4	pF
C_{os}	output capacitance	V_{DS} = 15 V; V_{GS} = −10 V; f = 1 MHz	0.8	pF
		V_{DS} = 15 V; V_{GS} = 0; f = 1 MHz	2	pF
C_{rs}	feedback capacitance	V_{DS} = 15 V; V_{GS} = −10 V; f = 1 MHz	0.8	pF
		V_{DS} = 15 V; V_{GS} = 0; f = 1 MHz	0.9	pF
g_{is}	common source input conductance	V_{DS} = 15 V; V_{GS} = 0; f = 100 MHz	70	μS
		V_{DS} = 15 V; V_{GS} = 0; f = 450 MHz	1.1	mS
g_{fs}	common source transfer conductance	V_{DS} = 15 V; V_{GS} = 0; f = 100 MHz	7.5	mS
		V_{DS} = 15 V; V_{GS} = 0; f = 450 MHz	7.5	mS
g_{rs}	common source feedback conductance	V_{DS} = 15 V; V_{GS} = 0; f = 100 MHz	−8	μS
		V_{DS} = 15 V; V_{GS} = 0; f = 450 MHz	−90	μS
g_{os}	common source output conductance	V_{DS} = 15 V; V_{GS} = 0; f = 100 MHz	95	μS
		V_{DS} = 15 V; V_{GS} = 0; f = 450 MHz	200	μS
V_n	equivalent input noise voltage	V_{DS} = 15 V; V_{GS} = 0; f = 1 kHz	5	nV/√Hz



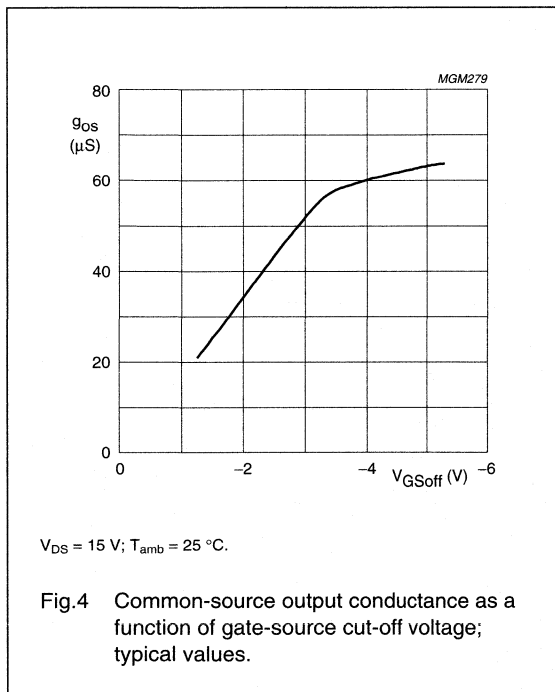
V_{DS} = 15 V; T_j = 25 °C.

Fig.2 Drain current as a function of gate-source cut-off voltage; typical values.



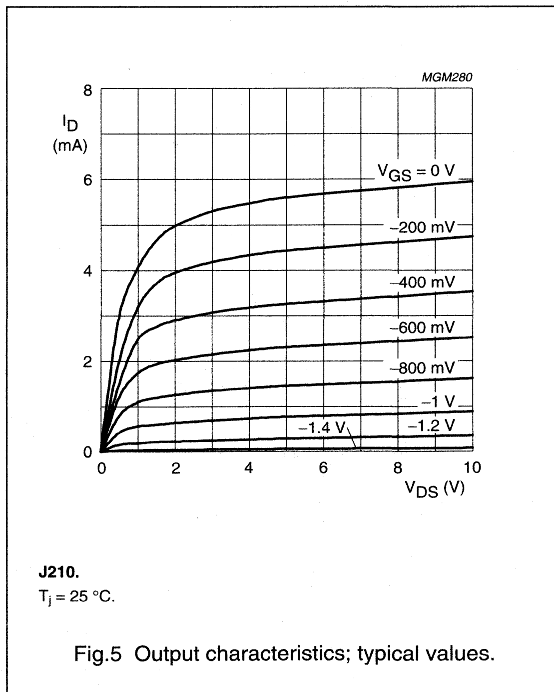
V_{DS} = 15 V; T_j = 25 °C.

Fig.3 Common-source transfer admittance as a function of gate-source cut-off voltage; typical values.



V_{DS} = 15 V; T_{amb} = 25 °C.

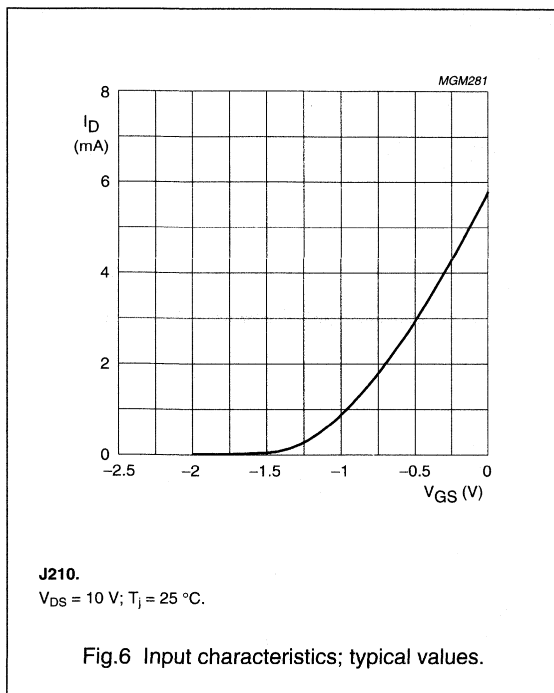
Fig.4 Common-source output conductance as a function of gate-source cut-off voltage; typical values.



J210.

T_j = 25 °C.

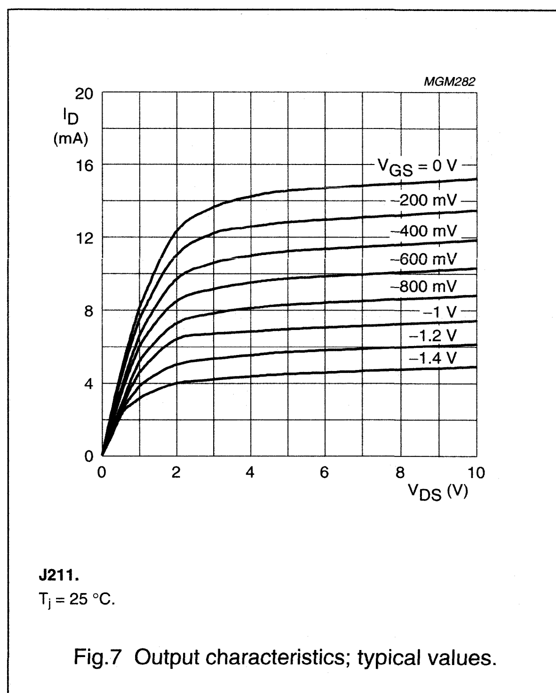
Fig.5 Output characteristics; typical values.



J210.

V_{DS} = 10 V; T_j = 25 °C.

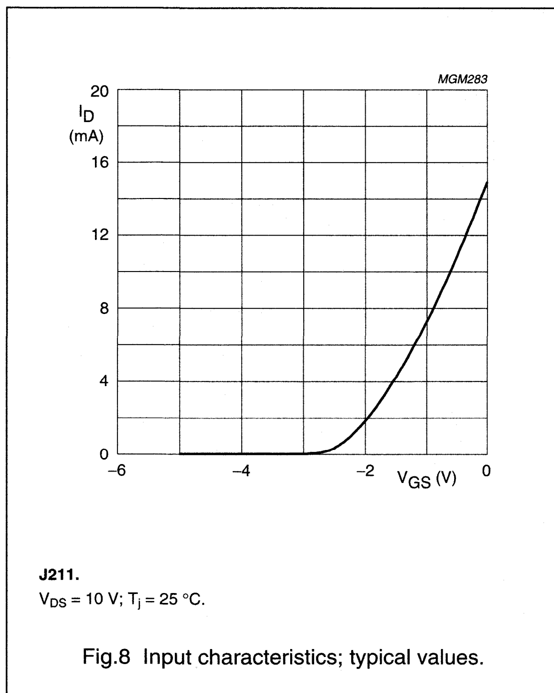
Fig.6 Input characteristics; typical values.



J211.

T_j = 25 °C.

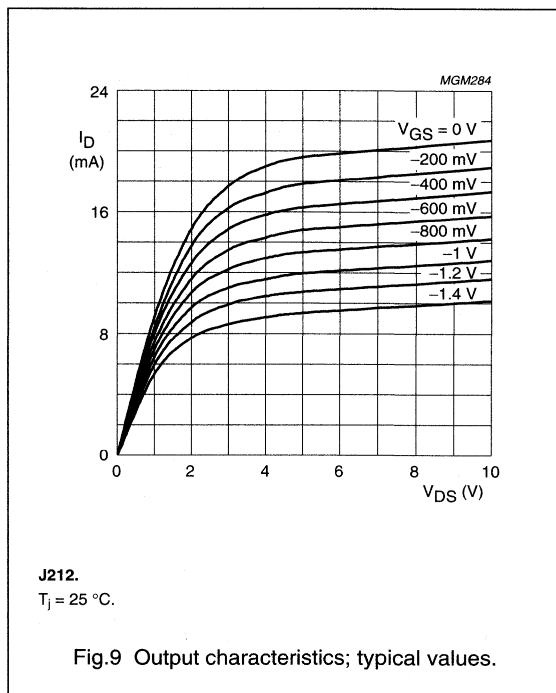
Fig.7 Output characteristics; typical values.



J211.

V_{DS} = 10 V; T_j = 25 °C.

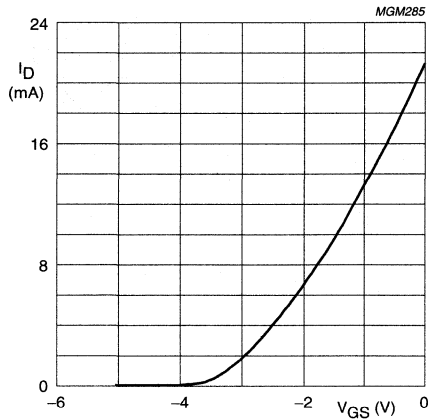
Fig.8 Input characteristics; typical values.



J212.

T_j = 25 °C.

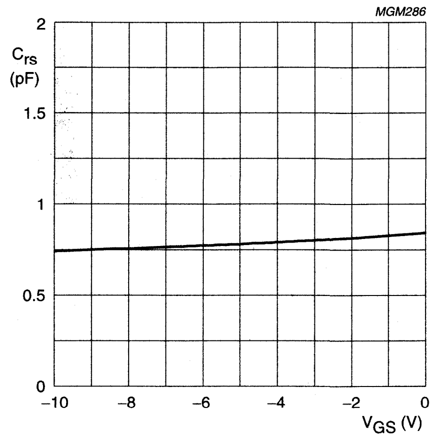
Fig.9 Output characteristics; typical values.



J212.

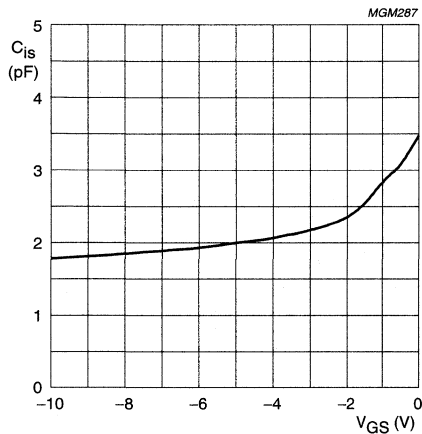
V_{DS} = 10 V; T_j = 25 °C.

Fig.10 Input characteristics; typical values.



V_{DS} = 15 V; f = 1 Mhz; T_{amb} = 25 °C.

Fig.11 Feedback capacitance as a function of gate-source voltage; typical values.



V_{DS} = 15 V; f = 1 Mhz; T_{amb} = 25 °C.

Fig.12 Input capacitance as a function of gate-source voltage; typical values.

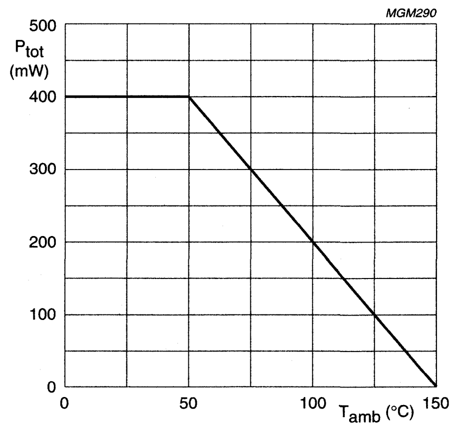
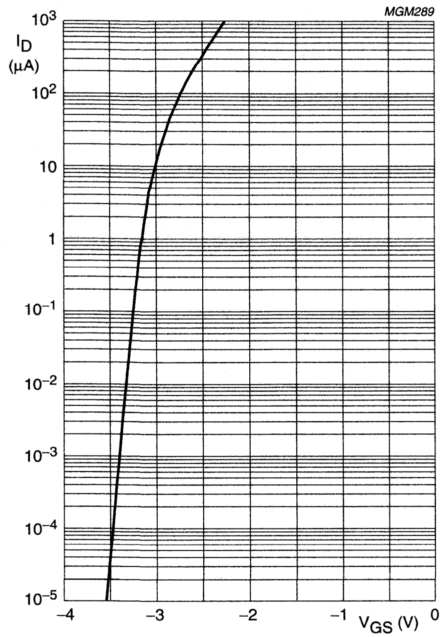
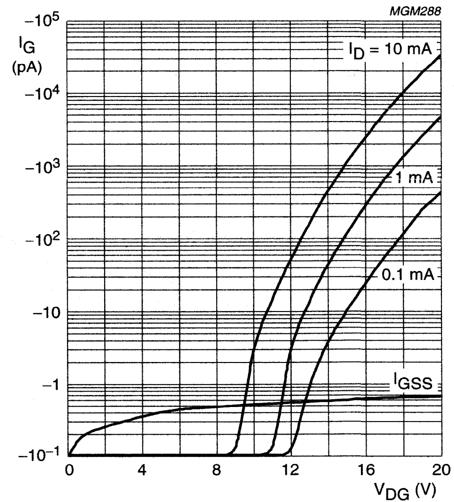


Fig.13 Power derating curve.



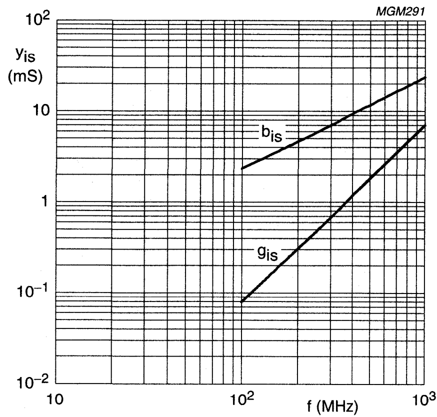
V_{DS} = 15 V; T_j = 25 °C.

Fig.14 Drain current as a function of gate-source voltage; typical values.



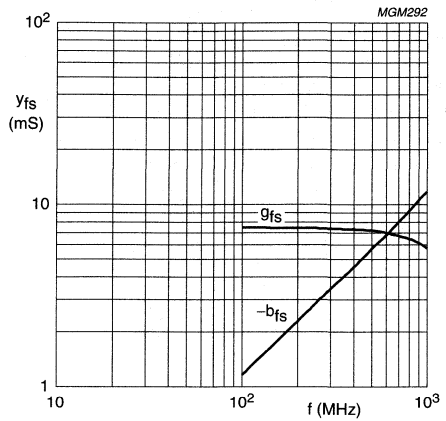
T_j = 25 °C.

Fig.15 Gate current as a function of drain-gate voltage; typical values.



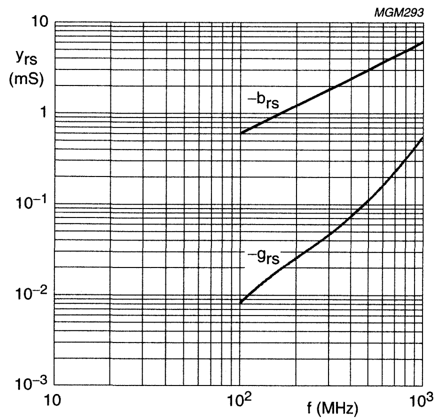
V_{DS} = 15 V; V_{GS} = 0; T_{amb} = 25 °C.

Fig.16 Common source input admittance as a function of frequency; typical values.



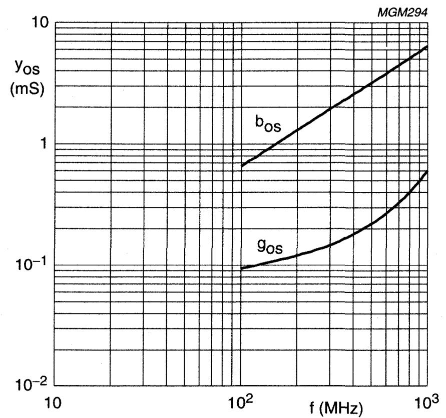
V_{DS} = 15 V; V_{GS} = 0; T_{amb} = 25 °C.

Fig.17 Common source transfer admittance as a function of frequency; typical values.



V_{DS} = 15 V; V_{GS} = 0; T_{amb} = 25 °C.

Fig.18 Common source reverse admittance as a function of frequency; typical values.



V_{DS} = 15 V; V_{GS} = 0; T_{amb} = 25 °C.

Fig.19 Common source output admittance as a function of frequency; typical values.

N-channel FETs

PMBF4391; PMBF4392; PMBF4393

DESCRIPTION

Symmetrical silicon n-channel depletion type junction field-effect transistors on a plastic microminiature envelope intended for application in thick and thin-film circuits. The transistors are intended for low-power chopper or switching applications in industry.

PINNING

1 = drain
2 = source
3 = gate

Note

1. Drain and source are interchangeable.

Marking code

PMBF4391 = p6J
PMBF4392 = p6K
PMBF4393 = p6G

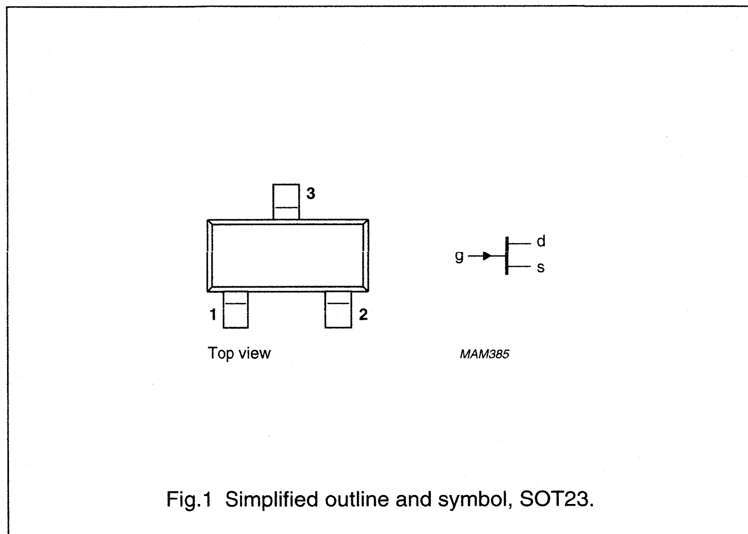


Fig.1 Simplified outline and symbol, SOT23.

QUICK REFERENCE DATA

			PMBF4391	PMBF4392	PMBF4393	
Drain-source voltage	$\pm V_{DS}$	max.	40	40	40	V
Drain current						
$V_{DS} = 20$ V; $V_{GS} = 0$	I_{DSS}	>	50	25	5	mA
Gate-source cut-off voltage						
$V_{DS} = 20$ V; $I_D = 1$ nA	$-V_{(P)GS}$	>	4	2	0.5	V
		<	10	5	3	V
Drain-source resistance (on) at f = 1 kHz						
$I_D = 0$; $V_{GS} = 0$	$R_{ds\ on}$	<	30	60	100	Ω
Feedback capacitance at f = 1 MHz						
$-V_{GS} = 12$ V; $V_{DS} = 0$	C_{rs}	<	3.5	3.5	3.5	pF
Turn-off time						
$V_{DD} = 10$ V; $V_{GS} = 0$						
$I_D = 12$ mA; $-V_{GSM} = 12$ V	t_{off}	<	20	–	–	ns
$I_D = 6$ mA; $-V_{GSM} = 7$ V	t_{off}	<	–	35	–	ns
$I_D = 3$ mA; $-V_{GSM} = 5$ V	t_{off}	<	–	–	50	ns

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Parameter	Symbol		Value	Unit
Drain-source voltage	$\pm V_{DS}$	max.	40	V
Drain-gate voltage	V_{DGO}	max.	40	V
Gate-source voltage	$-V_{GSO}$	max.	40	V
Gate current (DC)	I_G	max.	50	mA
Total power dissipation up to T_{amb} = 40 °C (1)	P_{tot}	max.	250	mW
Storage temperature range	T_{stg}		−65 to + 150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

Parameter	Symbol		Value	Unit
From junction to ambient(1)	$R_{th\ j\text{-}a}$	=	430	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Parameter	Symbol		Value	Unit
Gate-source voltage				
I_G = 1 mA; V_{DS} = 0	V_{GSon}	<	1	V
Gate-source cut-off current				
V_{DS} = 0 V; $-V_{GS}$ = 20 V	$-I_{GSS}$	<	0.1	nA
V_{DS} = 0 V; $-V_{GS}$ = 20 V; T_{amb} = 150 °C	$-I_{GSS}$	<	0.2	μA

Parameter	Symbol		PMBF4391	PMBF4392	PMBF4393	Unit
Drain current V_{DS} = 20 V; V_{GS} = 0	I_{DSS}	>	50	25	5	mA
		<	150	75	30	mA
Gate-source breakdown voltage $-I_G$ = 1 μA; V_{DS} = 0	$-V_{(BR)GSS}$	>	40	40	40	V
Gate-source cut-off voltage I_D = 1 nA; V_{DS} = 20 V	$-V_{(P)GS}$	>	4	2	0.5	V
		<	10	5	3	V
Drain-source voltage (on)						
I_D = 12 mA; V_{GS} = 0	V_{DSon}	<	0.4	–	–	V
I_D = 6 mA; V_{GS} = 0	V_{DSon}	<		0.4	–	V
I_D = 3 mA; V_{GS} = 0	V_{DSon}	<	–	–	0.4	V
Drain-source resistance (on)						
I_D = 0; V_{GS} = 0; f = 1 kHz; T_{amb} = 25 °C	$r_{ds\ on}$	<	30	–	100	Ω
Drain cut-off current						
$-V_{GS}$ = 12 V; V_{DS} = 20 V	I_{DSX}	<	0.1	–	–	nA
$-V_{GS}$ = 7 V; V_{DS} = 20 V	I_{DSX}	<	–	0.1	–	nA
$-V_{GS}$ = 5 V; V_{DS} = 20 V	I_{DSX}	<	–	–	0.1	nA
$-V_{GS}$ = 12 V; V_{DS} = 20 V; T_{amb} = 150 °C	I_{DSX}	<	0.2	–	–	μA
$-V_{GS}$ = 7 V; V_{DS} = 20 V; T_{amb} = 150 °C	I_{DSX}	<	–	0.2	–	μA
$-V_{GS}$ = 5 V; V_{DS} = 20 V; T_{amb} = 150 °C	I_{DSX}	<	–	–	0.2	μA

y-parameters (common source)					
V_{DS} = 20 V; V_{GS} = 0; f = 1 MHz; T_{amb} = 25 °C			**PMBF4391**	**PMBF4392**	**PMBF4393**
Input capacitance	C_{is}	<	14	14	14 pF
Feedback capacitance					
$-V_{GS}$ = 12 V ; V_{DS} = 0	C_{rs}	<	3.5	–	– pF
$-V_{GS}$ = 7 V ; V_{DS} = 0	C_{rs}	<	–	3.5	– pF
$-V_{GS}$ = 5 V ; V_{DS} = 0	C_{rs}	<	–	–	3.5 pF
Switching times					
V_{DD} = 10 V ; V_{DS} = 0					
Conditions I_D and $-V_{GSoff}$	I_D	=	12	6	3 mA
	$-V_{GS\,off}$	=	12	7	5 V
	R_L	=	750	1550	3150 Ω
Rise time	t_r	<	5	5	5 ns
Turn on time	t_{on}	<	15	15	15 ns
Fall time	t_f	<	15	20	30 ns
Turn off time	t_{off}	<	20	35	50 ns

Note

1. Mounted on a ceramic substrate of 8 mm × 10 mm × 0,7 mm.

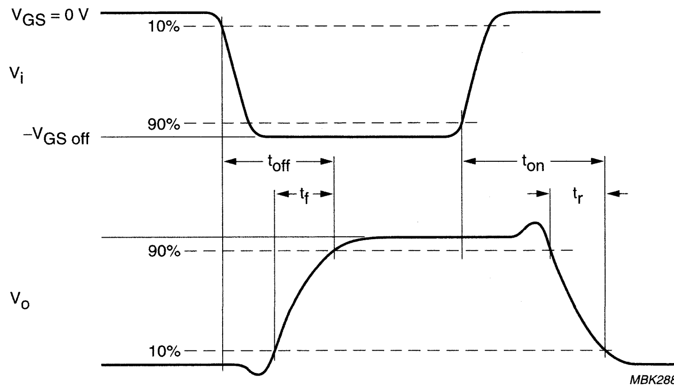


Fig.2 Switching times waveforms.

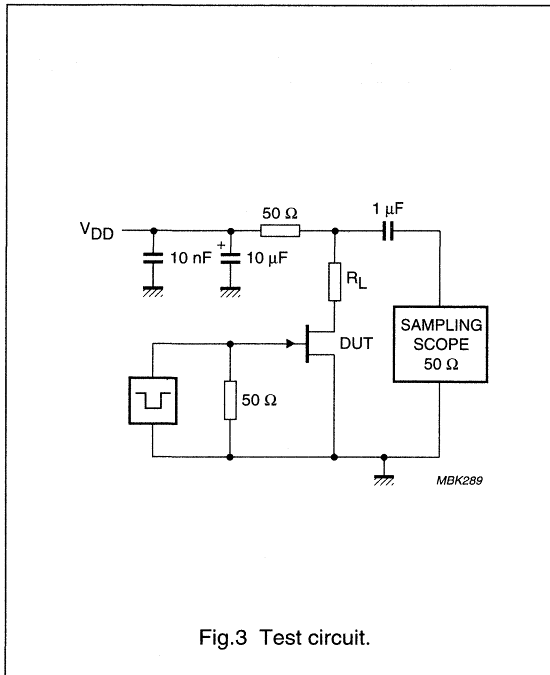


Fig.3 Test circuit.

Pulse generator:

t_r	<	0.5	ns
t_f	<	0.5	ns
t_p	=	100	μs
δ	=	0.01	

Oscilloscope:

R_i	=	50	Ω

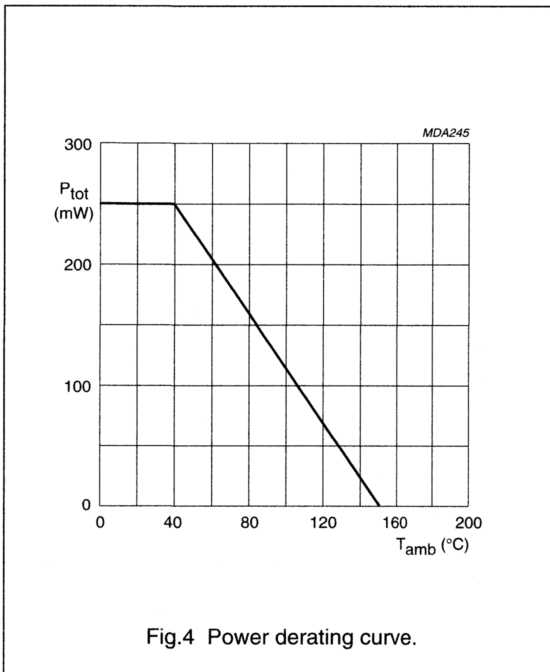


Fig.4 Power derating curve.

N-channel field-effect transistor PMBF4416; PMBF4416A

FEATURES

- Low noise
- Interchangeability of drain and source connections
- High gain.

DESCRIPTION

N-channel symmetrical silicon junction FETs in a surface-mountable SOT23 envelope. These devices are intended for use in VHF/UHF amplifiers, oscillators and mixers.

PINNING - SOT23

PIN	DESCRIPTION
1	source
2	drain
3	gate

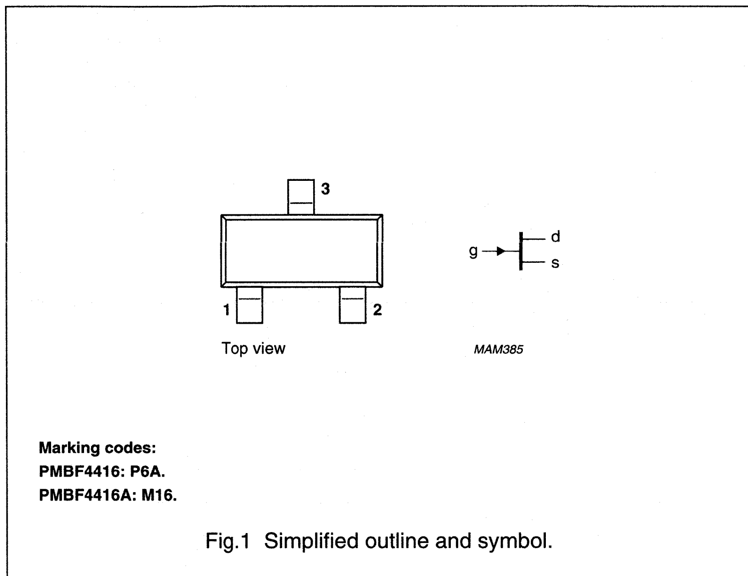


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage				
	PMBF4416		–	30	V
	PMBF4416A		–	35	V
I_{DSS}	drain-source current	V_{DS} = 15 V; V_{GS} = 0	5	15	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C	–	250	mW
$V_{GS(off)}$	gate-source cut-off voltage	V_{DS} = 15 V; I_D = 1 nA			
	PMBF4416		–	–6	V
	PMBF4416A		–2.5	–6	V
$\lvert Y_{fs} \rvert$	common-source transfer admittance	V_{DS} = 15 V; V_{GS} = 0; f = 1 kHz	4.5	7.5	mS

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage				
	PMBF4416		–	30	V
	PMBF4416A		–	35	V
V_{GSO}	gate-source voltage				
	PMBF4416		–	–30	V
	PMBF4416A		–	–35	V
V_{GDO}	gate-drain voltage				
	PMBF4416		–	–30	V
	PMBF4416A		–	–35	V
I_G	DC forward gate current		–	10	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C (note 1)	–	250	mW
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j-a}$	from junction to ambient (note 1)	500 K/W

Note

1. Mounted on an FR4 printed-circuit board.

STATIC CHARACTERISTICS

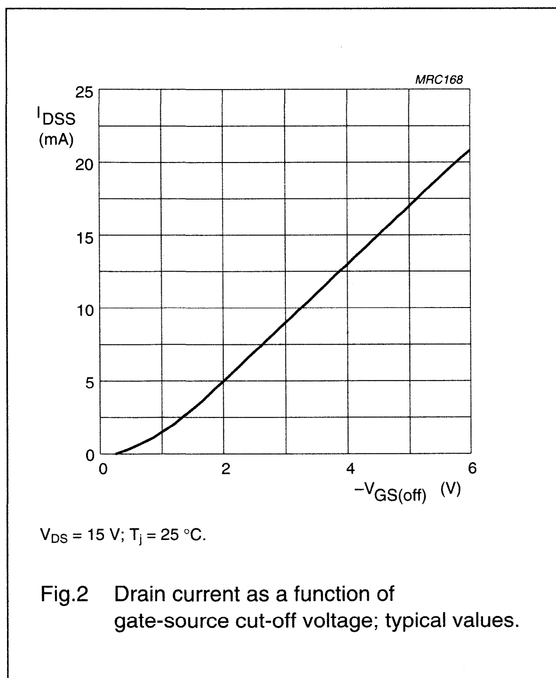
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{(BR)GSS}$	gate-source breakdown voltage	V_{DS} = 0; I_G = –1 μA			
	PMBF4416		–30	–	V
	PMBF4416A		–35	–	V
I_{GSS}	reverse gate leakage current	V_{DS} = 0; V_{GS} = –15 V	–	1	nA
I_{DSS}	drain current	V_{DS} = 15 V; V_{GS} = 0	5	15	mA
V_{GSS}	gate-source forward voltage	V_{DS} = 0; I_G = 1 mA	–	1	V
$V_{GS(off)}$	gate-source cut-off voltage	V_{DS} = 15 V; I_D = 1 nA			
	PMBF4416		–	–6	V
	PMBF4416A		–2.5	–6	V
$\|Y_{fs}\|$	common source transfer admittance	V_{DS} = 15 V; V_{GS} = 0	4.5	7.5	mS
$\|Y_{os}\|$	common source output admittance	V_{DS} = 15 V; V_{GS} = 0			
	PMBF4416		–	50	μS
	PMBF4416A		–	50	μS

DYNAMIC CHARACTERISTICS

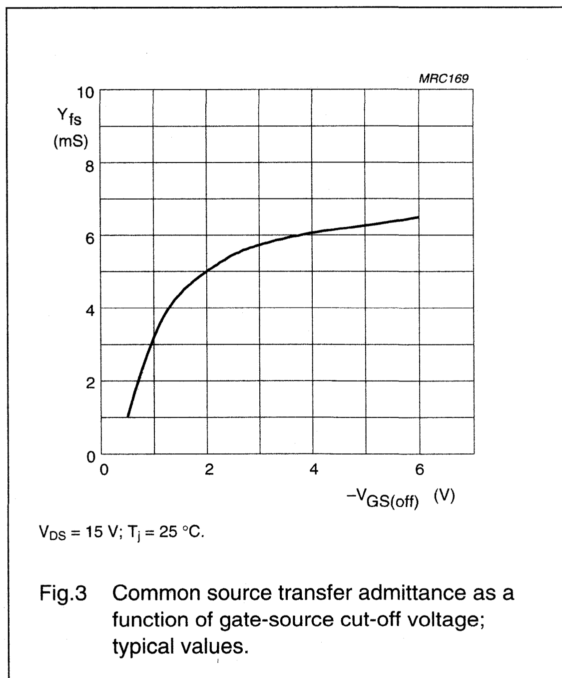
$T_j = 25$ °C; $V_{DS} = 15$ V; $V_{GS} = 0$.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_{is}	input capacitance	f = 1 MHz	–	–	4	pF
C_{os}	output capacitance	f = 1 MHz	–	–	2	pF
C_{rs}	feedback capacitance	f = 1 MHz	–	–	0.8	pF
g_{is}	common source input conductance	f = 100 MHz	–	–	100	μS
		f = 400 MHz	–	–	1	mS
g_{fs}	common source transfer conductance	f = 100 MHz	–	5.2	–	mS
		f = 400 MHz	4	5	–	mS
g_{rs}	common source feedback conductance	f = 100 MHz	–	–8	–	μS
		f = 400 MHz	–	–100	–	μS
g_{os}	common source output conductance	f = 100 MHz	–	–	75	μS
		f = 400 MHz	–	–	100	μS
V_n	equivalent input noise voltage	f = 100 Hz	–	5	–	nV/√Hz



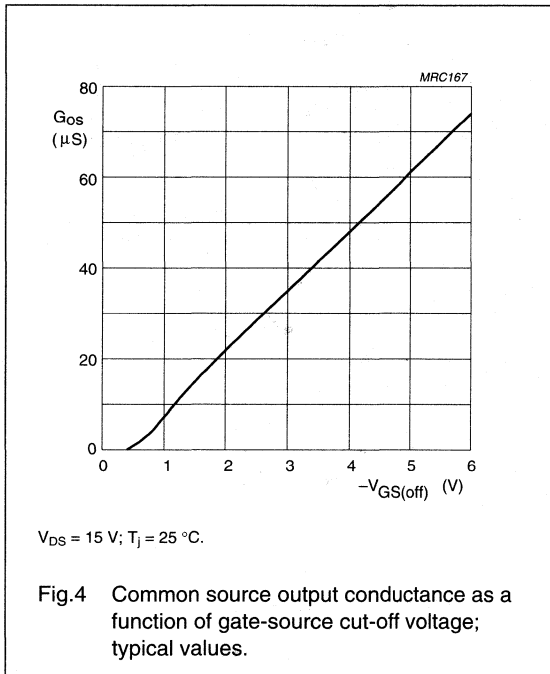
$V_{DS} = 15$ V; $T_j = 25$ °C.

Fig.2 Drain current as a function of gate-source cut-off voltage; typical values.



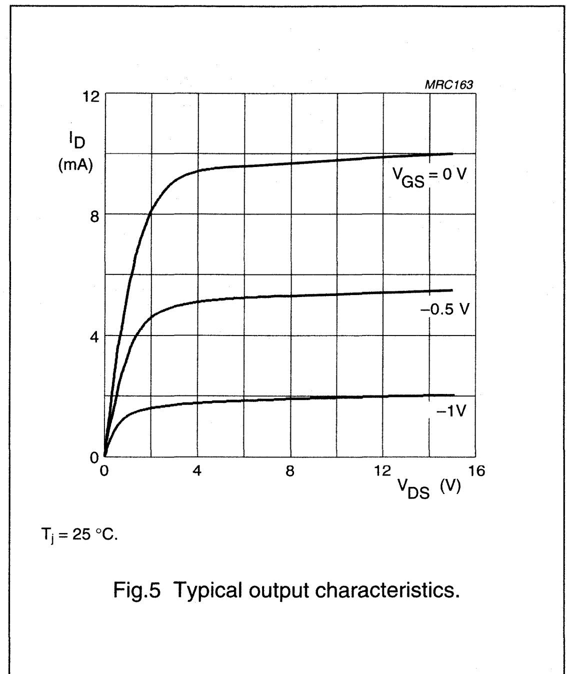
$V_{DS} = 15$ V; $T_j = 25$ °C.

Fig.3 Common source transfer admittance as a function of gate-source cut-off voltage; typical values.



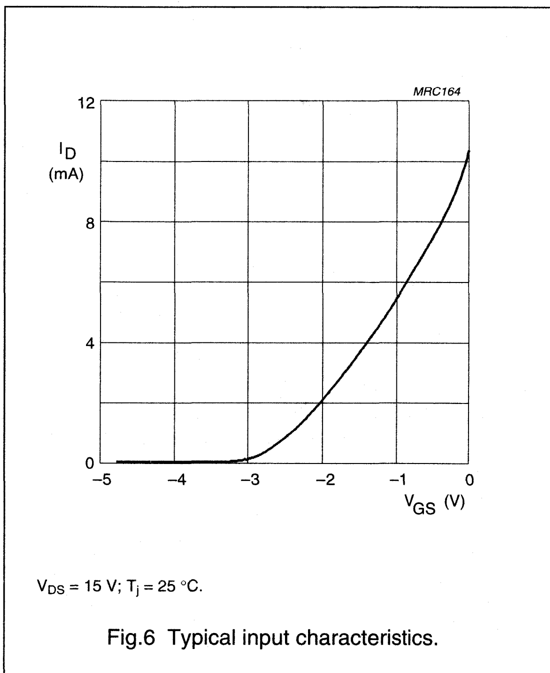
V_{DS} = 15 V; T_j = 25 °C.

Fig.4 Common source output conductance as a function of gate-source cut-off voltage; typical values.



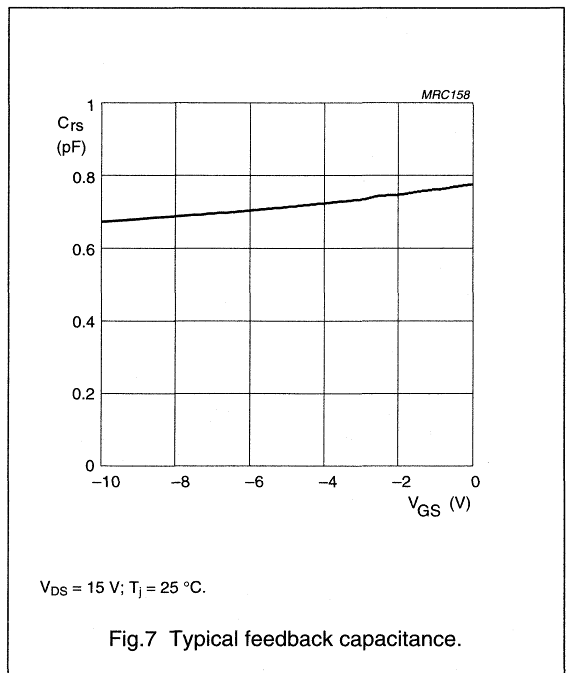
T_j = 25 °C.

Fig.5 Typical output characteristics.



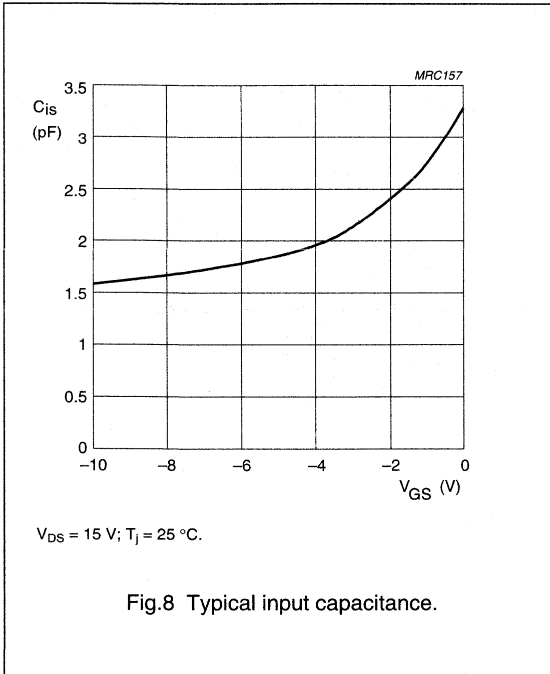
V_{DS} = 15 V; T_j = 25 °C.

Fig.6 Typical input characteristics.



V_{DS} = 15 V; T_j = 25 °C.

Fig.7 Typical feedback capacitance.



V_{DS} = 15 V; T_j = 25 °C.

Fig.8 Typical input capacitance.

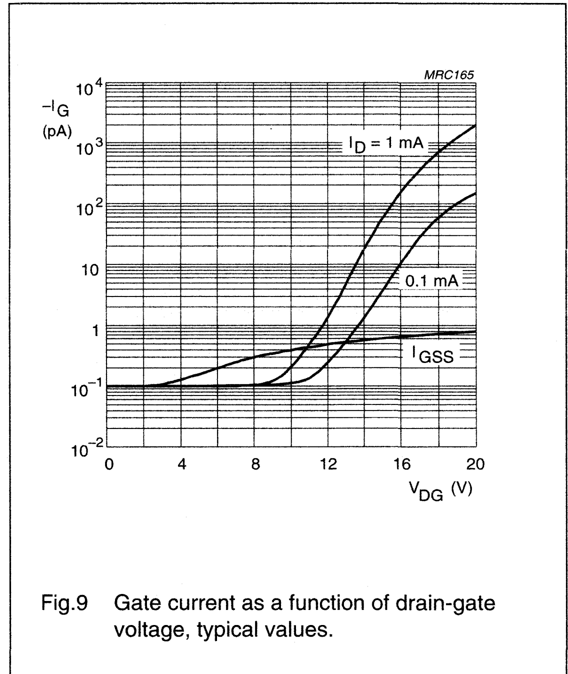


Fig.9 Gate current as a function of drain-gate voltage, typical values.

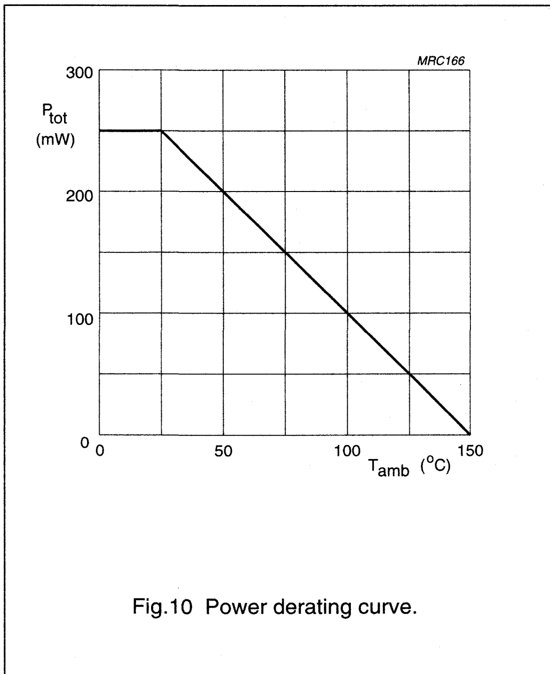
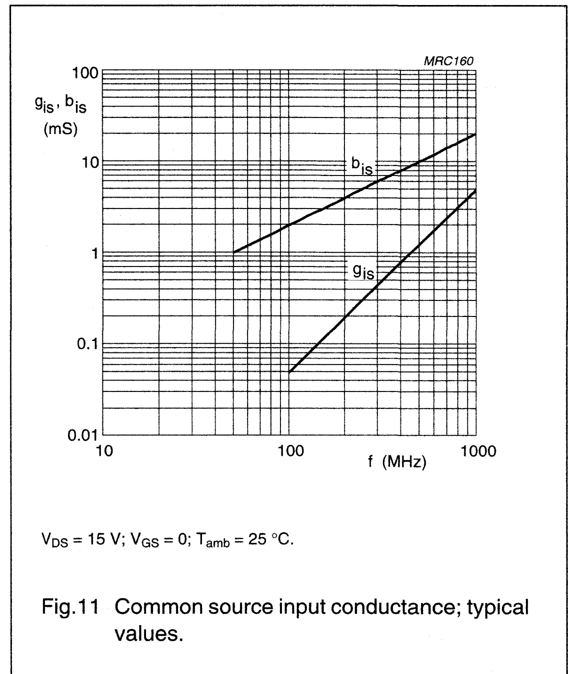
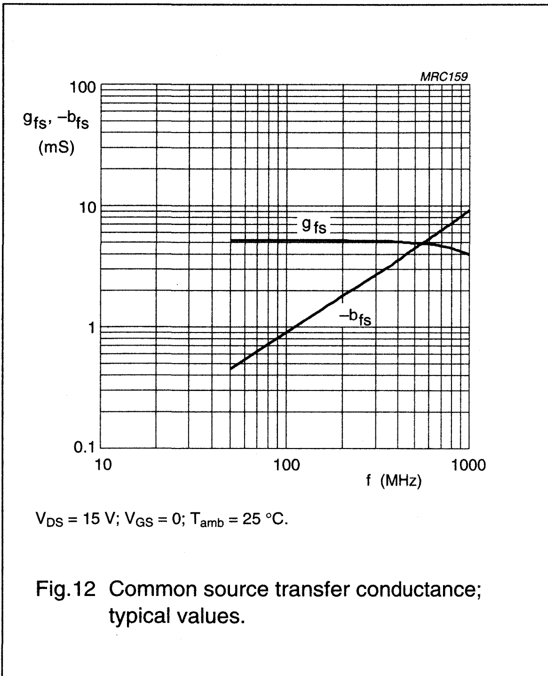


Fig.10 Power derating curve.



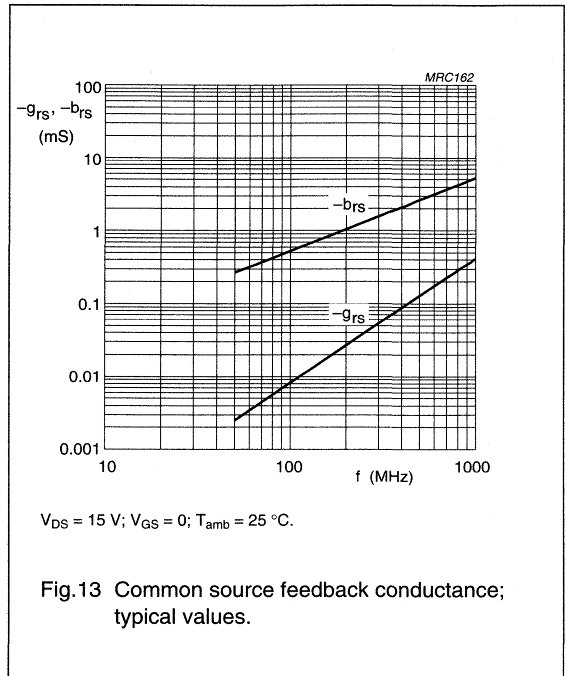
V_{DS} = 15 V; V_{GS} = 0; T_{amb} = 25 °C.

Fig.11 Common source input conductance; typical values.



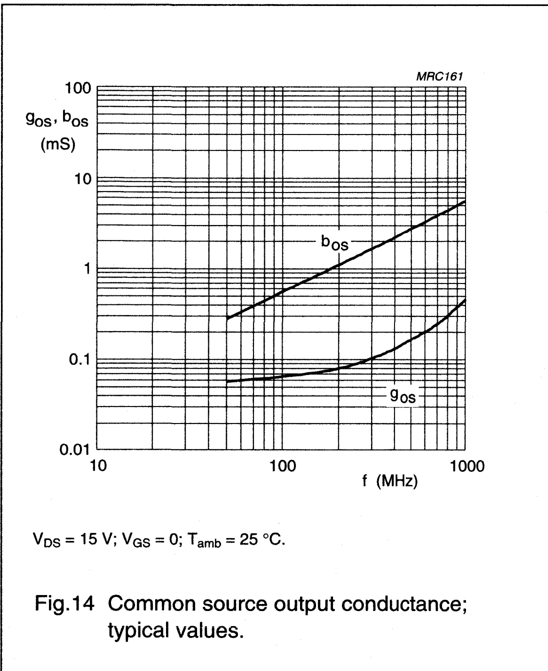
V_{DS} = 15 V; V_{GS} = 0; T_{amb} = 25 °C.

Fig.12 Common source transfer conductance; typical values.



V_{DS} = 15 V; V_{GS} = 0; T_{amb} = 25 °C.

Fig.13 Common source feedback conductance; typical values.



V_{DS} = 15 V; V_{GS} = 0; T_{amb} = 25 °C.

Fig.14 Common source output conductance; typical values.

SPICE parameters for PMBF4416

September 1992; version 1.0.

1	VTO = −3.553	V
2	BETA = 792.6	μA/V^2
3	LAMBDA = 18.46	m/V
4	RD = 7.671	Ω
5	RS = 7.671	Ω
6	IS = 333.4	aA
7	CGSO = 2.920	pF
8	CGDO = 2.261	pF
9	PB = 1.090	V
10 (note 1)	FC = 500.0	m

Note

1. Parameter not extracted; default value.

N-channel field-effect transistors

PMBF5484; PMBF5485; PMBF5486

FEATURES

- Low noise
- Interchangeability of drain and source connections
- High gain.

DESCRIPTION

N-channel, symmetrical, silicon junction FETs in a surface-mountable SOT23 envelope. Intended for use in VHF/UHF amplifiers, oscillators and mixers.

PINNING - SOT23

PIN	DESCRIPTION
1	source
2	drain
3	gate

MARKING CODES:

PMBF5484: p6B
PMBF5485: p6M
PMBF5486: p6H

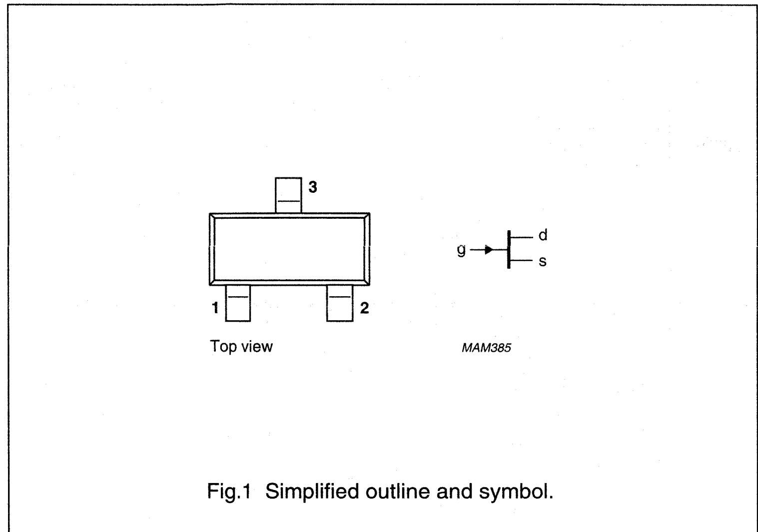


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	25	V
I_{DSS}	drain current	V_{DS} = 15 V; V_{GS} = 0			
	PMBF5484		1	5	mA
	PMBF5485		4	10	mA
	PMBF5486		8	20	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C	–	250	mW
$V_{GS(off)}$	gate-source cut-off voltage	V_{DS} = 15 V; I_D = 1 nA			
	PMBF5484		−0.3	−3	V
	PMBF5485		−0.5	−4	V
	PMBF5486		−2	−6	V
$\lvert Y_{fs} \rvert$	common source transfer admittance	V_{DS} = 15 V; V_{GS} = 0; f = 1 kHz			
	PMBF5484		3	6	mS
	PMBF5485		3.5	7	mS
	PMBF5486		4	8	mS

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	25	V
V_{GSO}	gate-source voltage		–	–25	V
V_{GDO}	gate-drain voltage		–	–25	V
I_G	DC forward gate current		–	10	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C (note 1)	–	250	mW
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	500 K/W

Note

1. Device mounted on an FR4 printed-circuit board.

STATIC CHARACTERISTICS

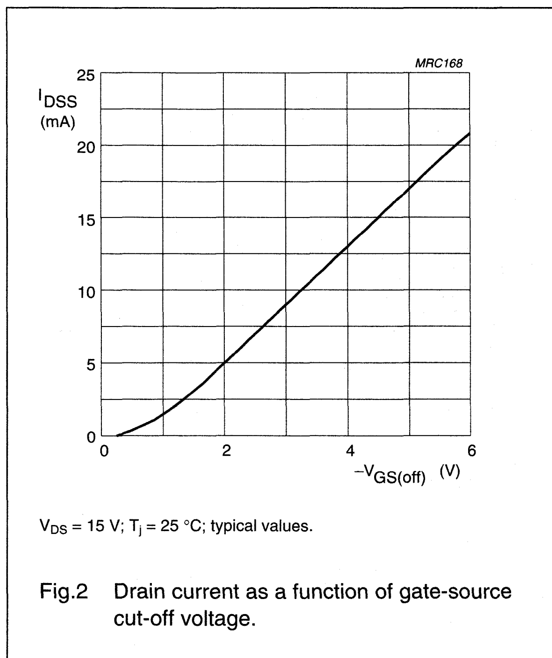
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{(BR)GSS}$	gate-source breakdown voltage	V_{DS} = 0; I_G = –1 μA	–25	–	V
I_{DSS}	drain current	V_{DS} = 15 V; V_{GS} = 0			
	PMBF5484		1	5	mA
	PMBF5485		4	10	mA
	PMBF5486		8	20	mA
I_{GSS}	reverse gate leakage current	V_{DS} = 0; V_{GS} = –15 V	–	–1	nA
V_{GSS}	gate-source forward voltage	V_{DS} = 0; I_G = 1 mA	–	1	V
$V_{GS(off)}$	gate-source cut-off voltage	V_{DS} = 15 V; I_D = 1 nA			
	PMBF5484		–0.3	–3	V
	PMBF5485		–0.5	–4	V
	PMBF5486		–2	–6	V
$\|Y_{fs}\|$	common source transfer admittance	V_{DS} = 15 V; V_{GS} = 0			
	PMBF5484		3	6	mS
	PMBF5485		3.5	7	mS
	PMBF5486		4	8	mS
$\|Y_{os}\|$	common source output admittance	V_{DS} = 15 V; V_{GS} = 0			
	PMBF5484		–	50	μS
	PMBF5485		–	60	μS
	PMBF5486		–	75	μS

DYNAMIC CHARACTERISTICS

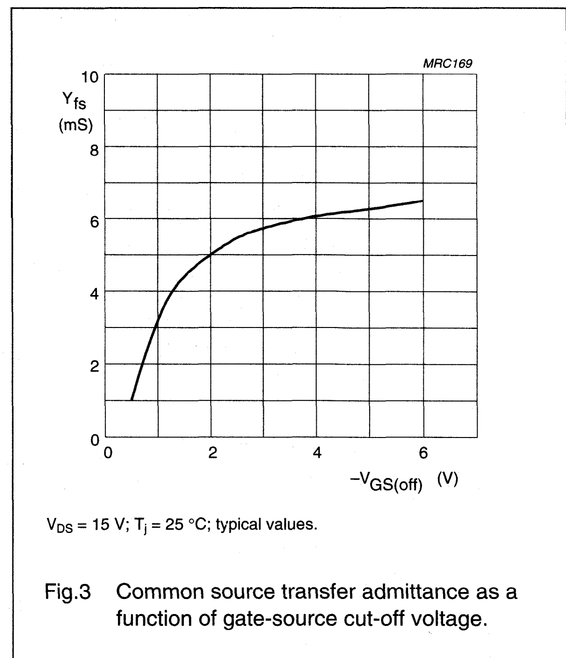
T_j = 25 °C; V_{DS} = 15 V; V_{GS} = 0

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_{is}	input capacitance	f = 1 MHz	–	–	5	pF
C_{os}	output capacitance	f = 1 MHz	–	–	2	pF
C_{rs}	feedback capacitance	f = 1 MHz	–	–	1	pF
g_{is}	common source input conductance					
	PMBF5484	f = 100 MHz	100	–	–	µS
	PMBF5485; PMBF5486	f = 400 MHz	–	–	1	mS
g_{fs}	common source transfer conductance					
	PMBF5484	f = 100 MHz	2.5	–	–	mS
	PMBF5485	f = 400 MHz	3	–	1	mS
	PMBF5486	f = 400 MHz	3.5	–	1	mS
g_{os}	common source output conductance					
	PMBF5484	f = 100 MHz	–	–	75	µS
	PMBF5485; PMBF5486	f = 400 MHz	–	–	100	µS
V_n	equivalent input noise voltage	f = 100 Hz	–	5	–	nV/√Hz



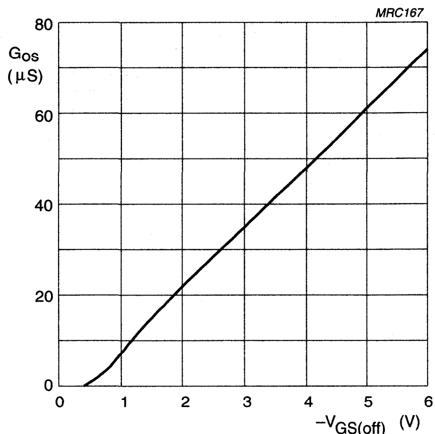
V_{DS} = 15 V; T_j = 25 °C; typical values.

Fig.2 Drain current as a function of gate-source cut-off voltage.



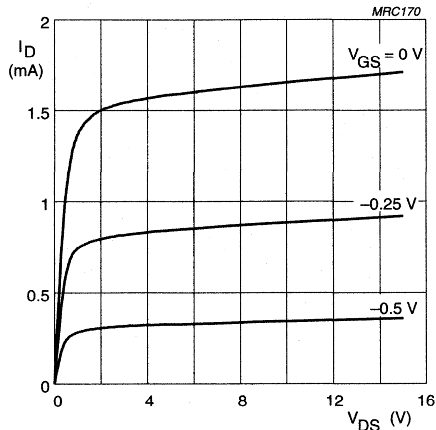
V_{DS} = 15 V; T_j = 25 °C; typical values.

Fig.3 Common source transfer admittance as a function of gate-source cut-off voltage.



V_{DS} = 15 V; T_j = 25 °C; typical values.

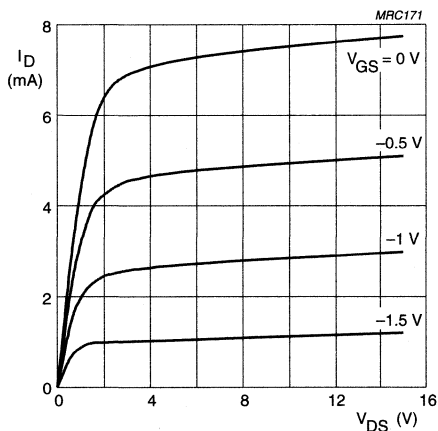
Fig.4 Common source output conductance as a function of gate-source cut-off voltage.



PMBF5484

T_j = 25 °C.

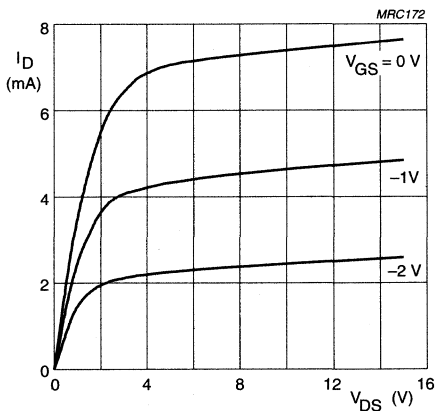
Fig.5 Typical output characteristics.



PMBF5485

T_j = 25 °C.

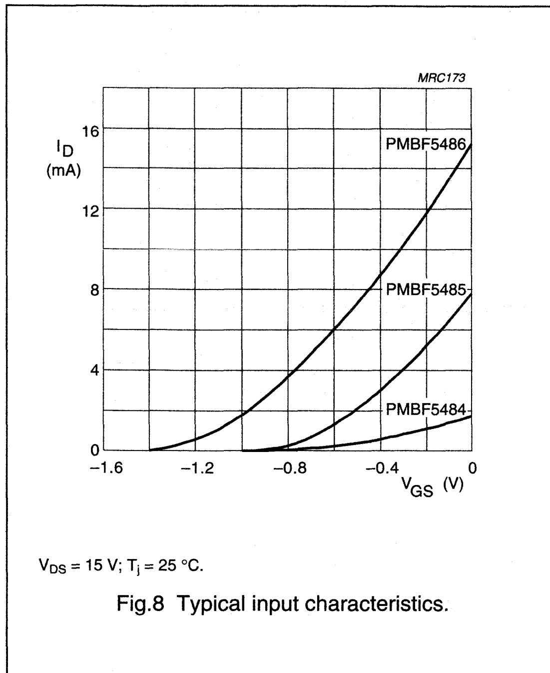
Fig.6 Typical output characteristics.



PMBF5486

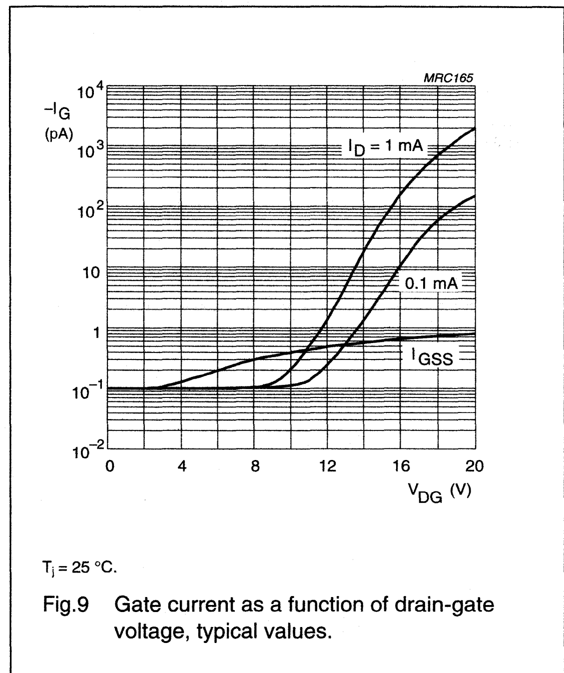
T_j = 25 °C.

Fig.7 Typical output characteristics.



V_{DS} = 15 V; T_j = 25 °C.

Fig.8 Typical input characteristics.



T_j = 25 °C.

Fig.9 Gate current as a function of drain-gate voltage, typical values.

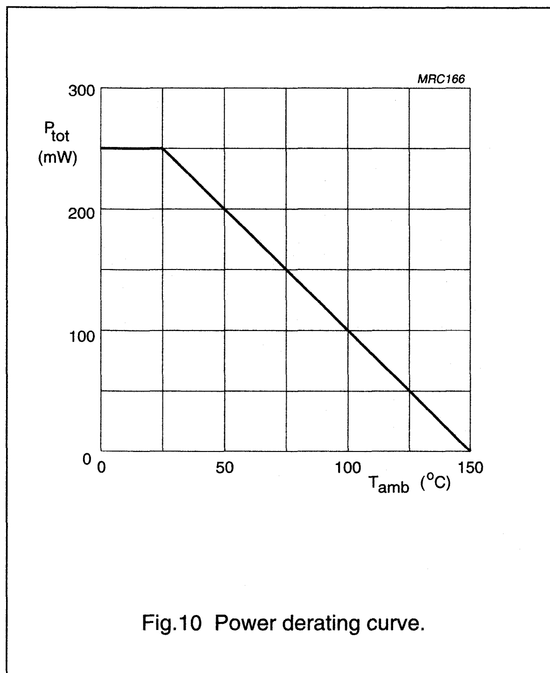
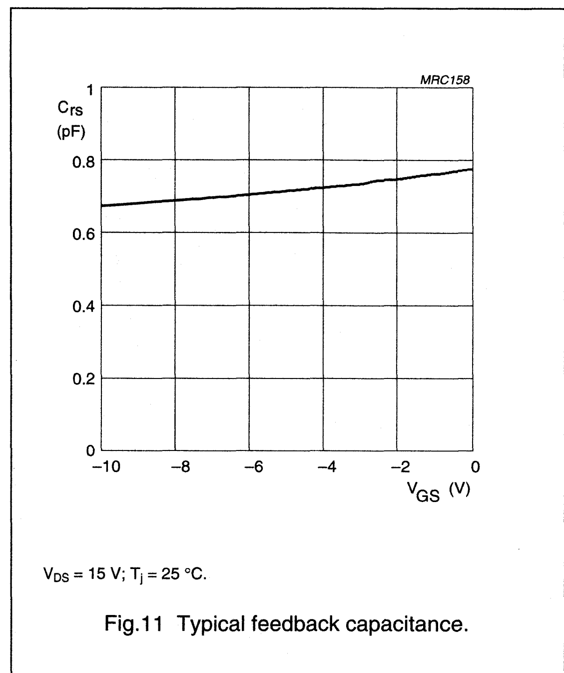
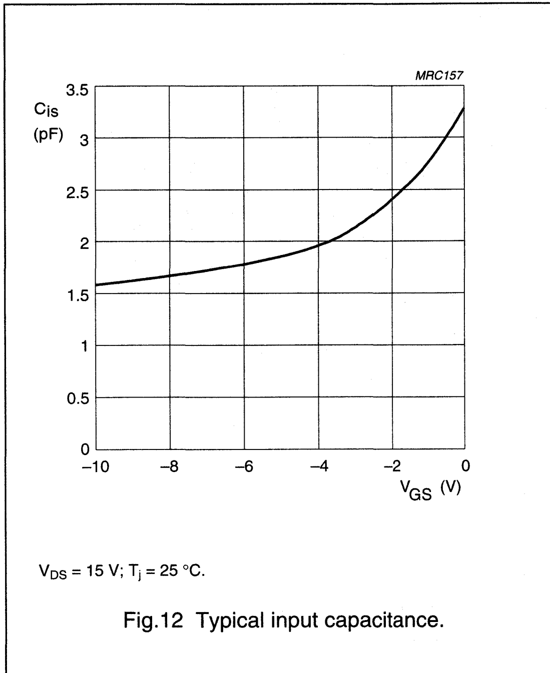


Fig.10 Power derating curve.



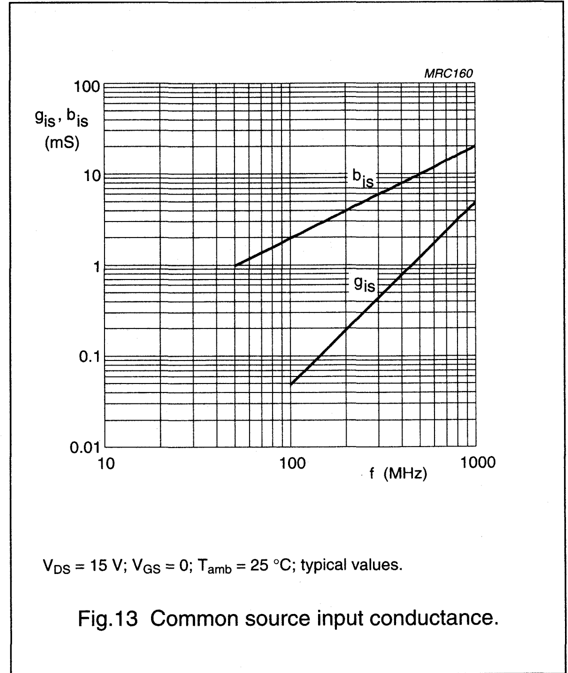
V_{DS} = 15 V; T_j = 25 °C.

Fig.11 Typical feedback capacitance.



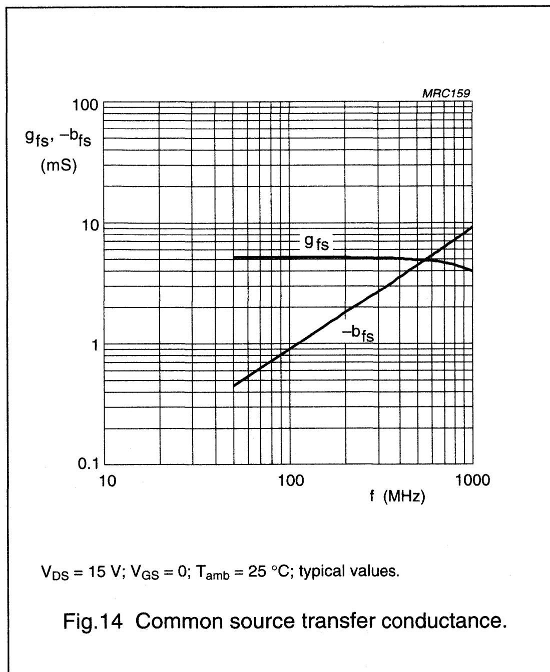
V_{DS} = 15 V; T_j = 25 °C.

Fig.12 Typical input capacitance.



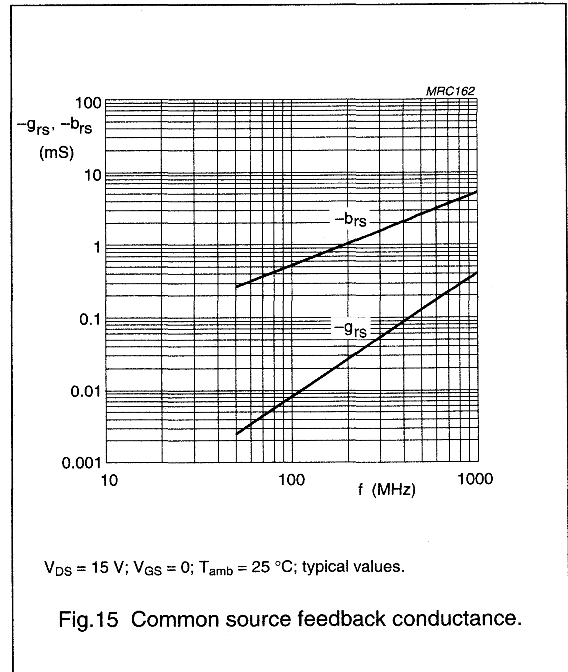
V_{DS} = 15 V; V_{GS} = 0; T_{amb} = 25 °C; typical values.

Fig.13 Common source input conductance.



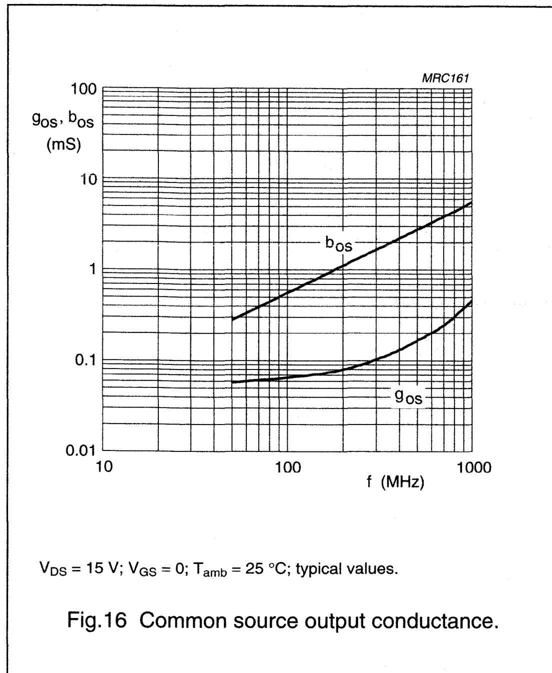
V_{DS} = 15 V; V_{GS} = 0; T_{amb} = 25 °C; typical values.

Fig.14 Common source transfer conductance.



V_{DS} = 15 V; V_{GS} = 0; T_{amb} = 25 °C; typical values.

Fig.15 Common source feedback conductance.



V_{DS} = 15 V; V_{GS} = 0; T_{amb} = 25 °C; typical values.

Fig.16 Common source output conductance.

N-channel junction FETs

PMBFJ108; PMBFJ109; PMBFJ110

FEATURES

- High-speed switching
- Interchangeability of drain and source connections
- Low R_{DSon} at zero gate voltage (< 8 Ω for PMBFJ108).

DESCRIPTION

Symmetrical N-channel junction FETs in a SOT23 envelope. Intended for use in applications such as analog switches, choppers and commutators and in audio amplifiers.

PINNING - SOT23

PIN	DESCRIPTION
1	drain
2	source
3	gate

Note

1. Drain and source are interchangeable.

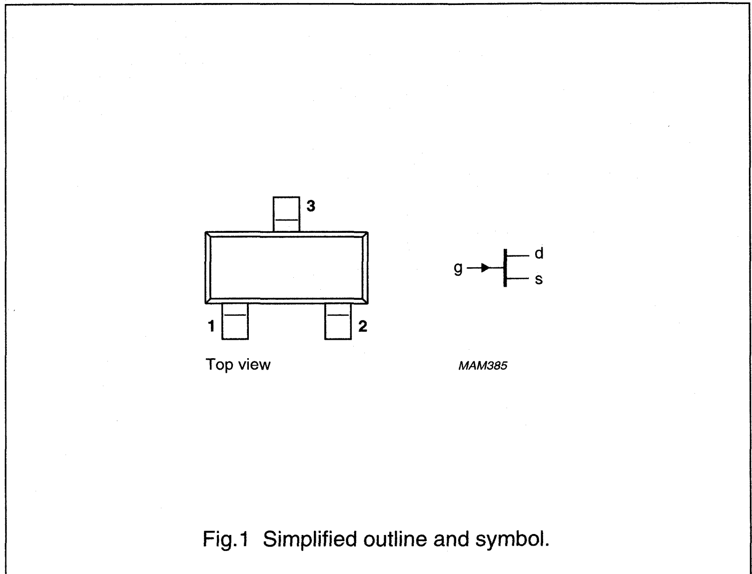


Fig.1 Simplified outline and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	±25	V
V_{GSO}	gate-source voltage		–	–25	V
V_{GDO}	drain-drain voltage		–	–25	V
I_G	forward gate current (DC)			50	mA
P_{tot}	total power dissipation	T_{amb} = 25°C; note 1	–	250	mW
T_{stg}	storage temperature		–65	150	°C
T_j	operating junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	500	K/W

Notes

1. Mounted on an FR-4 printboard.

STATIC CHARACTERISTICS

$T_j = 25\ °C$.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$-I_{GSS}$	reverse gate current	$-V_{GS} = 15$ V $V_{DS} = 0$	–	3	nA
I_{DSX}	drain-source cut-off current	$V_{GS} = -10$ V $V_{DS} = 5$ V	–	3	nA
I_{DSS}	drain current	$V_{GS} = 0$ $V_{DS} = 15$ V			
	PMBFJ108		80	–	mA
	PMBFJ109		40	–	
	PMBFJ110		10	–	
$-V_{(BR)GSS}$	gate-source breakdown voltage	$-I_G = 1$ µA $V_{DS} = 0$	–	25	V
$-V_{GS(off)}$	gate-source cut-off voltage	$I_D = 1$ µA $V_{DS} = 5$ V			
	PMBFJ108		3	10	V
	PMBFJ109		2	6	
	PMBFJ110		0.5	4	
$R_{DS(on)}$	drain-source on-resistance	$V_{GS} = 0$ V $V_{DS} = 0.1$ V			
	PMBFJ108		–	8	Ω
	PMBFJ109		–	12	
	PMBFJ110		–	18	

DYNAMIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
C_{is}	input capacitance	V_{DS} = 0 $-V_{GS}$ = 10 V f = 1 MHz	15	30	pF
C_{is}	input capacitance	V_{DS} = 0 $-V_{GS}$ = 0 f = 1 MHz T_{amb} = 25 °C	50	85	pF
C_{rs}	feedback capacitance	V_{DS} = 0 $-V_{GS}$ = 10 V f = 1 MHz	8	15	pF
Switching times (see Fig.3)					
t_d	delay time	note 1	2	–	ns
t_{on}	turn-on time	note 1	4	–	ns
t_s	storage time	note 1	4	–	ns
t_{off}	turn-off time	note 1	6	–	ns

Notes

1. Test conditions for switching times are as follows:
   V_{DD} = 1.5 V, V_{GS} = 0 to $-V_{GS(off)}$ (all types);
   $-V_{GS(off)}$ = 12 V, R_L = 100 Ω (PMBFJ108);
   $-V_{GS(off)}$ = 7 V, R_L = 100 Ω (PMBFJ109);
   $-V_{GS(off)}$ = 5 V, R_L = 100 Ω (PMBFJ110).

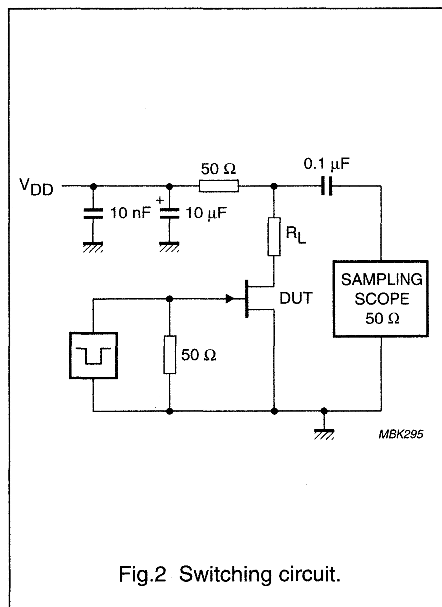


Fig.2 Switching circuit.

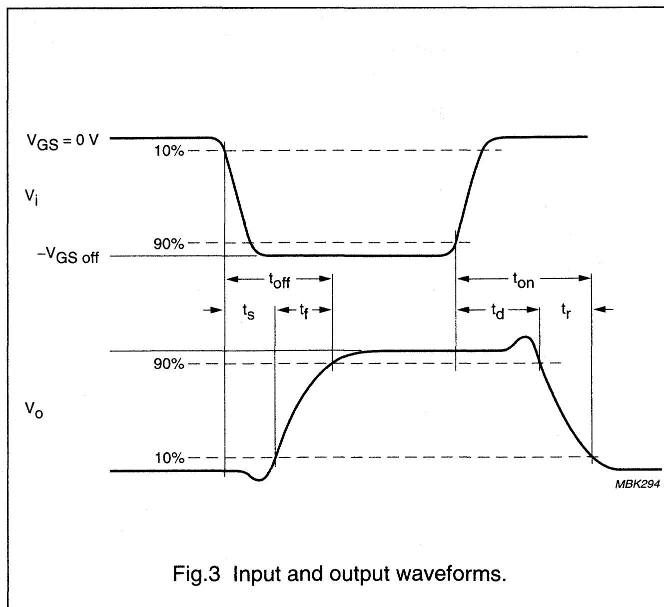


Fig.3 Input and output waveforms.

N-channel junction FETs

PMBFJ111; PMBFJ112; PMBFJ113

FEATURES

- High-speed switching
- Interchangeability of drain and source connections
- Low R_{DSon} at zero gate voltage (< 30 Ω for PMBFJ111).

DESCRIPTION

Symmetrical N-channel junction FETs in a surface mount SOT23 envelope. Intended for use in applications such as analog switches, choppers, commutators, multiplexers and thin and thick film hybrids.

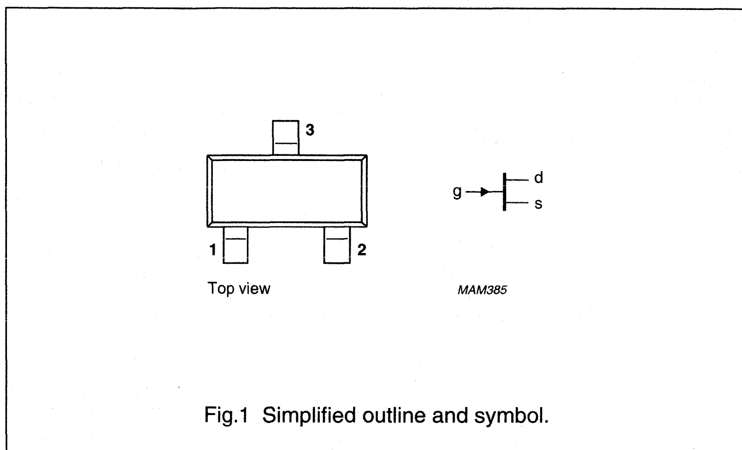


Fig.1 Simplified outline and symbol.

PINNING - SOT23

PIN	DESCRIPTION
1	drain
2	source
3	gate

Note

1. Drain and source are interchangeable.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	±40	V
V_{GSO}	gate-source voltage		–	–40	V
V_{GDO}	drain-drain voltage		–	–40	V
I_G	forward gate current (DC)		–	50	mA
P_{tot}	total power dissipation	T_{amb} = 25 °C; note 1	–	300	mW
T_{stg}	storage temperature		–65	150	°C
T_j	operating junction temperature		–	150	°C

THERMAL CHARACTERISTICS

$T_j = P(R_{th\ j\text{-}t} + R_{th\ t\text{-}s} + R_{th\ s\text{-}a}) + T_{amb}$

SYMBOL	PARAMETER	MAX.	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	430	K/W
$R_{th\ j\text{-}a}$	from junction to ambient (note 2)	500	K/W

Notes

1. Mounted on a ceramic substrate, 8 mm × 10 mm × 0.7 mm.
2. Mounted on printed circuit board.

STATIC CHARACTERISTICS

T_j = 25 °C.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$-I_{GSS}$	reverse gate current	$-V_{GS}$ = 15 V; V_{DS} = 0	–	1	nA
I_{DSS}	drain current	V_{GS} = 0; V_{DS} = 15 V			
	PMBFJ111		20	–	mA
	PMBFJ112		5	–	
	PMBFJ113		2	–	
$-V_{(BR)GSS}$	gate-source breakdown voltage	$-I_G$ = 1 μA; V_{DS} = 0	40	–	V
$-V_{GS(off)}$	gate-source cut-off voltage	I_D = 1 μA; V_{DS} = 5 V			
	PMBFJ111		3	10	V
	PMBFJ112		1	5	
	PMBFJ113		0.5	3	
$R_{DS(on)}$	drain-source on-resistance	V_{GS} = 0 V; V_{DS} = 0.1 V			
	PMBFJ111		–	30	Ω
	PMBFJ112		–	50	
	PMBFJ113		–	100	

DYNAMIC CHARACTERISTICS

T_j = 25 °C.

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
C_{iss}	input capacitance	V_{DS} = 0 $-V_{GS}$ = 10 V f = 1 MHz	6	–	pF
		V_{DS} = 0 $-V_{GS}$ = 0 f = 1 MHz T_{amb} = 25 °C	22	28	pF
C_{rss}	feedback capacitance	V_{DS} = 0 $-V_{GS}$ = 10 V f = 1 MHz	3	–	pF
Switching times (see Fig.2)					
t_r	rise time	note 1	6	–	ns
t_{on}	turn-on time	note 1	13	–	ns
t_f	fall time	note 1	15	–	ns
t_{off}	turn-off time	note 1	35	–	ns

Notes

1. Test conditions for switching times are as follows:
   V_{DD} = 10 V, V_{GS} = 0 to $-V_{GS(off)}$ (all types);
   $-V_{GS(off)}$ = 12 V, R_L = 750 Ω (PMBFJ111);
   $-V_{GS(off)}$ = 7 V, R_L = 1550 Ω (PMBFJ112);
   $-V_{GS(off)}$ = 5 V, R_L = 3150 Ω (PMBFJ113).

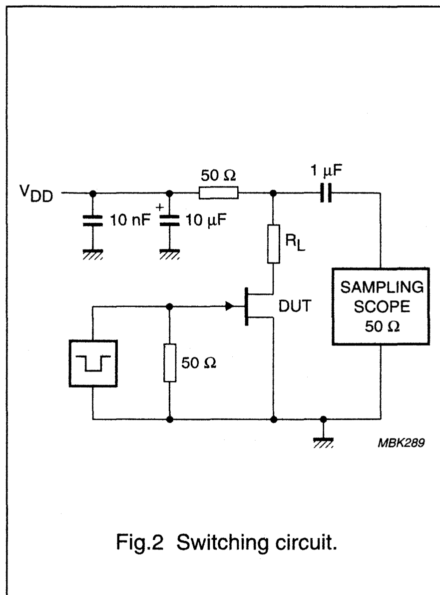


Fig.2 Switching circuit.

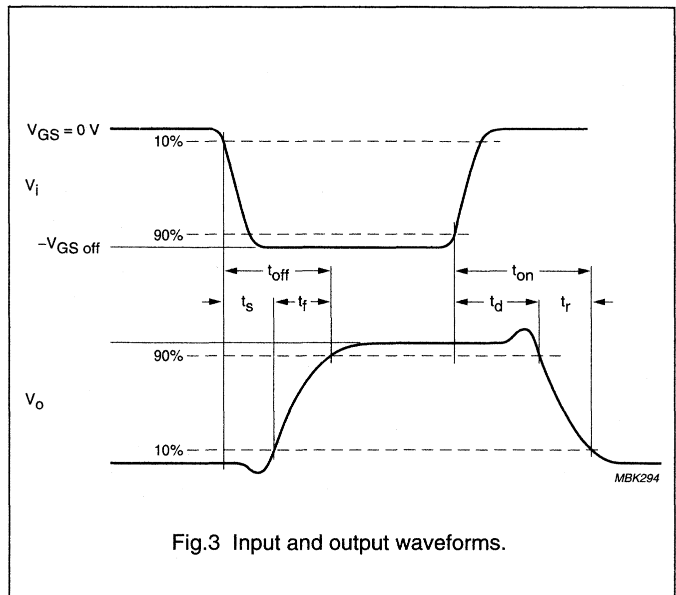


Fig.3 Input and output waveforms.

P-channel silicon field-effect transistors PMBFJ174 to 177

DESCRIPTION

Silicon symmetrical p-channel junction FETs in plastic microminiature SOT23 envelopes.They are intended for application with analogue switches, choppers, commutators etc. using SMD technology. A special feature is the interchangeability of the drain and source connections.

PINNING

1 = drain
2 = source
3 = gate

Note

1. Drain and source are interchangeable.

Marking codes:

174 : p6X
175 : p6W
176 : p6S
177 : p6Y

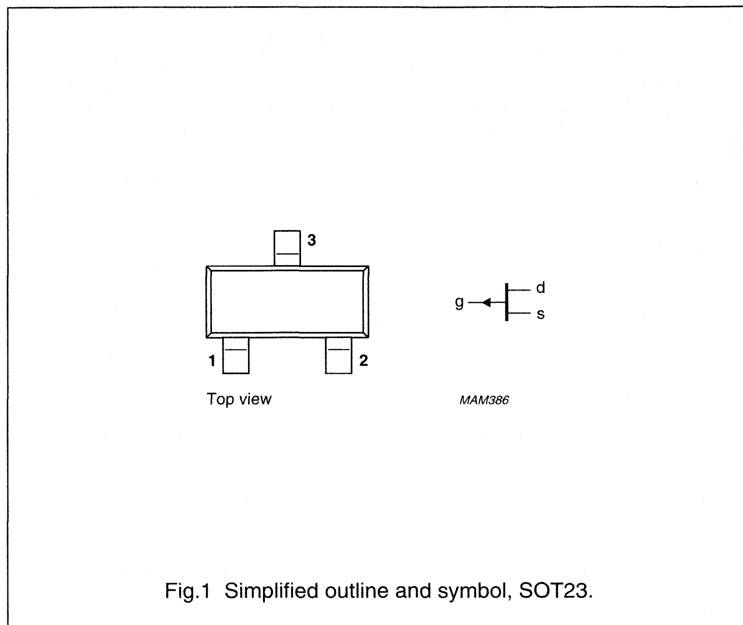


Fig.1 Simplified outline and symbol, SOT23.

QUICK REFERENCE DATA

Drain-source voltage	$\pm V_{DS}$	max.		30			V
Gate-source voltage	V_{GSO}	max.		30			V
Gate current	$-I_G$	max.		50			mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.		300			mW
			PMBFJ174	175	176	177	
Drain current $-V_{DS}$ = 15 V; V_{GS} = 0	$-I_{DSS}$	>	20	7	2	1,5	mA
		<	135	70	35	20	mA
Drain-source ON-resistance $-V_{DS}$ = 0,1 V; V_{GS} = 0	$R_{DS\ on}$	<	85	125	250	300	Ω

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	30	V
Gate-source voltage	V_{GSO}	max.	30	V
Gate-drain voltage	V_{GDO}	max.	30	V
Gate current (d.c.)	$-I_G$	max.	50	mA
Total power dissipation up to T_{amb} = 25 °C[1]	P_{tot}	max.	300	mW
Storage temperature range	T_{stg}		−65 to + 150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j-a}$	=	430	K/W

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

			PMBFJ174	175	176	177	
Gate cut-off current V_{GS} = 20 V; V_{DS} = 0	I_{GSS}	<	1	1	1	1	nA
Drain cut-off current $-V_{DS}$ = 15 V; V_{GS} = 10 V	$-I_{DSX}$	<	1	1	1	1	nA
Drain current $-V_{DS}$ = 15 V; V_{GS} = 0	$-I_{DSS}$	>	20	7	2	1,5	mA
		<	135	70	35	20	mA
Gate-source breakdown voltage I_G = 1 µA; V_{DS} = 0	$V_{(BR)GSS}$	>	30	30	30	30	V
Gate-source cut-off voltage $-I_D$ = 10 nA; V_{DS} = −15 V	$V_{GS\ off}$	>	5	3	1	0,8	V
		<	10	6	4	2,25	V
Drain-source ON-resistance $-V_{DS}$ = 0,1 V; V_{GS} = 0	$R_{DS\ on}$	<	85	125	250	300	Ω

Note

1. Mounted on a ceramic substrate of 8 mm × 10 mm × 0,7 mm.

DYNAMIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Input capacitance, f = 1 MHz							
V_{GS} = 10 V; V_{DS} = 0 V	C_{is}	typ.		8			pF
V_{GS} = V_{DS} = 0	C_{is}	typ.		30			pF
Feedback capacitance, f = 1 MHz							
V_{GS} = 10 V; V_{DS} = 0 V	C_{rs}	typ.		4			pF
Switching times (see Fig.2 + 3)		**PMBFJ174**		**175**	**176**	**177**	
Delay time	t_d	typ.	2	5	15	20	ns
Rise time	t_r	typ.	5	10	20	25	ns
Turn-on time	t_{on}	typ.	7	15	35	45	ns
Storage temperature	t_s	typ.	5	10	15	20	ns
Fall time	t_f	typ.	10	20	20	25	ns
Turn-off time	t_{off}	typ.	15	30	35	45	ns
Test conditions:	$-V_{DD}$		10	6	6	6	V
	$V_{GS\ off}$		12	8	6	3	V
	R_L		560	1200	2000	2900	Ω
	$V_{GS\ on}$		0	0	0	0	V

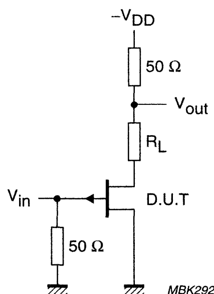
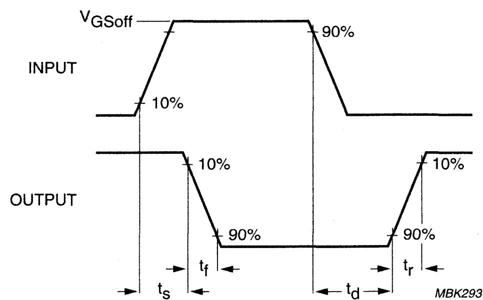


Fig.2 Switching times test circuit



Rise time input voltage < 1 ns

Fig.3 Input and output waveforms
$t_d + t_r = t_{on}$
$t_s + t_f = t_{off}$

FEATURES

- High speed switching
- Interchangeability of drain and source connections
- High impedance.

APPLICATIONS

- Analog switches
- Choppers, multiplexers and commutators
- Audio amplifiers.

DESCRIPTION

N-channel symmetrical junction field-effect transistor in a SOT23 package.

CAUTION
This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling. For further information, refer to Philips specs.: SNW-EQ-608, SNW-FQ-302A and SNW-FQ-302B.

PINNING - SOT23

PIN	SYMBOL	DESCRIPTION
1	s	source
2	d	drain
3	g	gate

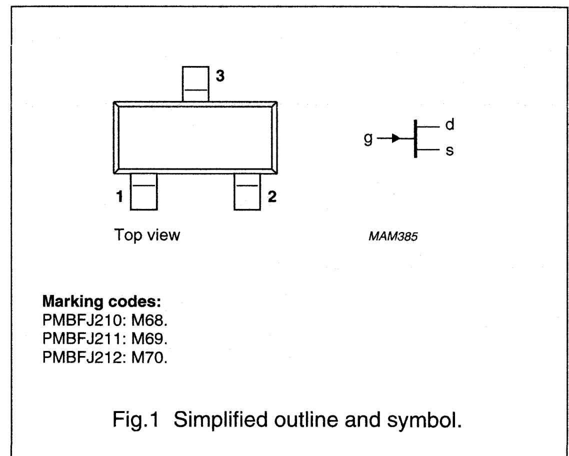


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	±25	V
V_{GSoff}	gate-source cut-off voltage	I_D = 1 nA; V_{DS} = 15 V			
	PMBFJ210		–1	–3	V
	PMBFJ211		–2.5	–4.5	V
	PMBFJ212		–4	–6	V
I_{DSS}	drain current	V_{GS} = 0; V_{DS} = 15 V			
	PMBFJ210		2	15	mA
	PMBFJ211		7	20	mA
	PMBFJ212		15	40	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C	–	250	mW
$\lvert y_{fs} \rvert$	common-source transfer admittance	V_{GS} = 0; V_{DS} = 15 V			
	PMBFJ210		4	12	mS
	PMBFJ211		6	12	mS
	PMBFJ212		7	12	mS

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	±25	V
V_{GSO}	gate-source voltage	open drain	–	–25	V
V_{DGO}	drain-gate voltage	open source	–	–25	V
I_G	forward gate current (DC)		–	10	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C; note 1; see Fig.13	–	250	mW
T_{stg}	storage temperature		–65	150	°C
T_j	operating junction temperature		–	150	°C

Note

1. Device mounted on an FR4 printed-circuit board.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient; note 1	500	K/W

Note

1. Device mounted on an FR4 printed-circuit board.

STATIC CHARACTERISTICS

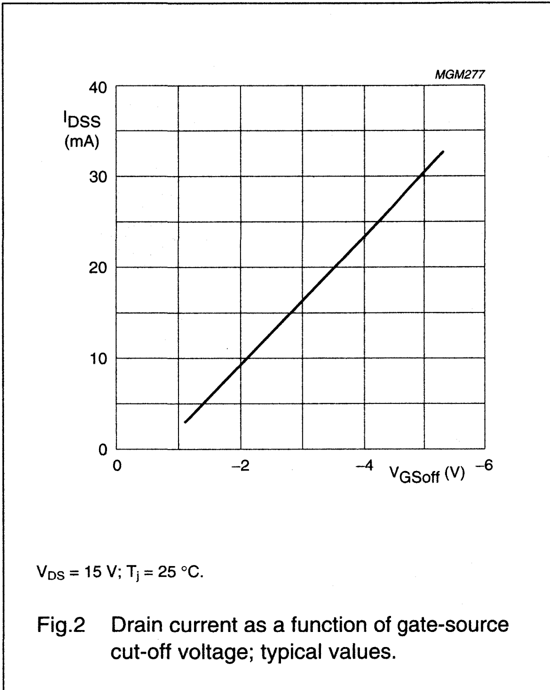
T_j = 25 °C.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{(BR)GSS}$	gate-source breakdown voltage	I_G = −1 μA; V_{DS} = 0	−	−25	V
V_{GSoff}	gate-source cut-off voltage	I_D = 1 nA; V_{DS} = 15 V			
	PMBFJ210		−1	−3	V
	PMBFJ211		−2.5	−4.5	V
	PMBFJ212		−4	−6	V
V_{GSS}	gate-source forward voltage	I_G = 0; V_{DS} = 0	−	1	V
I_{DSS}	drain current	V_{GS} = 0; V_{DS} = 15 V			
	PMBFJ10		2	15	mA
	PMBFJ11		7	20	mA
	PMBFJ12		15	40	mA
I_{GSS}	reverse gate leakage current	V_{GS} = −15 V; V_{DS} = 0	−	−100	pA
$\lvert y_{fs} \rvert$	common-source transfer admittance	V_{GS} = 0; V_{DS} = 15 V			
	PMBFJ210		4	12	mS
	PMBFJ211		6	12	mS
	PMBFJ212		7	12	mS
$\lvert y_{os} \rvert$	common source output admittance	V_{GS} = 0; V_{DS} = 15 V			
	PMBFJ210		−	150	μS
	PMBFJ211		−	200	μS
	PMBFJ212		−	200	μS

DYNAMIC CHARACTERISTICS

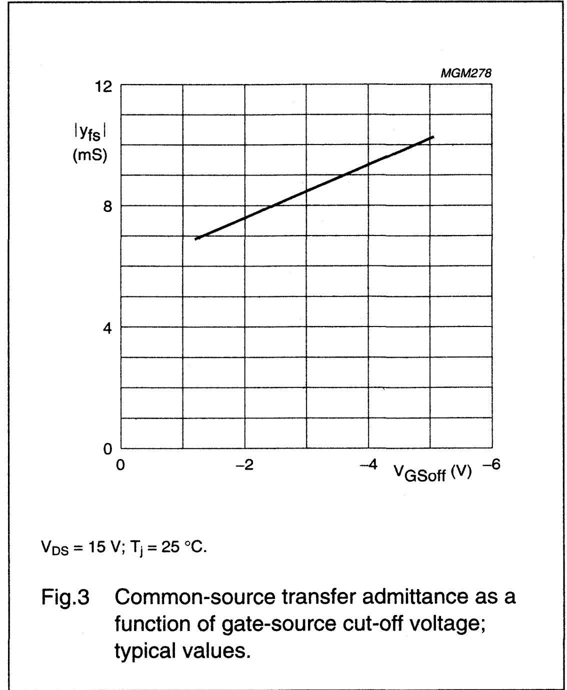
T_{amb} = 25 °C.

SYMBOL	PARAMETER	CONDITIONS	TYP.	UNIT
C_{is}	input capacitance	V_{DS} = 15 V; V_{GS} = −10 V; f = 1 MHz	2	pF
		V_{DS} = 15 V; V_{GS} = 0; f = 1 MHz	4	pF
C_{os}	output capacitance	V_{DS} = 15 V; V_{GS} = −10 V; f = 1 MHz	0.8	pF
		V_{DS} = 15 V; V_{GS} = 0; f = 1 MHz	2	pF
C_{rs}	feedback capacitance	V_{DS} = 15 V; V_{GS} = −10 V; f = 1 MHz	0.8	pF
		V_{DS} = 15 V; V_{GS} = 0; f = 1 MHz	0.9	pF
g_{is}	common source input conductance	V_{DS} = 15 V; V_{GS} = 0; f = 100 MHz	70	μS
		V_{DS} = 15 V; V_{GS} = 0; f = 450 MHz	1.1	mS
g_{fs}	common source transfer conductance	V_{DS} = 15 V; V_{GS} = 0; f = 100 MHz	7.5	mS
		V_{DS} = 15 V; V_{GS} = 0; f = 450 MHz	7.5	mS
g_{rs}	common source feedback conductance	V_{DS} = 15 V; V_{GS} = 0; f = 100 MHz	−8	μS
		V_{DS} = 15 V; V_{GS} = 0; f = 450 MHz	−90	μS
g_{os}	common source output conductance	V_{DS} = 15 V; V_{GS} = 0; f = 100 MHz	95	μS
		V_{DS} = 15 V; V_{GS} = 0; f = 450 MHz	200	μS
V_n	equivalent input noise voltage	V_{DS} = 15 V; V_{GS} = 0; f = 1 kHz	5	$nV/\sqrt{Hz}$



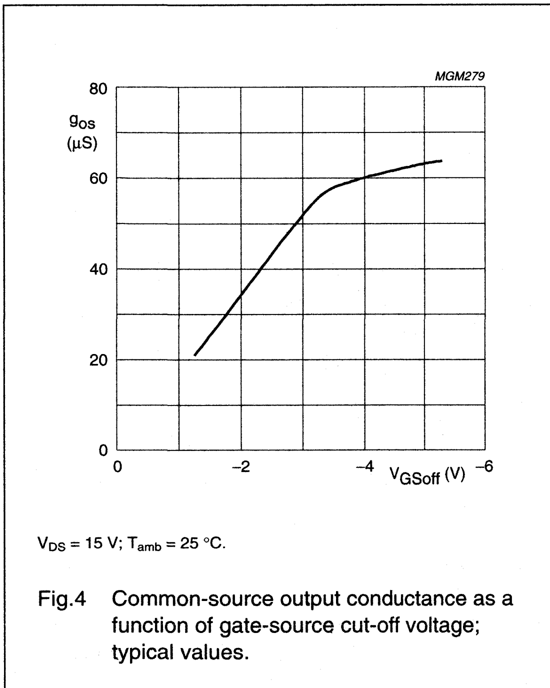
V_{DS} = 15 V; T_j = 25 °C.

Fig.2 Drain current as a function of gate-source cut-off voltage; typical values.



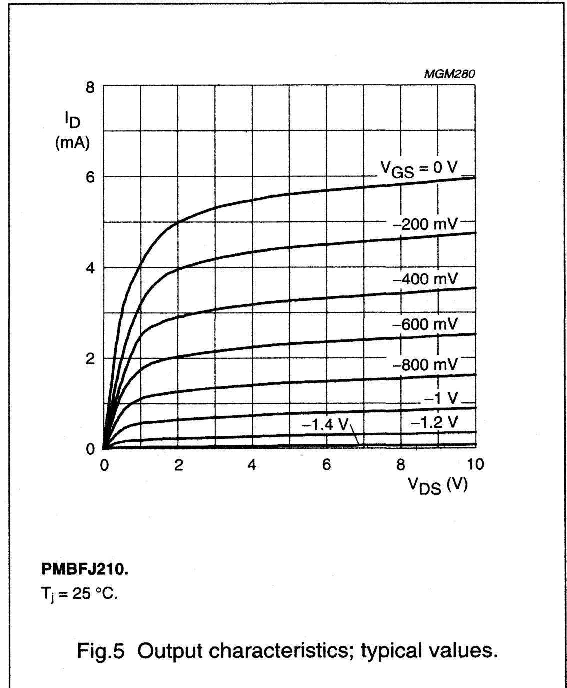
V_{DS} = 15 V; T_j = 25 °C.

Fig.3 Common-source transfer admittance as a function of gate-source cut-off voltage; typical values.



V_{DS} = 15 V; T_{amb} = 25 °C.

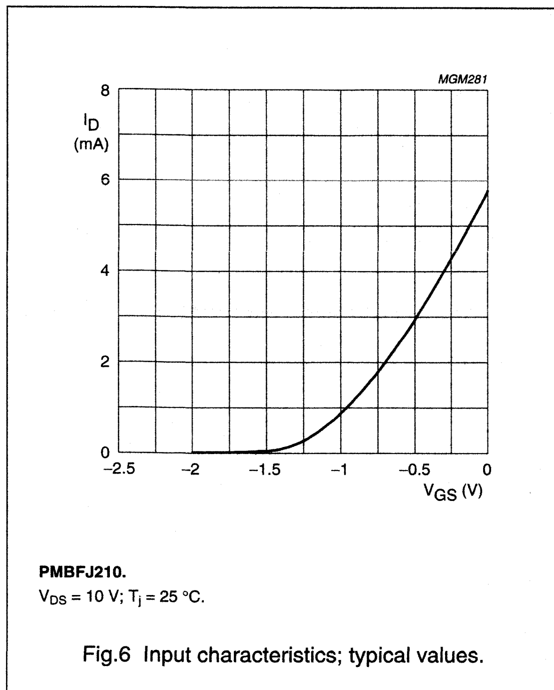
Fig.4 Common-source output conductance as a function of gate-source cut-off voltage; typical values.



PMBFJ210.

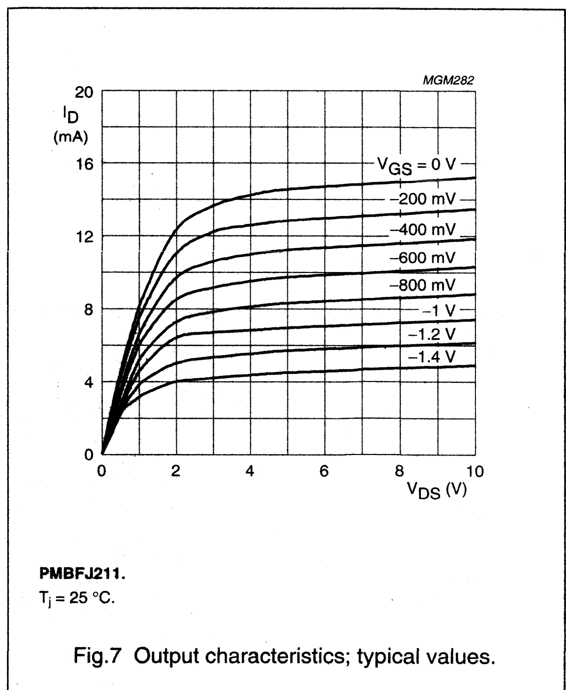
T_j = 25 °C.

Fig.5 Output characteristics; typical values.



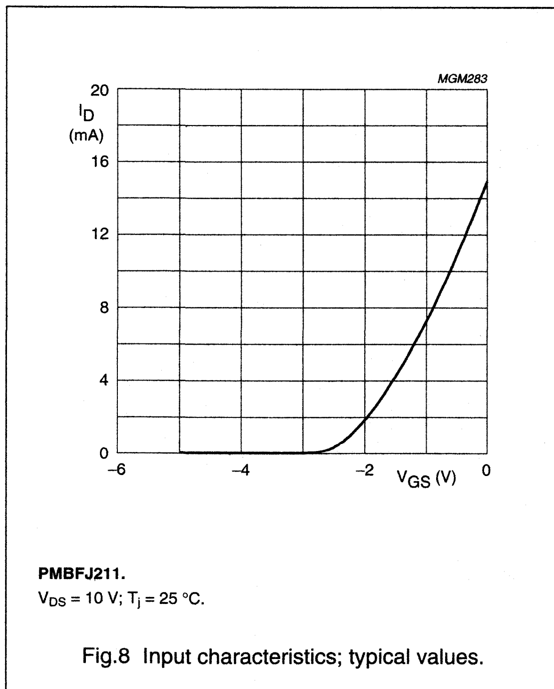
PMBFJ210.
V_{DS} = 10 V; T_j = 25 °C.

Fig.6 Input characteristics; typical values.



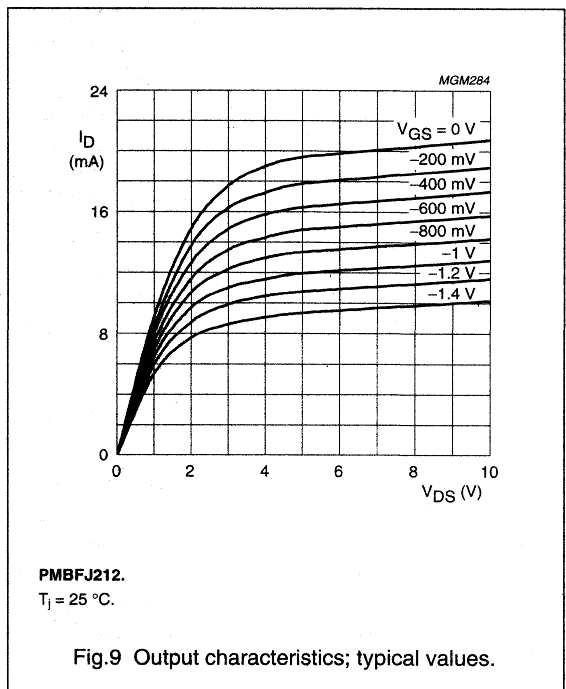
PMBFJ211.
T_j = 25 °C.

Fig.7 Output characteristics; typical values.



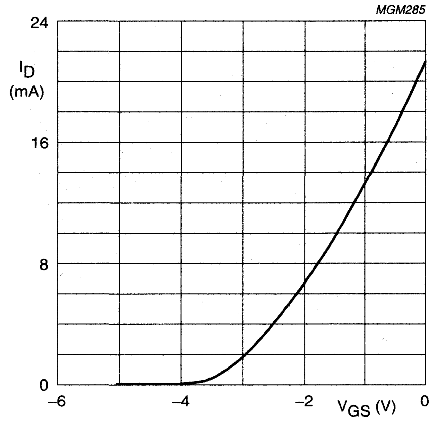
PMBFJ211.
V_{DS} = 10 V; T_j = 25 °C.

Fig.8 Input characteristics; typical values.



PMBFJ212.
T_j = 25 °C.

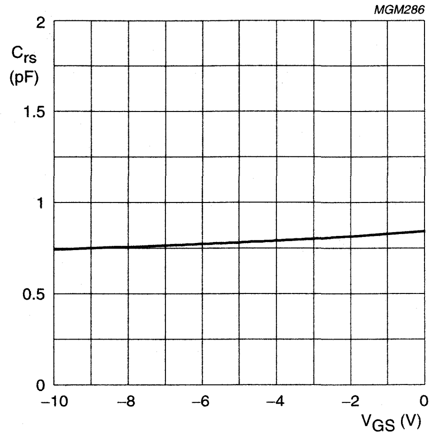
Fig.9 Output characteristics; typical values.



PMBFJ212.

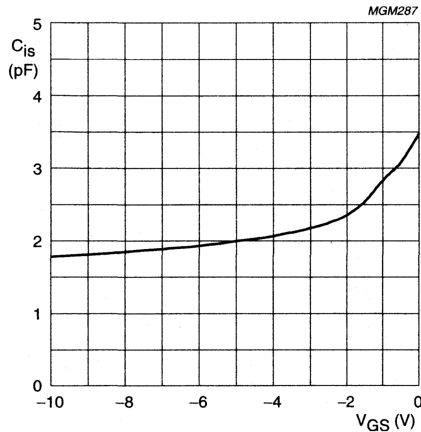
V_{DS} = 10 V; T_j = 25 °C.

Fig.10 Input characteristics; typical values.



V_{DS} = 15 V; f = 1 Mhz; T_{amb} = 25 °C.

Fig.11 Feedback capacitance as a function of gate-source voltage; typical values.



V_{DS} = 15 V; f = 1 Mhz; T_{amb} = 25 °C.

Fig.12 Input capacitance as a function of gate-source voltage; typical values.

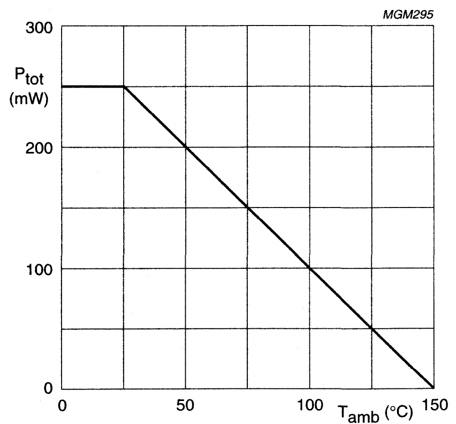
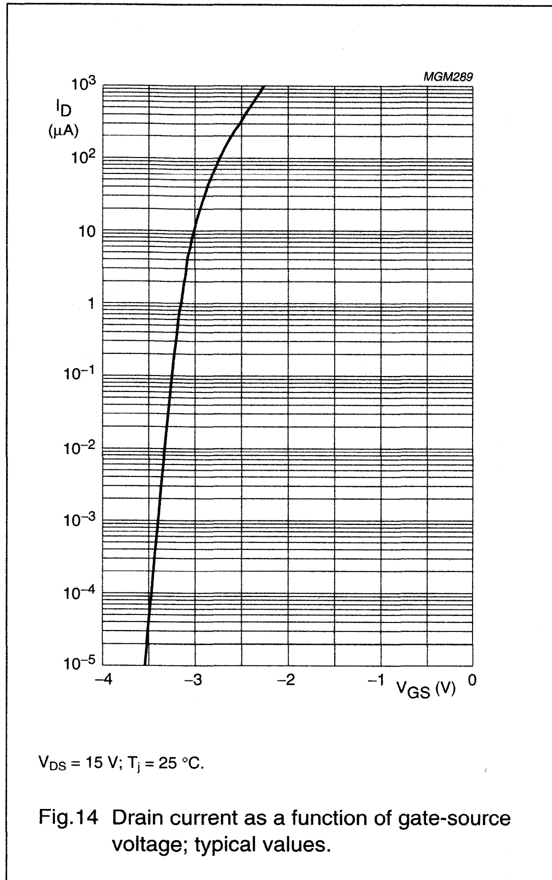
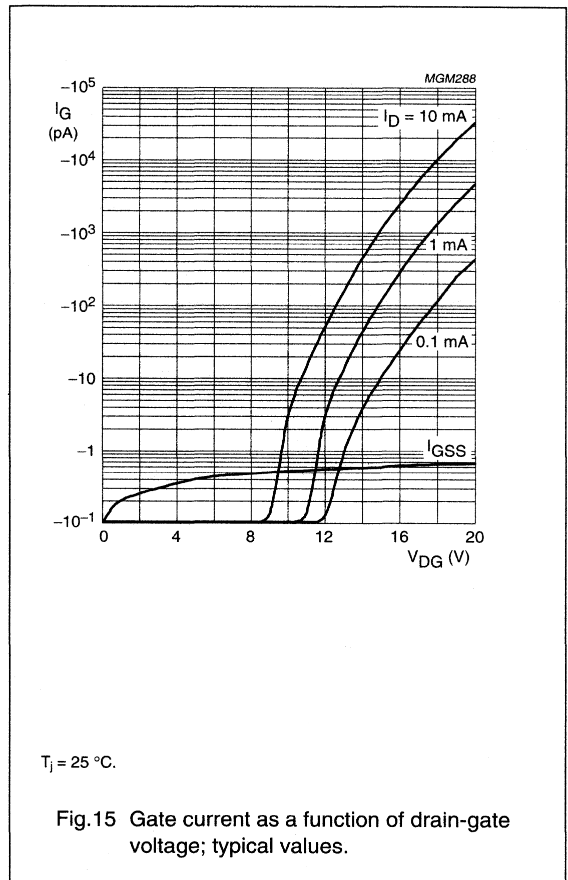


Fig.13 Power derating curve.



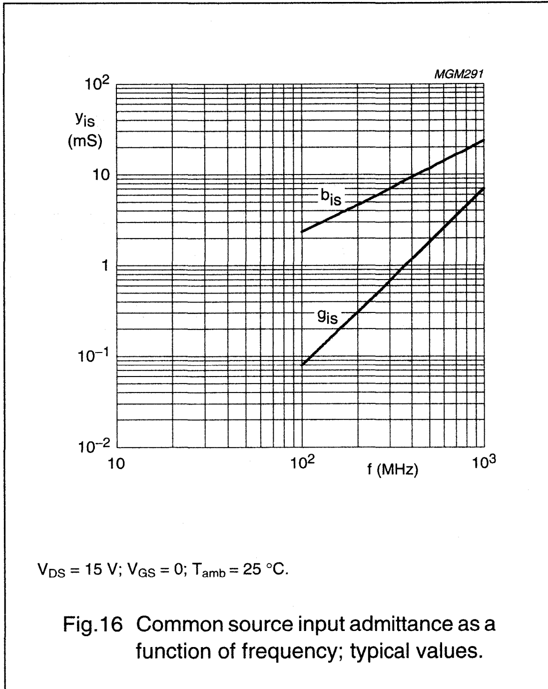
V_{DS} = 15 V; T_j = 25 °C.

Fig.14 Drain current as a function of gate-source voltage; typical values.



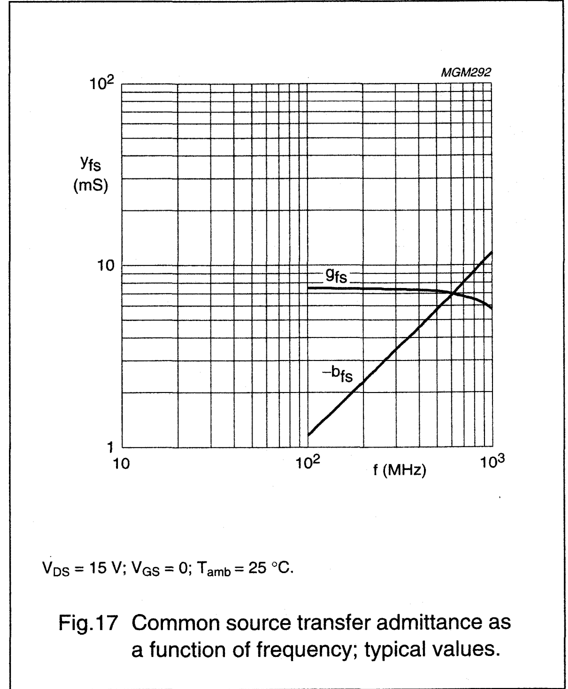
T_j = 25 °C.

Fig.15 Gate current as a function of drain-gate voltage; typical values.



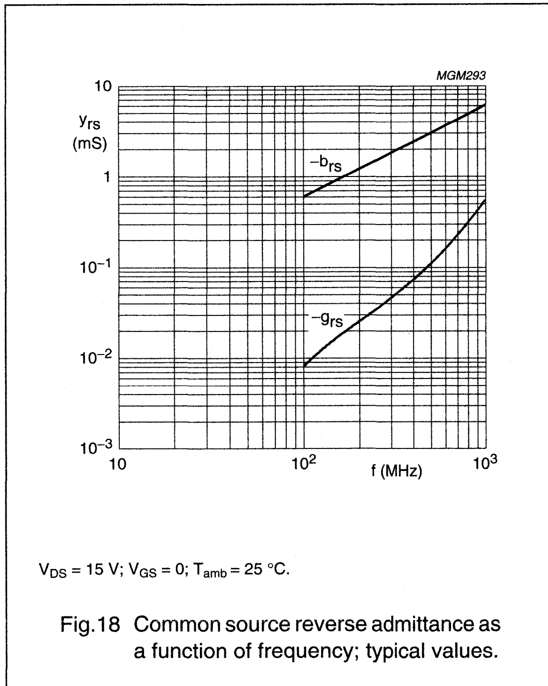
V_{DS} = 15 V; V_{GS} = 0; T_{amb} = 25 °C.

Fig.16 Common source input admittance as a function of frequency; typical values.



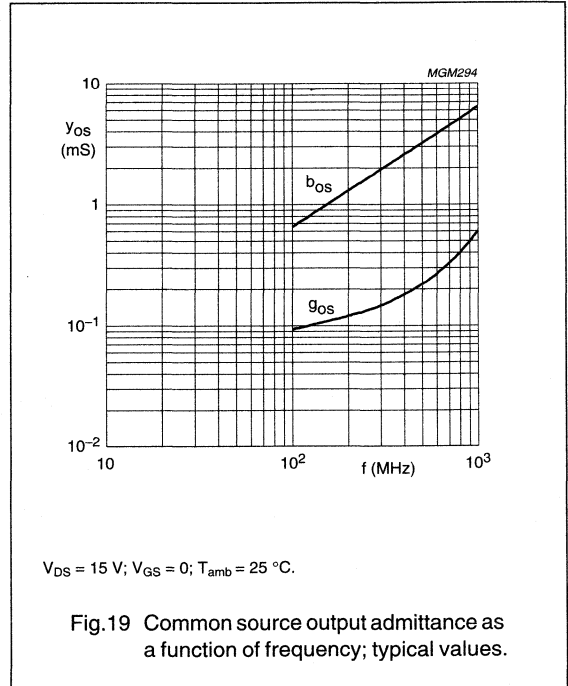
V_{DS} = 15 V; V_{GS} = 0; T_{amb} = 25 °C.

Fig.17 Common source transfer admittance as a function of frequency; typical values.



V_{DS} = 15 V; V_{GS} = 0; T_{amb} = 25 °C.

Fig.18 Common source reverse admittance as a function of frequency; typical values.



V_{DS} = 15 V; V_{GS} = 0; T_{amb} = 25 °C.

Fig.19 Common source output admittance as a function of frequency; typical values.

N-channel silicon field-effect transistors

PMBFJ308; PMBFJ309; PMBFJ310

FEATURES

- Low noise
- Interchangeability of drain and source connections
- High gain.

APPLICATIONS

- AM input stage in car radios
- VHF amplifiers
- Oscillators and mixers.

DESCRIPTION

N-channel symmetrical silicon junction field-effect transistors in a SOT23 package.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING - SOT23

PIN	SYMBOL	DESCRIPTION
1	s	source
2	d	drain
3	g	gate

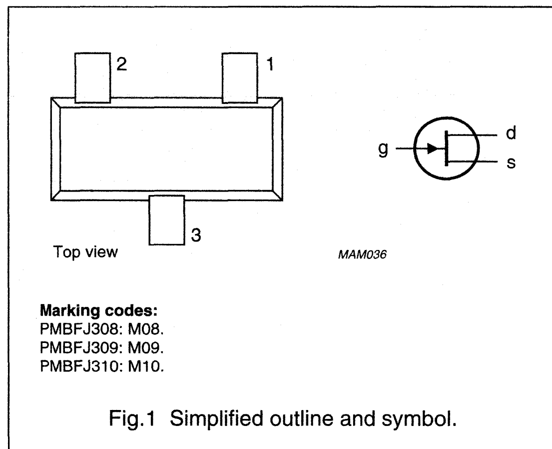


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	±25	V
V_{GSoff}	gate-source cut-off voltage	V_{DS} = 10 V; I_D = 1 μA			
	PMBFJ308		–1	–6.5	V
	PMBFJ309		–1	–4	V
	PMBFJ310		–2	–6.5	V
I_{DSS}	drain current	V_{GS} = 0; V_{DS} = 10 V			
	PMBFJ308		12	60	mA
	PMBFJ309		12	30	mA
	PMBFJ310		24	60	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C	–	250	mW
$\|y_{fs}\|$	forward transfer admittance	V_{DS} = 10 V; I_D = 10 mA	10	–	mS

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	±25	V
V_{GSO}	gate-source voltage	open drain	–	–25	V
V_{GDO}	gate-drain voltage	open source	–	–25	V
I_G	forward gate current (DC)		–	50	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C	–	250	mW
T_{stg}	storage temperature		–65	150	°C
T_j	operating junction temperature		–	150	°C

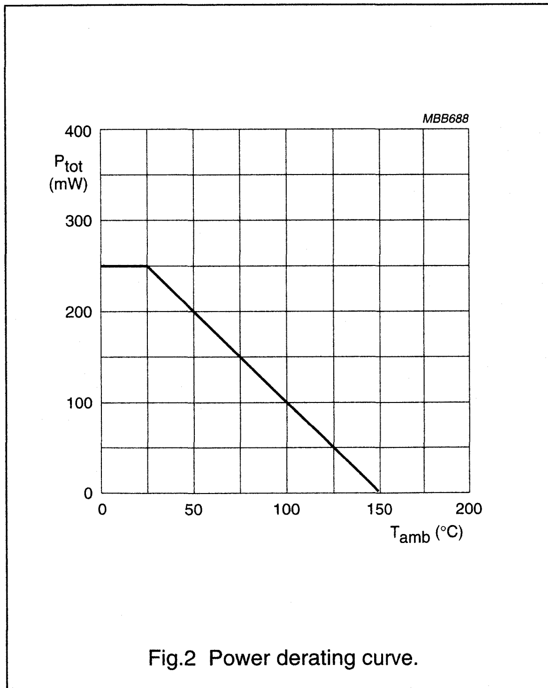


Fig.2 Power derating curve.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient; note 1	500	K/W

Note

1. Device mounted on an FR4 printed-circuit board.

STATIC CHARACTERISTICS

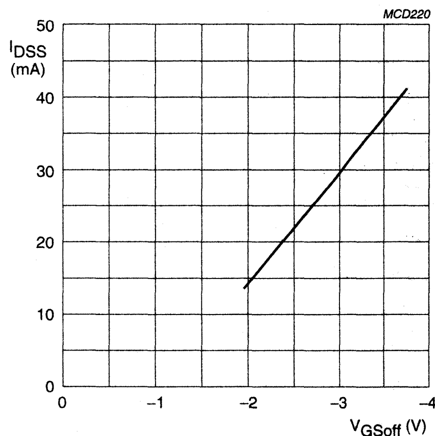
T_j = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)GSS}$	gate-source breakdown voltage	I_G = −1 μA; V_{DS} = 0	−25	–	–	V
V_{GSoff}	gate-source cut-off voltage	I_D = 1 μA; V_{DS} = 10 V				V
	PMBFJ308		−1	–	−6.5	V
	PMBFJ309		−1	–	−4	V
	PMBFJ310		−2	–	−6.5	V
V_{GSS}	gate-source forward voltage	I_G = 1 mA; V_{DS} = 0	–	–	1	V
I_{DSS}	drain current	V_{DS} = 10 V; V_{GS} = 0				
	PMBFJ308		12	–	60	mA
	PMBFJ309		12	–	30	mA
	PMBFJ310		24	–	60	mA
I_{GSS}	gate leakage current	V_{GS} = −15 V; V_{DS} = 0	–	–	−1	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 0; V_{DS} = 100 mV	–	50	–	Ω
$\lvert y_{fs} \rvert$	forward transfer admittance	I_D = 10 mA; V_{DS} = 10 V	10	–	–	mS
$\lvert y_{os} \rvert$	common source output admittance	I_D = 10 mA; V_{DS} = 10 V	–	–	250	μS

DYNAMIC CHARACTERISTICS

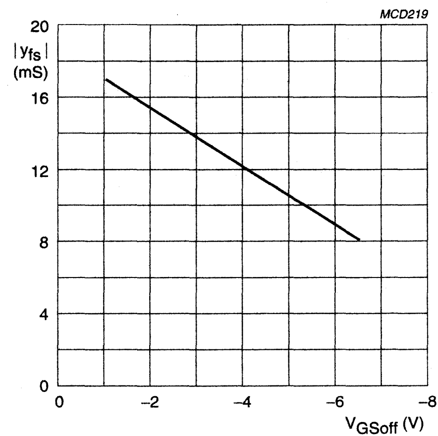
T_j = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
C_{is}	input capacitance	V_{DS} = 10 V; V_{GS} = −10 V; f = 1 MHz	3	5	pF
		V_{DS} = 10 V; V_{GS} = 0; T_{amb} = 25 °C	6	−	pF
C_{rs}	reverse transfer capacitance	V_{DS} = 0; V_{GS} = −10 V; f = 1 MHz	1.3	2.5	pF
g_{is}	common source input conductance	V_{DS} = 10 V; I_D = 10 mA; f = 100 MHz	200	−	µS
		V_{DS} = 10 V; I_D = 10 mA; f = 450 MHz	3	−	mS
g_{fs}	common source transfer conductance	V_{DS} = 10 V; I_D = 10 mA; f = 100 MHz	13	−	mS
		V_{DS} = 10 V; I_D = 10 mA; f = 450 MHz	12	−	mS
g_{rs}	common source reverse conductance	V_{DS} = 10 V; I_D = 10 mA; f = 100 MHz	−30	−	µS
		V_{DS} = 10 V; I_D = 10 mA; f = 450 MHz	−450	−	µS
g_{os}	common source output conductance	V_{DS} = 10 V; I_D = 10 mA; f = 100 MHz	150	−	µS
		V_{DS} = 10 V; I_D = 10 mA; f = 450 MHz	400	−	µS
V_n	equivalent input noise voltage	V_{DS} = 10 V; I_D = 10 mA; f = 100 Hz	6	−	nV/√Hz



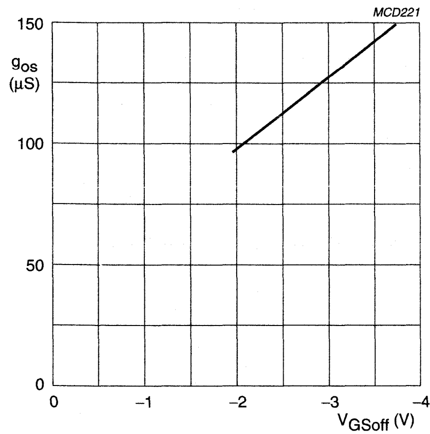
V_{DS} = 10 V; T_j = 25 °C.

Fig.3 Drain current as a function of gate-source cut-off voltage; typical values.



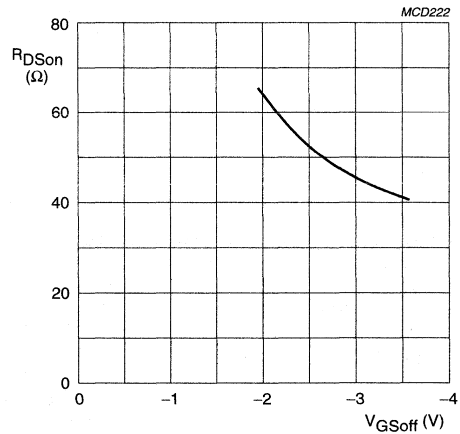
V_{DS} = 10 V; I_D = 10 mA; T_j = 25 °C.

Fig.4 Forward transfer admittance as a function of gate-source cut-off voltage; typical values.



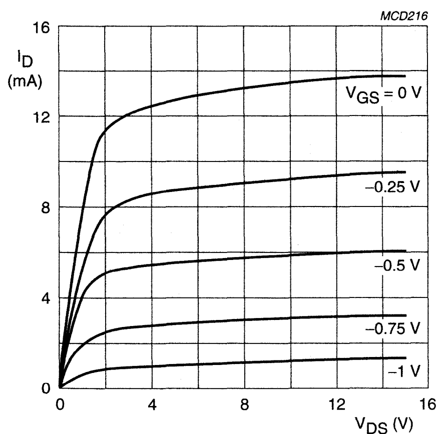
V_{DS} = 10 V; I_D = 10 mA; T_j = 25 °C.

Fig.5 Common-source output conductance as a function of gate-source cut-off voltage; typical values.



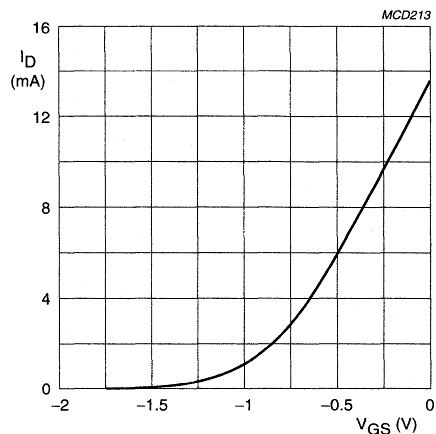
V_{DS} = 100 mV; V_{GS} = 0; T_j = 25 °C.

Fig.6 Drain-source on-state resistance as a function of gate-source cut-off voltage; typical values.



T_j = 25 °C.

Fig.7 Typical output characteristics; PMBFJ308.

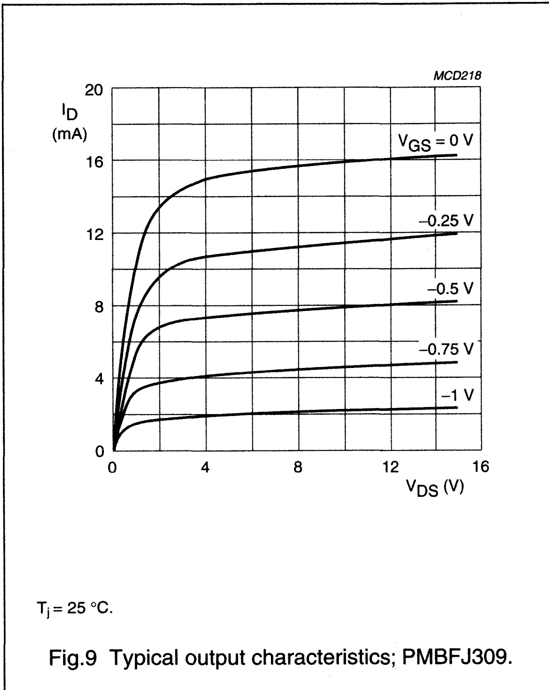


V_{DS} = 10 V; T_j = 25 °C.

Fig.8 Typical transfer characteristics; PMBFJ308.

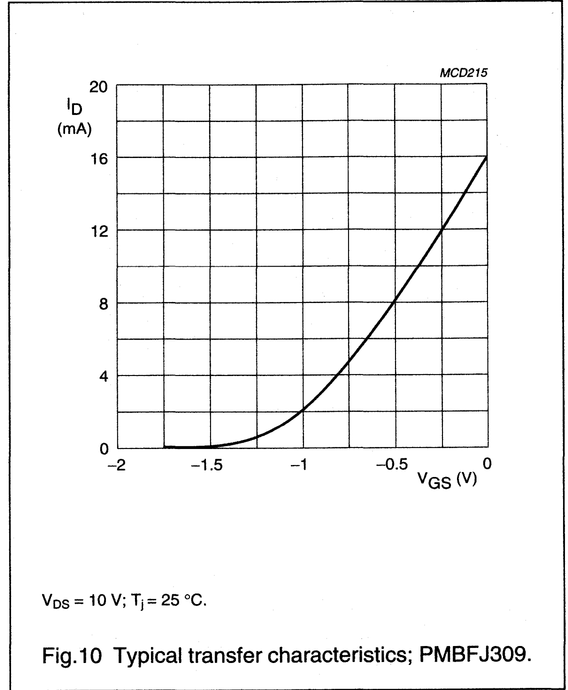
N-channel silicon field-effect transistors

PMBFJ308; PMBFJ309; PMBFJ310



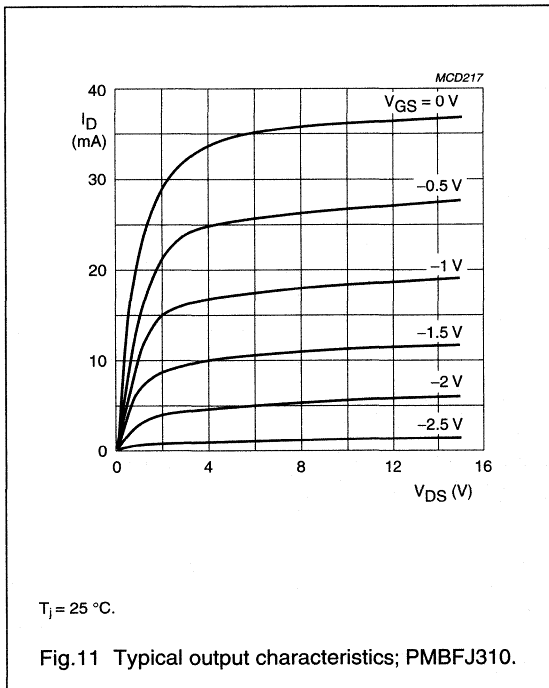
T_j = 25 °C.

Fig.9 Typical output characteristics; PMBFJ309.



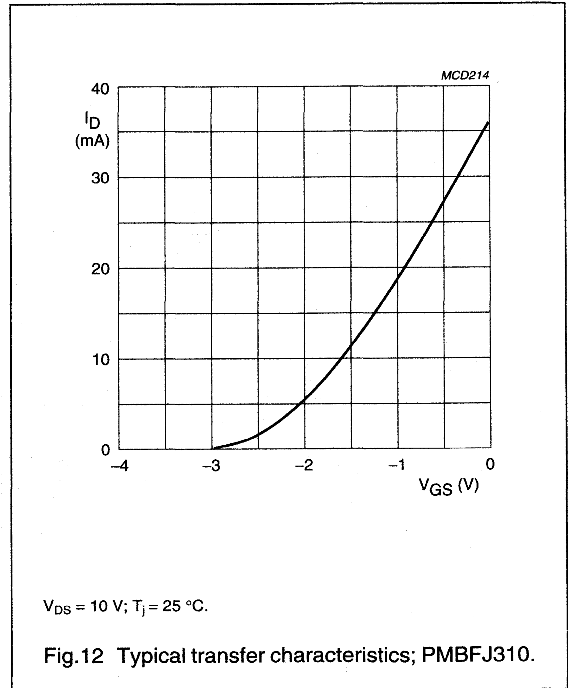
V_{DS} = 10 V; T_j = 25 °C.

Fig.10 Typical transfer characteristics; PMBFJ309.



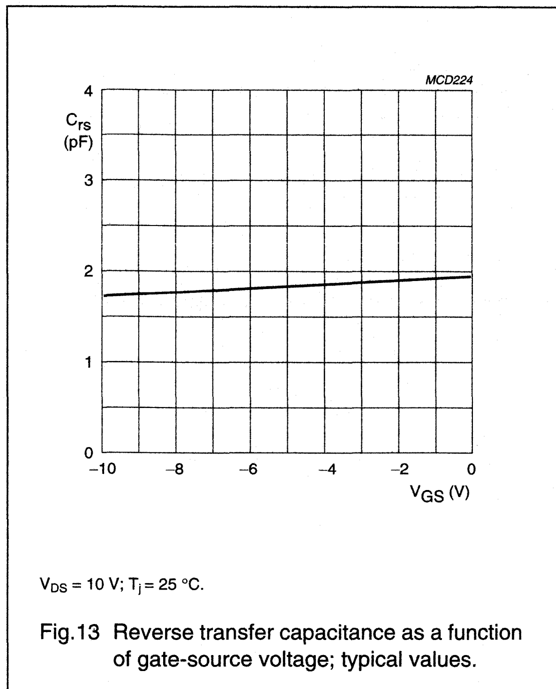
T_j = 25 °C.

Fig.11 Typical output characteristics; PMBFJ310.



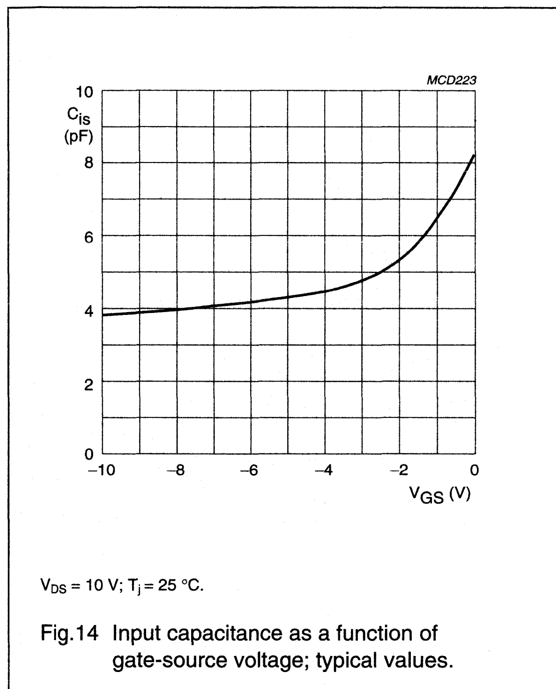
V_{DS} = 10 V; T_j = 25 °C.

Fig.12 Typical transfer characteristics; PMBFJ310.



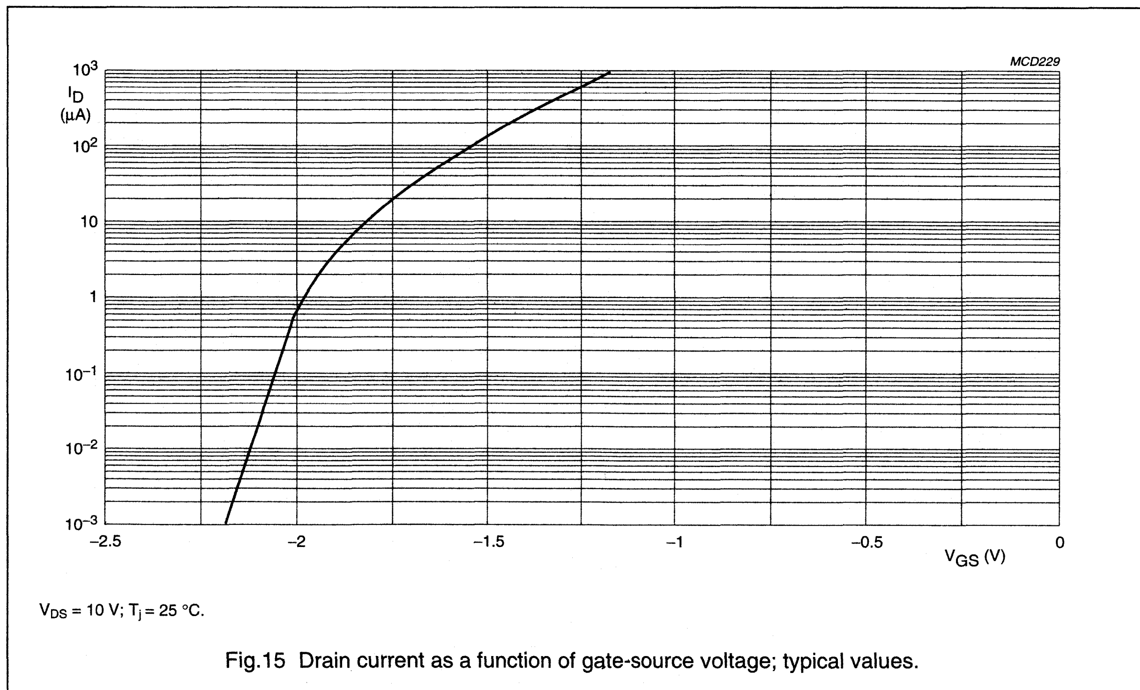
V_{DS} = 10 V; T_j = 25 °C.

Fig.13 Reverse transfer capacitance as a function of gate-source voltage; typical values.



V_{DS} = 10 V; T_j = 25 °C.

Fig.14 Input capacitance as a function of gate-source voltage; typical values.



V_{DS} = 10 V; T_j = 25 °C.

Fig.15 Drain current as a function of gate-source voltage; typical values.

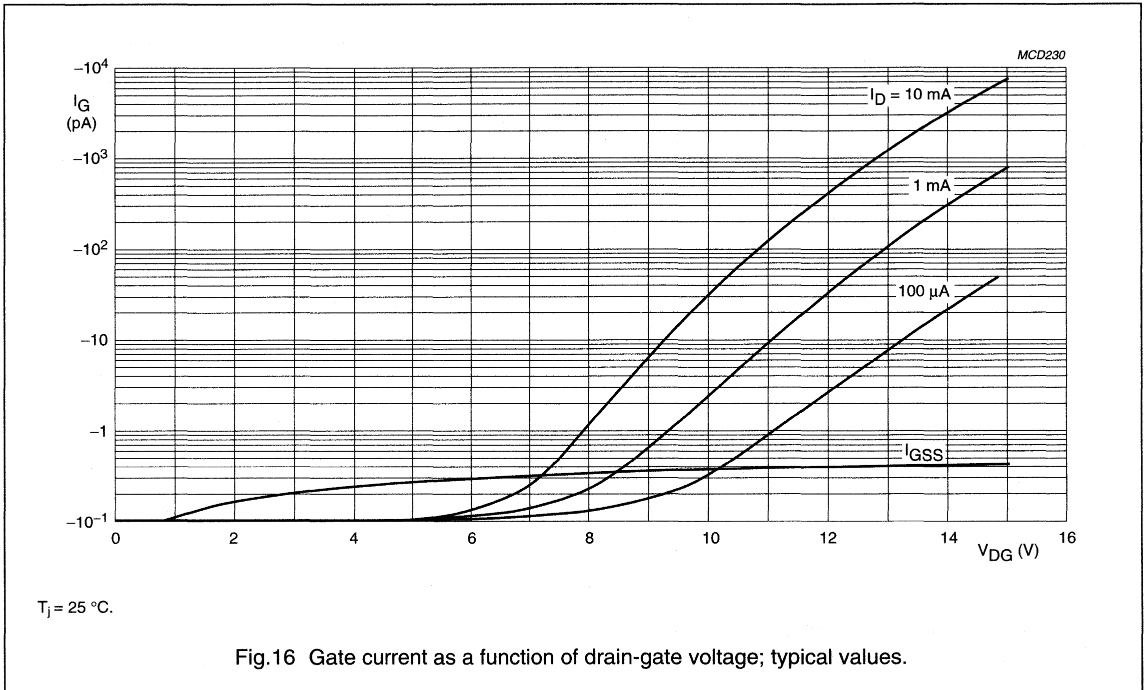


Fig.16 Gate current as a function of drain-gate voltage; typical values.

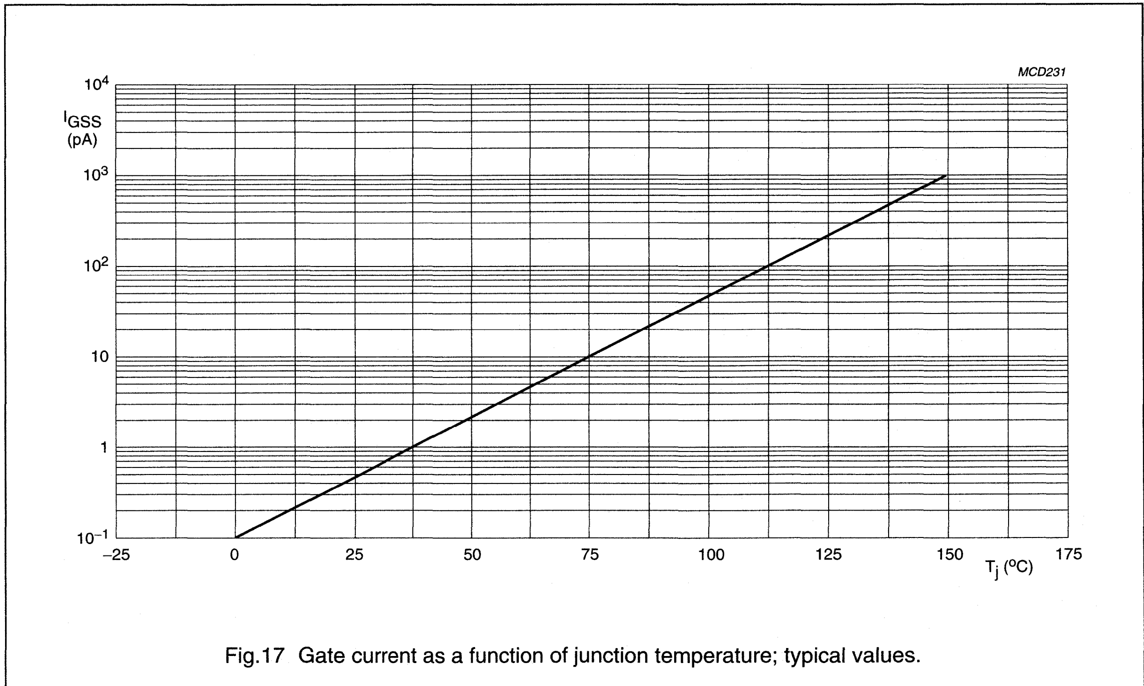
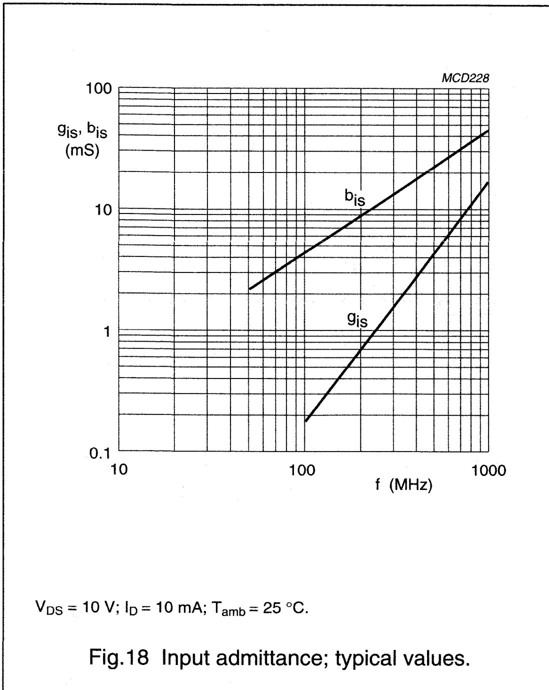
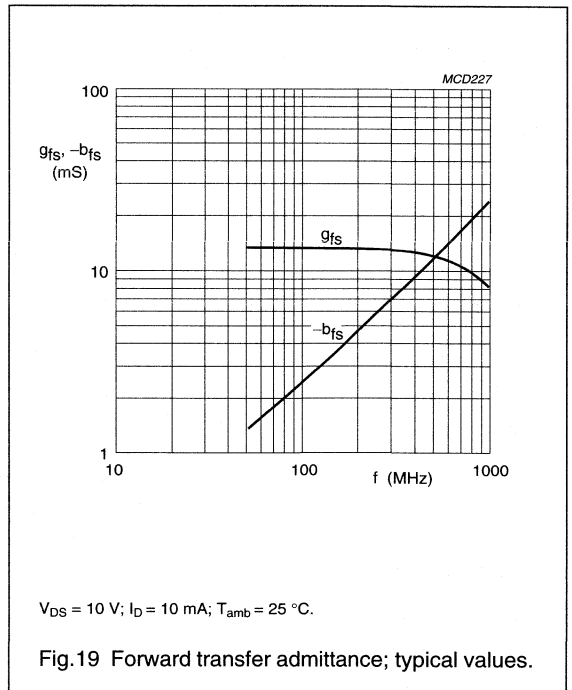


Fig.17 Gate current as a function of junction temperature; typical values.



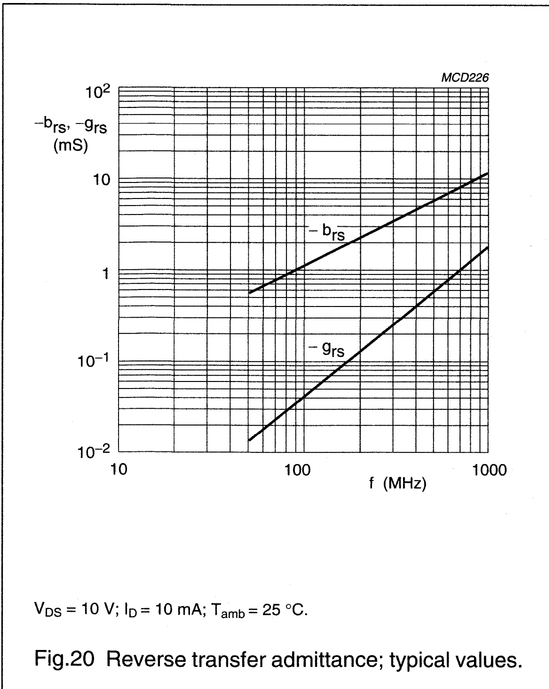
V_{DS} = 10 V; I_D = 10 mA; T_{amb} = 25 °C.

Fig.18 Input admittance; typical values.



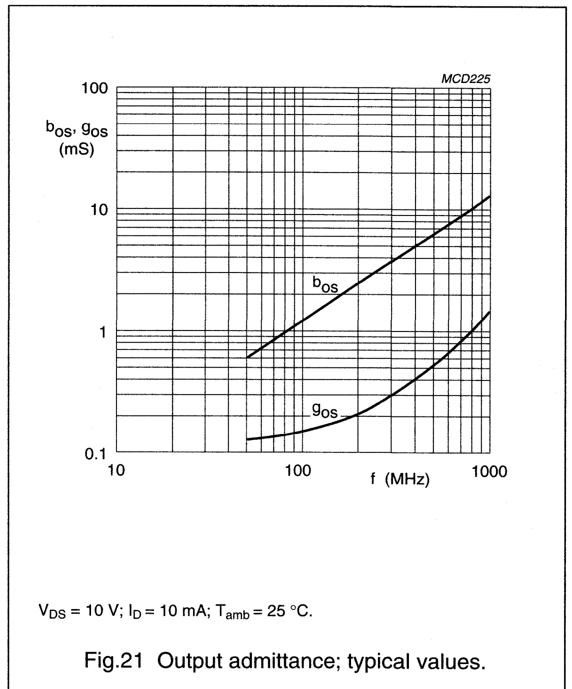
V_{DS} = 10 V; I_D = 10 mA; T_{amb} = 25 °C.

Fig.19 Forward transfer admittance; typical values.



V_{DS} = 10 V; I_D = 10 mA; T_{amb} = 25 °C.

Fig.20 Reverse transfer admittance; typical values.



V_{DS} = 10 V; I_D = 10 mA; T_{amb} = 25 °C.

Fig.21 Output admittance; typical values.

N-channel silicon field-effect transistors — PN4391 to 4393

DESCRIPTION

Symmetrical silicon n-channel junction FETs in plastic TO-92 envelopes. They are intended for applications such as analog switches, choppers, commutators etc.

PINNING

1 = gate
2 = source
3 = drain

Note: Drain and source are interchangeable.

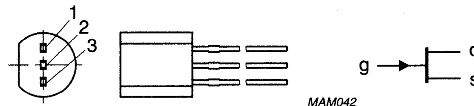


Fig.22 Simplified outline and symbol, TO-92.

QUICK REFERENCE DATA

Parameter	Symbol		PN4391	PN4392	PN4393	Unit
Drain-source voltage	$\pm V_{DS}$	max.		40		V
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.		360		mW
Drain current V_{DS} = 20 V; V_{GS} = 0	I_{DSS}	min.	50	25	5	mA
Gate-source cut-off voltage V_{DS} = 20 V; I_D = 1 nA	$-V_{GS\,off}$	min.	4	2	0.5	V
		max.	10	5	3	V
Drain-source on-resistance I_D = 1 mA; V_{GS} = 0	$R_{DS\,on}$	max.	30	60	100	Ω

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Parameter	Symbol		Value	Unit
Drain-source voltage	$\pm V_{DS}$	max.	40	V
Gate-source voltage	$-V_{GSO}$	max.	40	V
Gate-drain voltage	$-V_{GDO}$	max.	40	V
Forward gate current (DC)	I_G	max.	50	mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	360	mW
Storage temperature range	T_{stg}		−65 to+150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient in free air $R_{th\ j\text{-}a}$ = 350 K/W

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Parameter	Symbol		PN4391	PN4392	PN4393	Unit
Reverse gate current						
$-V_{GS}$ = 20 V; V_{DS} = 0	$-I_{GSS}$	max.	1.0	1.0	1.0	nA
$-V_{GS}$ = 20 V; V_{DS} = 0; T_{amb} = 100 °C	$-I_{GSS}$	max.	200	200	200	nA
Drain cut-off current						
$-V_{GS}$ = 12 V; V_{DS} = 20 V	I_{DSX}	max.	1.0			nA
$-V_{GS}$ = 7 V; V_{DS} = 20 V	I_{DSX}	max.		1.0		nA
$-V_{GS}$ = 5 V; V_{DS} = 20 V	I_{DSX}	max.			1.0	nA
$-V_{GS}$ = 12 V; V_{DS} = 20 V; T_{amb} = 100 °C	I_{DSX}	max.	200			nA
$-V_{GS}$ = 7 V; V_{DS} = 20 V; T_{amb} = 100 °C	I_{DSX}	max.		200		nA
$-V_{GS}$ = 5 V; V_{DS} = 20 V; T_{amb} = 100 °C	I_{DSX}	max.			200	nA
Drain saturation current						
V_{DS} = 20 V; V_{GS} = 0	I_{DSS}	min.	50	25	5	mA
		max.	150	100	60	mA
Gate-source breakdown voltage						
$-I_G$ = 1 µA; V_{DS} = 0	$-V_{(BR)GSS}$	min.	40	40	40	V
Gate-source cut-off voltage						
V_{DS} = 20 V; I_D = 1 nA	$-V_{GS\ off}$	min.	4.0	2.0	0.5	V
		max.	10	5.0	3.0	V
Drain-source on-resistance						
I_D = 1 mA; V_{GS} = 0	$R_{DS\ on}$	max.	30	60	100	Ω
Drain-source on-voltage						
V_{GS} = 0; I_D = 12 mA	$V_{DS\ on}$	max.	0.4			V
V_{GS} = 0; I_D = 6 mA	$V_{DS\ on}$	max.		0.4		V
V_{GS} = 0; I_D = 3 mA	$V_{DS\ on}$	max.			0.4	V

DYNAMIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

			PN4391	PN4392	PN4393	
Drain-source on-resistance						
V_{DS} = 0 V; V_{GS} = 0; f = 1 kHz; T_a = 25 °C	$R_{DS\,on}$	max.	30	60	100	Ω
Input capacitance						
V_{DS} = 20 V; V_{GS} = 0; f = 1 MHz; T_a = 25 °C	C_{iss}	max.	16	16	16	pF
Feedback capacitance						
V_{DS} = 0; $-V_{GS}$ = 12 V; f = 1 MHz	C_{rss}	max.	5			pF
V_{DS} = 0; $-V_{GS}$ = 7 V; f = 1 MHz	C_{rss}	max.		5		pF
V_{DS} = 0; $-V_{GS}$ = 5 V; f = 1 MHz	C_{rss}	max.			5	pF
Switching times						
test conditions						
V_{DD} = 10 V; V_{GS} = 0 to $V_{GS\,off}$	I_D	=	12	6.0	3.0	mA
	$-V_{GS\,off}$	=	12	7.0	5.0	V
	R_L	=	750	1550	3150	Ω
Rise time	t_r	max.	5	5	5	ns
Turn-on time	t_{on}	max.	15	15	15	ns
Fall time	t_f	max.	15	20	30	ns
Turn-off time	t_{off}	max.	20	35	50	ns

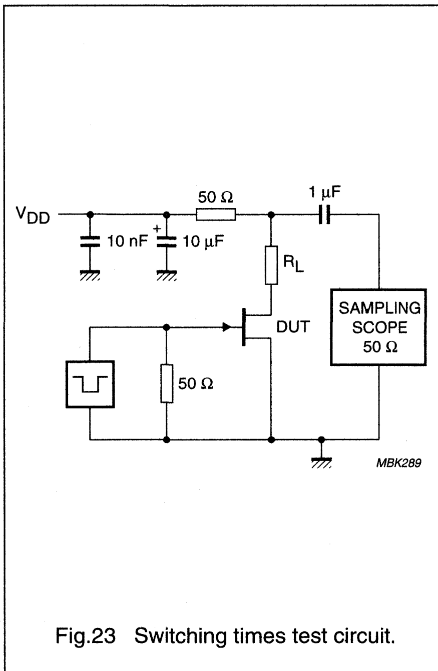


Fig.23 Switching times test circuit.

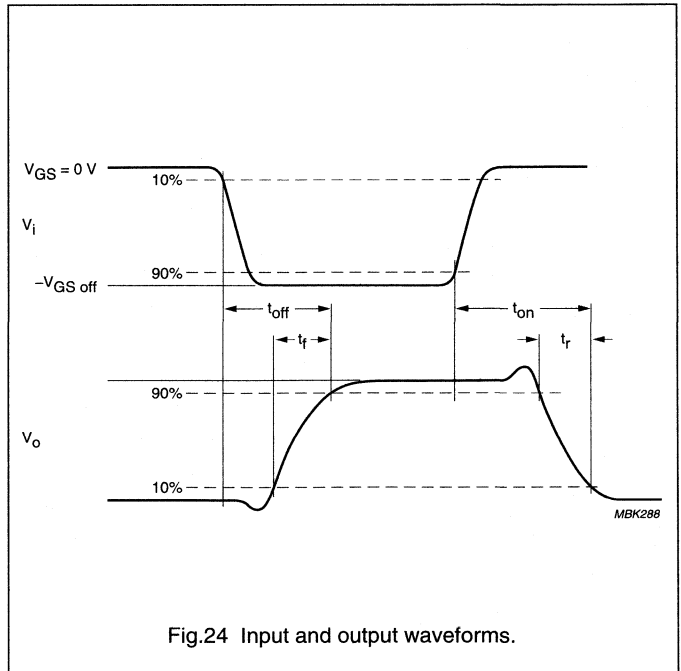


Fig.24 Input and output waveforms.

N-channel field-effect transistor PN4416; PN4416A

FEATURES

- Low noise
- Interchangeability of drain and source connections
- High gain.

DESCRIPTION

N-channel symmetrical silicon junction FETs in a SOT54 envelope. These devices are intended for use in VHF/UHF amplifiers, oscillators and mixers.

PINNING - SOT54 (TO-92).

PIN	DESCRIPTION
1	gate
2	source
3	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage				
	PN4416		–	30	V
	PN4416A		–	35	V
I_{DSS}	drain current	V_{DS} = 15 V; V_{GS} = 0	5	15	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C	–	400	mW
$V_{GS(off)}$	gate-source cut-off voltage	V_{DS} = 15 V; I_D = 1 nA			
	PN4416		–	−6	V
	PN4416A		−2.5	−6	V
$\|Y_{fs}\|$	common-source transfer admittance	V_{DS} = 15 V; V_{GS} = 0; f = 1 kHz	4.5	7.5	mS

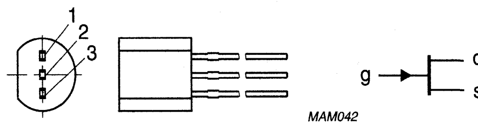


Fig.1 Simplified outline and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage				
	PN4416		–	30	V
	PN4416A		–	35	V
V_{GSO}	gate-source voltage				
	PN4416		–	–30	V
	PN4416A		–	–35	V
V_{GDO}	gate-drain voltage				
	PN4416		–	–30	V
	PN4416A		–	–35	V
I_G	DC forward gate current		–	10	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C (note 1)	–	400	mW
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j-a}$	from junction to ambient (note 1)	350 K/W

Note

1. Mounted on a printed-circuit board, maximum lead length 4 mm, mounting pad for drain leads 10 mm^2.

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{(BR)GSS}$	gate-source breakdown voltage	V_{DS} = 0; I_G = –1 μA			
	PN4416		–30	–	V
	PN4416A		–35	–	V
I_{GSS}	reverse gate leakage current	V_{DS} = 0; V_{GS} = –15 V	–	–1	nA
I_{DSS}	drain current	V_{DS} = 15 V; V_{GS} = 0	5	15	mA
V_{GSS}	gate-source forward voltage	V_{DS} = 0; I_G = 1 mA	–	1	V
$V_{GS(off)}$	gate-source cut-off voltage	V_{DS} = 15 V; I_D = 1 nA			
	PN4416		–	–6	V
	PN4416A		–2.5	–6	V
$\|Y_{fs}\|$	common source transfer admittance	V_{DS} = 15 V; V_{GS} = 0	4.5	7.5	mS
$\|Y_{os}\|$	common source output admittance	V_{DS} = 15 V; V_{GS} = 0			
	PN4416		–	50	μS
	PN4416A		–	50	μS

DYNAMIC CHARACTERISTICS

T_j = 25 °C; V_{DS} = 15 V; V_{GS} = 0.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_{is}	input capacitance	f = 1 MHz	–	–	4	pF
C_{os}	output capacitance	f = 1 MHz	–	–	2	pF
C_{rs}	feedback capacitance	f = 1 MHz	–	–	0.8	pF
g_{is}	common source input conductance	f = 100 MHz	–	–	100	μS
		f = 400 MHz	–	–	1	mS
g_{fs}	common source transfer conductance	f = 100 MHz	–	5.2	–	mS
		f = 400 MHz	4	5	–	mS
g_{rs}	common source feedback conductance	f = 100 MHz	–	–8	–	μS
		f = 400 MHz	–	–100	–	μS
g_{os}	common source output conductance	f = 100 MHz	–	–	75	μS
		f = 400 MHz	–	–	100	μS
V_n	equivalent input noise voltage	f = 100 Hz	–	5	–	nV/√Hz

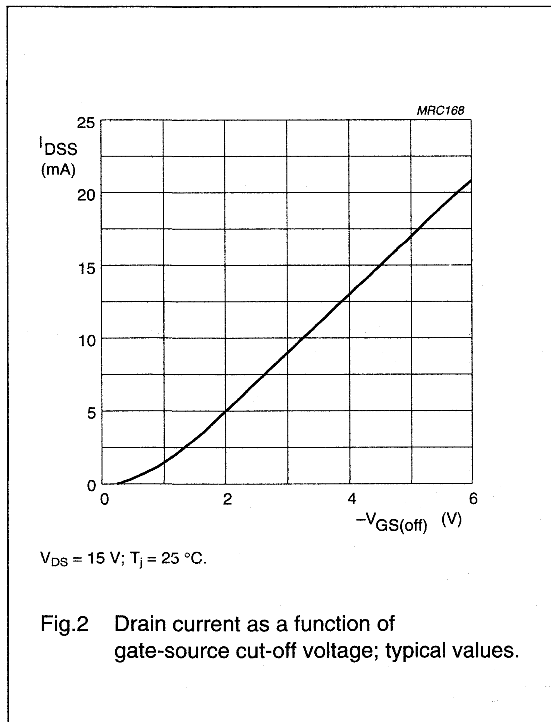


Fig.2 Drain current as a function of gate-source cut-off voltage; typical values.

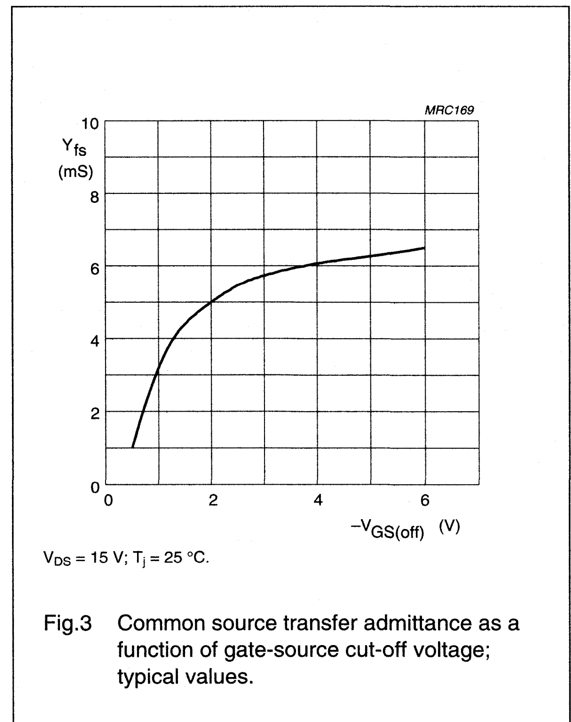
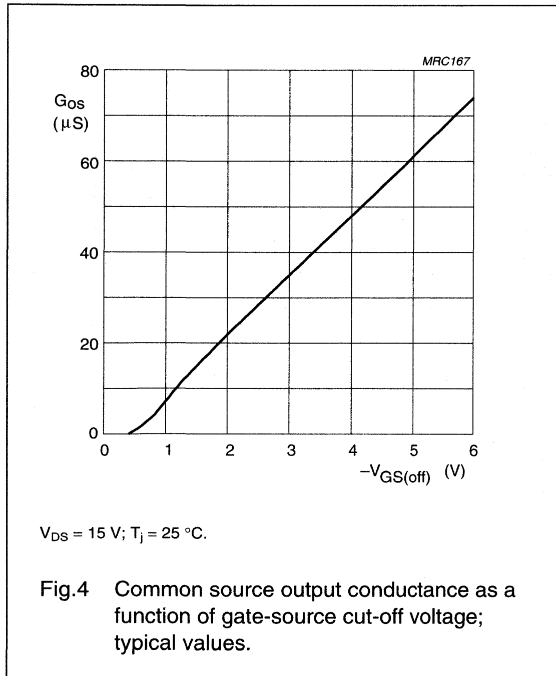
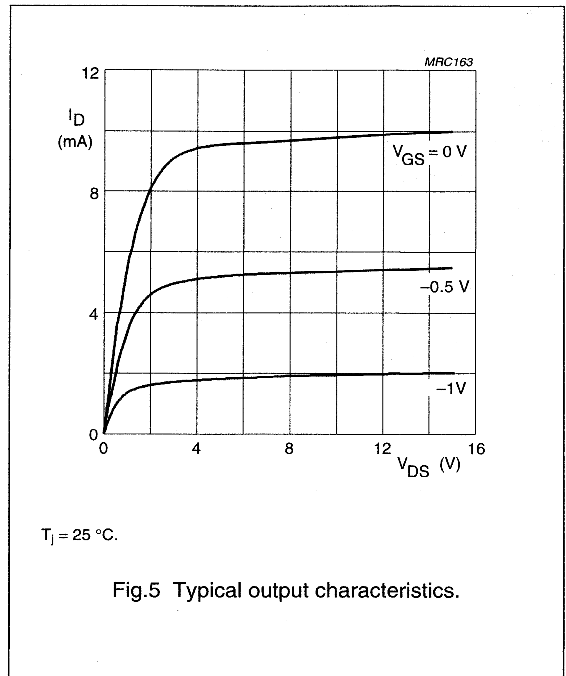


Fig.3 Common source transfer admittance as a function of gate-source cut-off voltage; typical values.



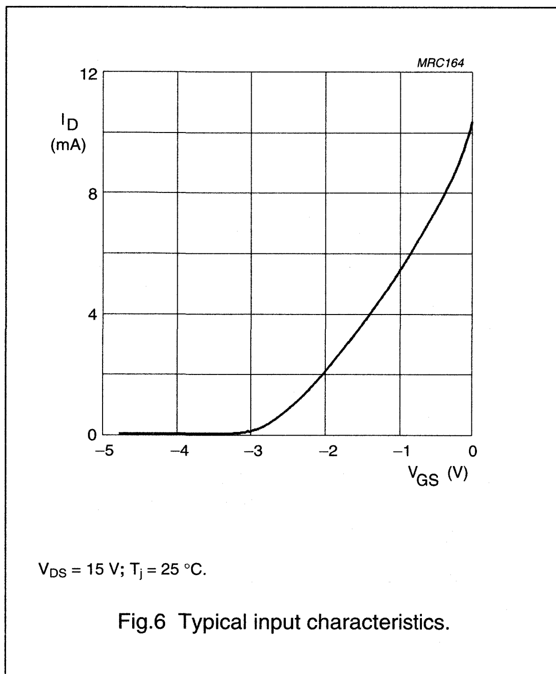
V_{DS} = 15 V; T_j = 25 °C.

Fig.4 Common source output conductance as a function of gate-source cut-off voltage; typical values.



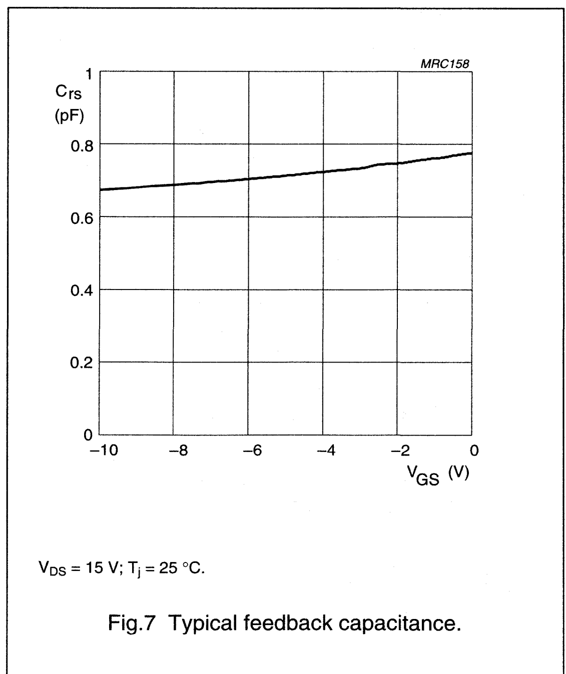
T_j = 25 °C.

Fig.5 Typical output characteristics.



V_{DS} = 15 V; T_j = 25 °C.

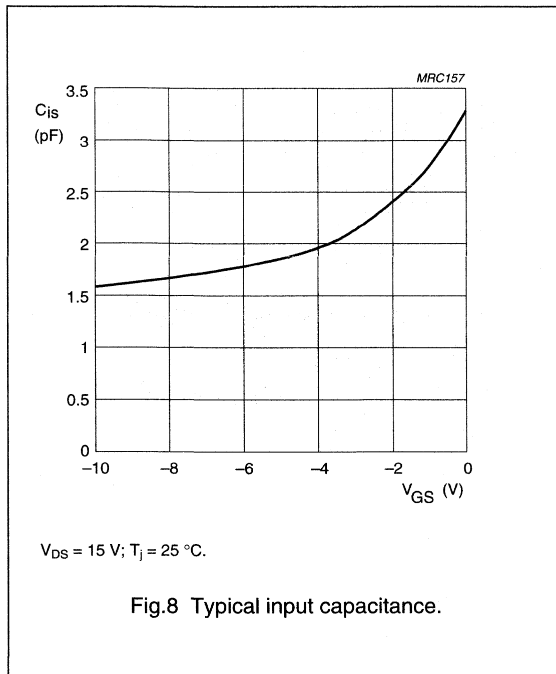
Fig.6 Typical input characteristics.



V_{DS} = 15 V; T_j = 25 °C.

Fig.7 Typical feedback capacitance.

N-channel field-effect transistor PN4416; PN4416A



V_{DS} = 15 V; T_j = 25 °C.

Fig.8 Typical input capacitance.

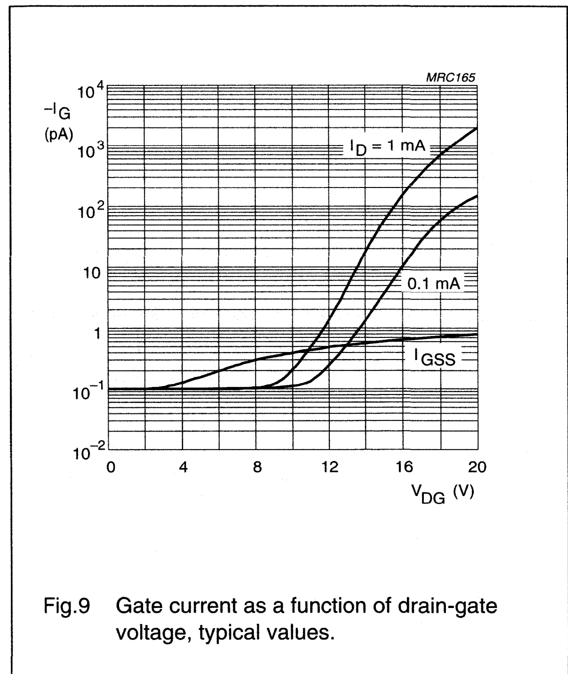


Fig.9 Gate current as a function of drain-gate voltage, typical values.

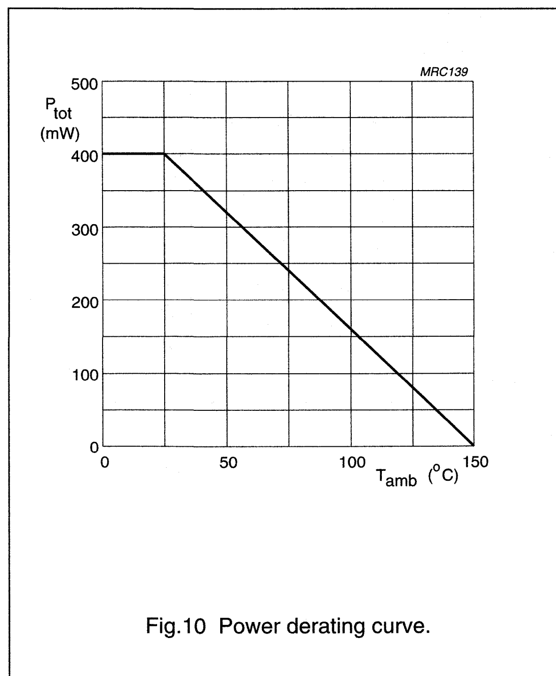
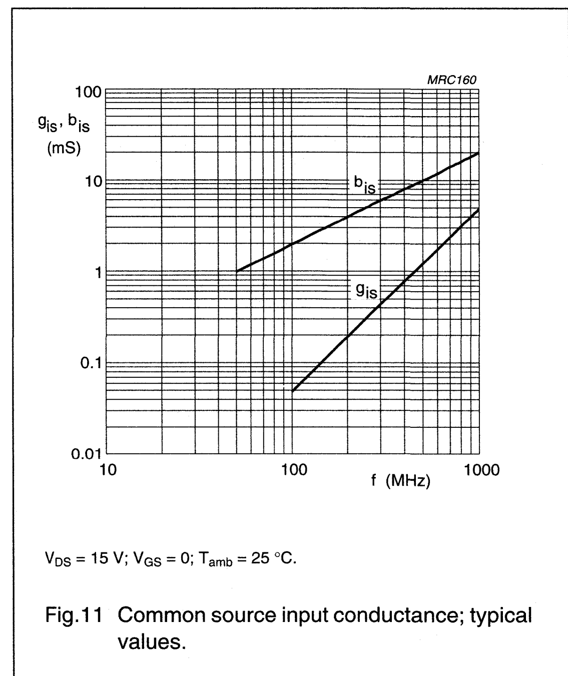
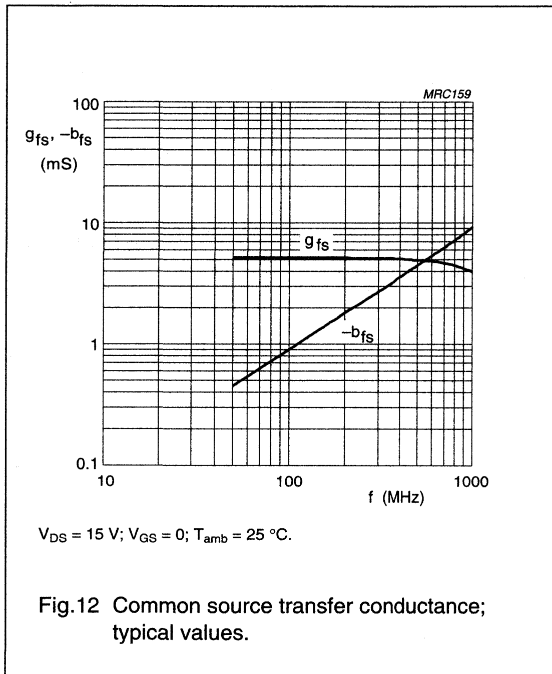


Fig.10 Power derating curve.



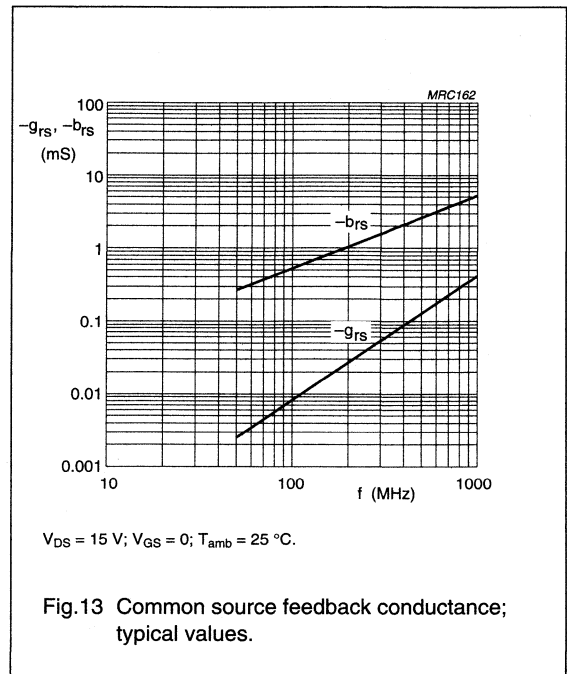
V_{DS} = 15 V; V_{GS} = 0; T_{amb} = 25 °C.

Fig.11 Common source input conductance; typical values.



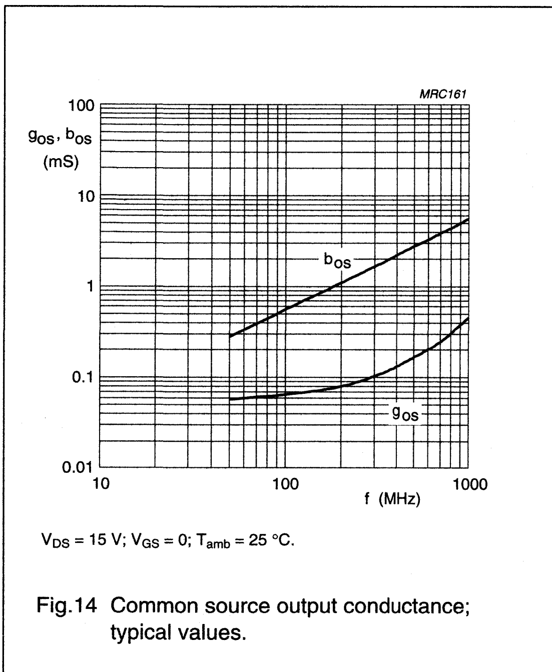
V_{DS} = 15 V; V_{GS} = 0; T_{amb} = 25 °C.

Fig.12 Common source transfer conductance; typical values.



V_{DS} = 15 V; V_{GS} = 0; T_{amb} = 25 °C.

Fig.13 Common source feedback conductance; typical values.



V_{DS} = 15 V; V_{GS} = 0; T_{amb} = 25 °C.

Fig.14 Common source output conductance; typical values.

SPICE parameters for PN4416

September 1992; version 1.0.

1	VTO = −3.553	V
2	BETA = 792.6	μA/V²
3	LAMBDA = 18.46	m/V
4	RD = 7.671	Ω
5	RS = 7.671	Ω
6	IS = 333.4	aA
7	CGSO = 2.920	pF
8	CGDO = 2.261	pF
9	PB = 1.090	V
10 (note 1)	FC = 500.0	m

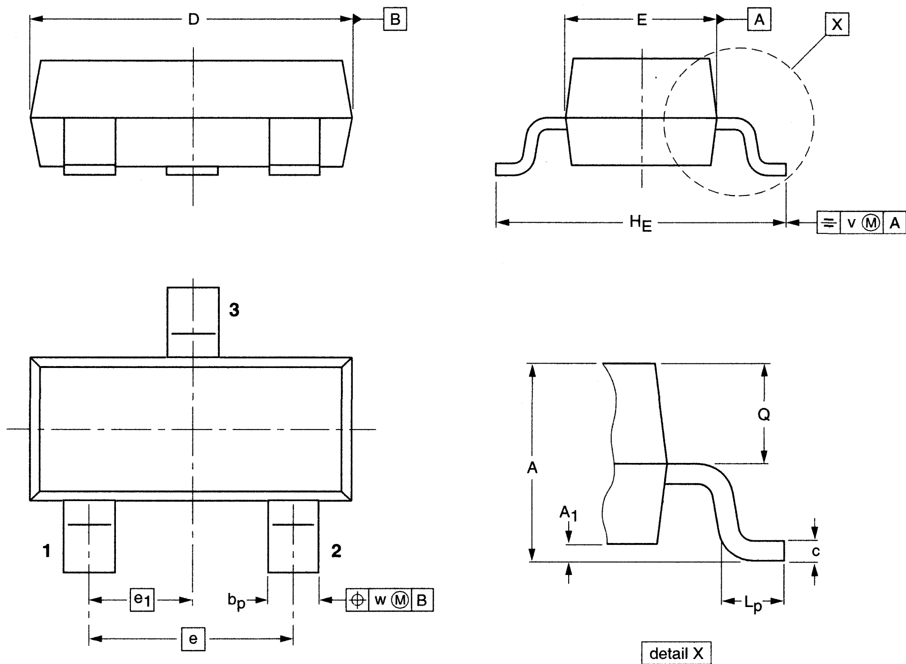
Note

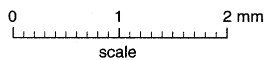
1. Parameter not extracted; default value.

PACKAGE OUTLINES

	Page
SOT23	346
SOT54	347
SOT54 variant	348
SOT143B	349
SOT143R	350
SOT343R	351

Plastic surface mounted package; 3 leads **SOT23**



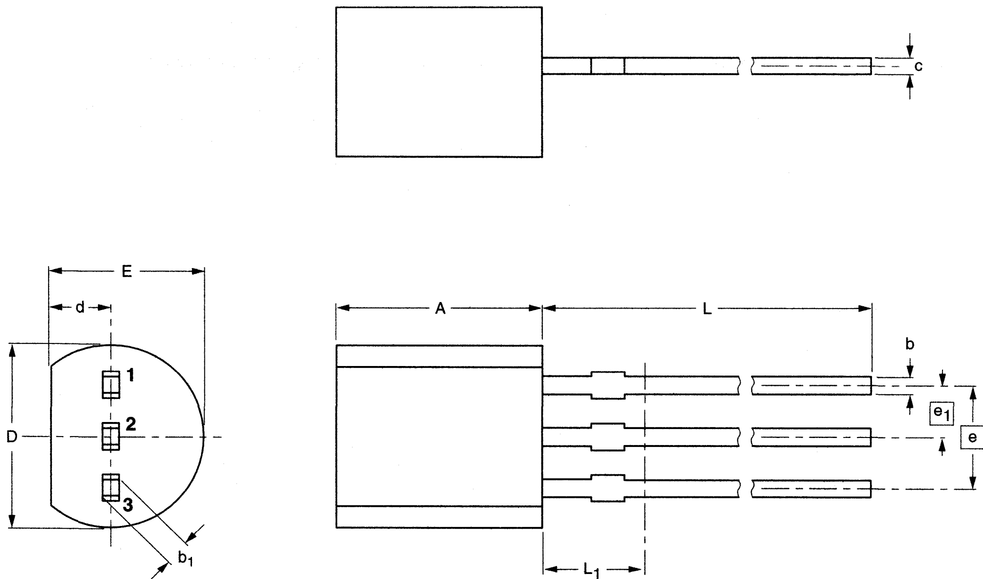


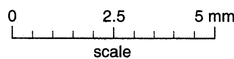
DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 max.	b_p	c	D	E	e	e_1	H_E	L_p	Q	v	w
mm	1.1 0.9	0.1	0.48 0.38	0.15 0.09	3.0 2.8	1.4 1.2	1.9	0.95	2.5 2.1	0.45 0.15	0.55 0.45	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT23						97-02-28

Plastic single-ended leaded (through hole) package; 3 leads **SOT54**





DIMENSIONS (mm are the original dimensions)

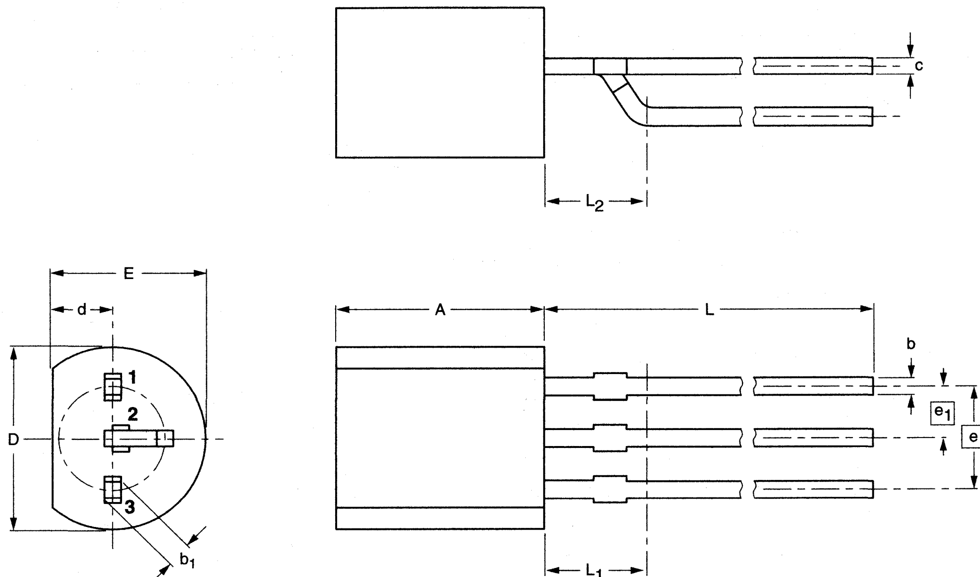
UNIT	A	b	b_1	c	D	d	E	e	e_1	L	L_1(1)
mm	5.2 5.0	0.48 0.40	0.66 0.56	0.45 0.40	4.8 4.4	1.7 1.4	4.2 3.6	2.54	1.27	14.5 12.7	2.5

Note

1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT54		TO-92	SC-43			97-02-28

Plastic single-ended leaded (through hole) package; 3 leads (on-circle) **SOT54 variant**



DIMENSIONS (mm are the original dimensions)

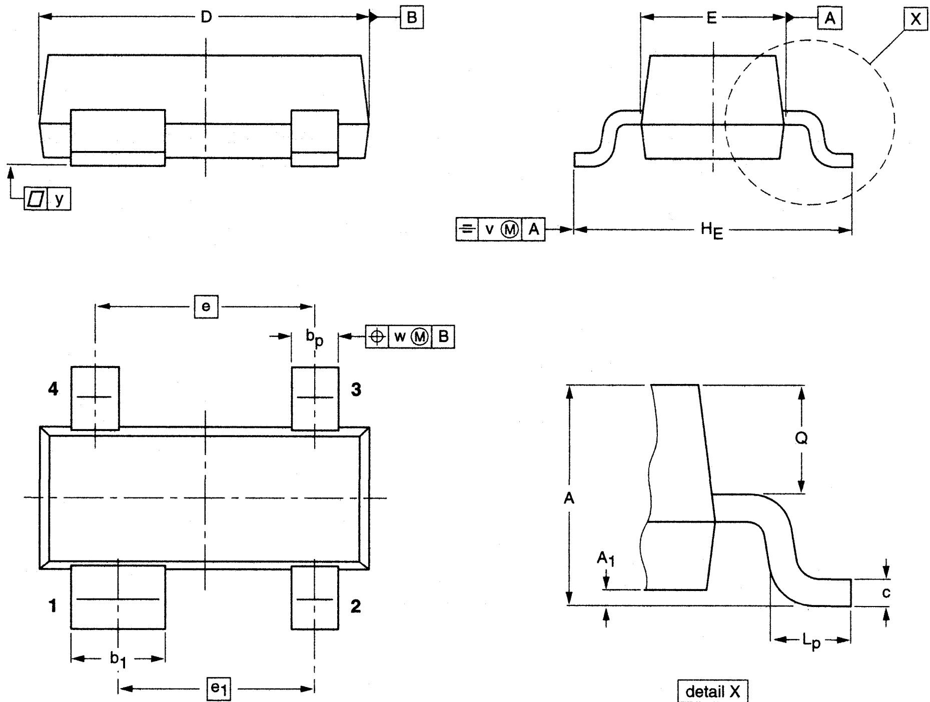
UNIT	A	b	b_1	c	D	d	E	e	e_1	L	$L_1^{(1)}$ max	L_2 max
mm	5.2 5.0	0.48 0.40	0.66 0.56	0.45 0.40	4.8 4.4	1.7 1.4	4.2 3.6	2.54	1.27	14.5 12.7	2.5	2.5

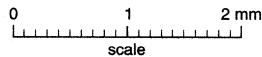
Notes

1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT54 variant		TO-92	SC-43			97-04-14

Plastic surface mounted package; 4 leads **SOT143B**



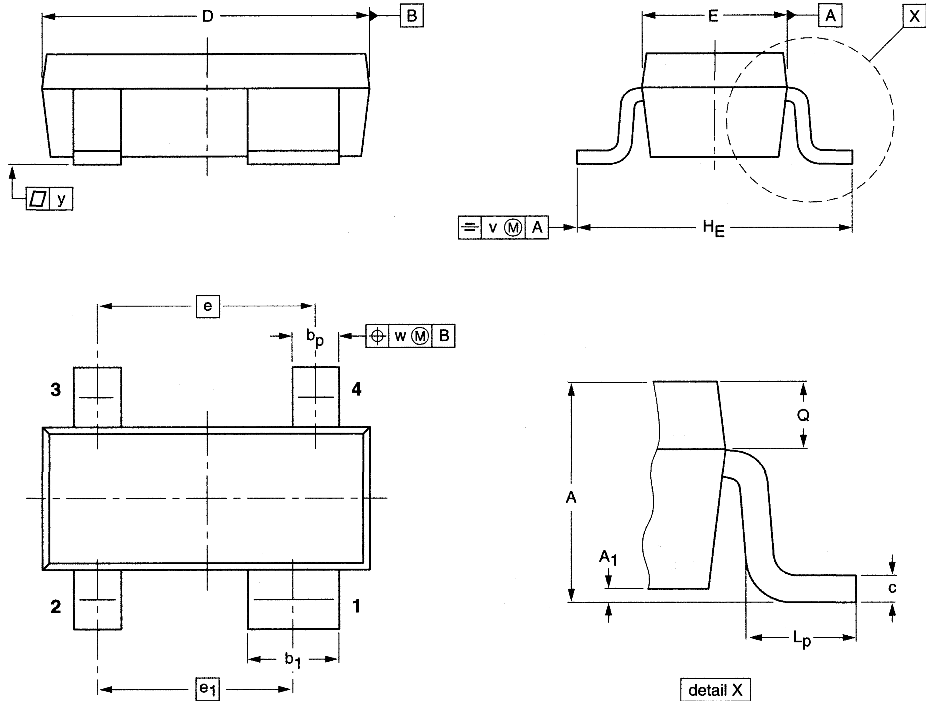


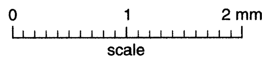
DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 max	b_p	b_1	c	D	E	e	e_1	H_E	L_p	Q	v	w	y
mm	1.1 0.9	0.1	0.48 0.38	0.88 0.78	0.15 0.09	3.0 2.8	1.4 1.2	1.9	1.7	2.5 2.1	0.45 0.15	0.55 0.45	0.2	0.1	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT143B						97-02-28

Plastic surface mounted package; reverse pinning; 4 leads **SOT143R**



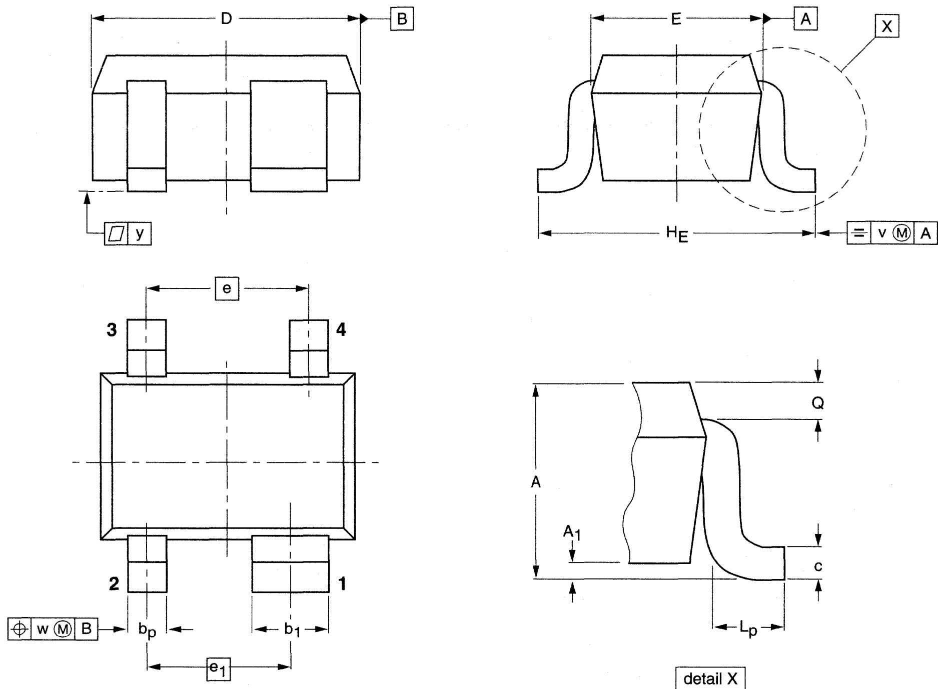


DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 max	b_p	b_1	c	D	E	e	e_1	H_E	L_p	Q	v	w	y
mm	1.1 0.9	0.1	0.48 0.38	0.88 0.78	0.15 0.09	3.0 2.8	1.4 1.2	1.9	1.7	2.5 2.1	0.55 0.25	0.45 0.25	0.2	0.1	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT143R						97-03-10

Plastic surface mounted package; reverse pinning; 4 leads **SOT343R**



0 1 2 mm
scale

DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 max	b_p	b_1	c	D	E	e	e_1	H_E	L_p	Q	v	w	y
mm	1.1 0.8	0.1	0.4 0.3	0.7 0.5	0.25 0.10	2.2 1.8	1.35 1.15	1.3	1.15	2.2 2.0	0.45 0.15	0.23 0.13	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT343R						97-05-21

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Data handbook system

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MA04	Dry-reed Switches

Passive components

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PA03	Potentiometers
PA04	Variable Capacitors
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